MAX32670/MAX32671 ERRATA SHEET

Revision A1 Errata

The errata listed below describe situations where components of this revision perform differently than expected or differently than described in the data sheet. Maxim Integrated Products, Inc. may, at its own discretion, take future steps to correct these errata when the opportunity to redesign the product presents itself. Prior to that, Maxim has determined the following potential workarounds that customers may want to consider when addressing one of the situations described below.

This errata sheet only applies to components of this revision. These components are branded on the topside of the package with a six-digit code in the form yywwRR, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively, and RR is the revision of the component. To obtain an errata sheet on other die revisions, visit the Maxim website at www.maximintegrated.com/errata.

1) DEVICE IS ONLY RESET BY POR WHEN FLASH MEMORY PAGES ARE LOCKED

Description:
The device is only reset by a POR if the flash memory protection is enabled. This can occur:
- When the bootloader executes the LOCK or PERMLOCK command.
- If the flash memory protection is enabled through a GDB command.

Workaround:
Only use POR to reset the device when one or more flash memory pages are locked. Do not use GCR_RSTR0.sys, the external RSTN pin, or the internal WDT timer to generate a reset.

2) LPUART STOP BIT ONE BIT TIME LONGER THAN EXPECTED

Description:
The length of the stop bit selected by the UARTn_CTRL.stopbits field is: (15238)

0: 2 stop bits

1: 2.5 stop bits (for 5 bit mode) or 3 stop bits (for 6/7/8 bit mode)

Workaround:
None.

3) 32kHz OSCILLATOR DOES NOT DISABLE IN LOW-POWER MODES

Description:
The 32kHz oscillator is always enabled when the device is in any mode other than ACTIVE, regardless of whether GCR.CLKCN.xclken has been set to 1 or 0. (15243)

Workaround:
None.

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4) DEVICE MUST OPERATE FROM 100MHz DEFAULT OSCILLATOR

Description:
The device will not operate as expected if a system oscillator other than the default IPO is selected.
(15280)

Workaround:
None. Do not change the system oscillator from its default value.

5) TMR AND LPTMR INSTANCES DO NOT RECOGNIZE POSITIVE EDGE DETECT INPUT SIGNALS LESS THAN 2 TIMER CLOCK CYCLES

Description:
External signals must be at least active for at least two timer clock cycles when configured to detect a positive edge. (15255)

Workaround:
External signals less than two timer clock signals can be detected by triggering on the falling edge of the external signal (TMRn_CTRL0.negtrig_a = 1 and or TMRn_CTRL0.negtrig_b =1).

6) DEVICE PINS ASSOCIATED WITH LPTIMER AND LPUART INSTANCES WILL NOT FUNCTION AS GPIO AFTER THE PERIPHERAL CLOCK IS ENABLED

Description:
All of the pins associated with an instance of an LPTIMER or LPUART will no longer operate with the GPIO functionality after the first time that peripheral clock is enabled. All of the alternate functions associated with the device pins operate correctly. (15276)

Workaround:
Do not use the device pins associated with an instance of an LPTIMER or LPUART once its peripheral clock has been enabled.

7) WDT FEED SEQUENCE NOT REQUIRED FOR ACCESS TO WDT_CTRL.en

Description:
The WDT_CTRL.en field is not write protected by the WDT feed sequence. (15292)

Workaround:
None. On B version silicon, unique feed sequences will be required for resetting the WDT count, writing WDT_CTRL.en to 1, and writing WDT_CTRL.en to 0.

8) SOME GPIO DO NOT ISOLATE WHEN V$_{DD}$ = 0V

Description:
The maximum voltage on P0.[2, 4, 5, 7] must be equal to or less than V$_{DD}$ + 0.3V.

Workaround:
None.

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/21	Initial release	—
1	3/22	Added erratum 8	2

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