DS28E02 ERRATA SHEET

Revision A1 Errata

The errata listed below describe situations where DS28E02 revision A1 components perform differently than expected or differently than described in the data sheet. Maxim Integrated Products, Inc., intends to correct these errata when the opportunity to redesign the product presents itself.

This errata sheet only applies to DS28E02 revision A1 components. To obtain an errata sheet on another DS28E02 die revision, visit our website at www.maximintegrated.com/errata.

Revision A1 components are branded on the topside of a TDFN package with a five-digit code in the form YM$$*, where Y and M are one-digit numbers representing the year and month of manufacture, respectively. The $$ represents the revision and the asterisk (*) represents the factory code.

**TOP SIDE - TDFN Markings**

```
+  
28E02  
YM$$*  
```

Revision A1 components are branded on the topside of a TSOC package with a five-digit code in the form of YWW$$, where Y is the last digit of the year of assembly and WW is the week of assembly. The $$ represents the revision.

**TOP SIDE - TSOC Markings**

```
+ O  
DS        
28E02  
YWWS$  
```
1) INITIAL SLOW POWER RAMP RESULTS IN FASTER 1-Wire TIMING

Description:
During power-on reset, a trim value is copied from an EEPROM location to the circuit that controls the DS28E02’s timing. If $t_{\text{RAMP}}$ is too long, the copy takes place before the EEPROM has reached its internal operating voltage. As a consequence, incorrect data is copied to the timing circuit, which in turn cannot operate within data sheet limits. This causes the 1-Wire Master to miss presence pulses or to read a logic 1 instead of a logic 0.

Workaround:
For all $t_{\text{RAMP}}$ cases, the incorrect timing is prevented if, after power-up, the 1-Wire master performs the initialization sequence ($t_{\text{H1}}$, $t_{\text{L1}}$, $t_{\text{H2}}$, $t_{\text{L2}}$, $t_{\text{H3}}$) as shown in Table 1 and Figure 1. The $t_{\text{L1}}$ segment forces a power-on reset of the DS28E02, which completes during $t_{\text{H2}}$. The fast rise time at the end of $t_{\text{L1}}$ ensures proper loading of the trim value and accurate timing.

Further, always start 1-Wire communication with a reset/presence detect sequence before issuing a 1-Wire ROM function command.

Table 1. Initialization Sequence Timing

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>RECOMMENDED TIME</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{\text{H1}}$</td>
<td>100ms</td>
</tr>
<tr>
<td>$t_{\text{L1}}$</td>
<td>100ms</td>
</tr>
<tr>
<td>$t_{\text{H2}}$</td>
<td>1ms</td>
</tr>
<tr>
<td>$t_{\text{L2}}$</td>
<td>480µs</td>
</tr>
<tr>
<td>$t_{\text{H3}}$</td>
<td>480µs</td>
</tr>
</tbody>
</table>

Figure 1. Initialization Sequence Waveform
<table>
<thead>
<tr>
<th>REVISION NUMBER</th>
<th>REVISION DATE</th>
<th>DESCRIPTION</th>
<th>PAGES CHANGED</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>11/12</td>
<td>Initial release</td>
<td>—</td>
</tr>
<tr>
<td>1</td>
<td>1/13</td>
<td>Updated erratum #1 and line style updates in Figure 1</td>
<td>2</td>
</tr>
</tbody>
</table>