



# DS89C440

## Ultra-High-Speed Flash Microcontroller

[www.maxim-ic.com](http://www.maxim-ic.com)

### REVISION A2 ERRATA

The errata listed below describe situations where DS89C440 revision A2 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS89C440 revision A2 components. Revision A2 components are branded on the top side of the package with a six-digit code in the form yywwA2, where yy and ww are two-digit numbers representing the year and workweek of manufacture, respectively. To obtain an errata sheet on another DS89C440 die revision, visit our website at [www.maxim-ic.com/errata](http://www.maxim-ic.com/errata).

#### 1. BOOTSTRAP LOADER MASS ERASE COMMAND DOES NOT CLEAR OPTION CONTROL REGISTER

**Description:**

The mass erase command of the bootstrap loader does not reset the OCR to FFh. As a result, the watchdog timer power-on reset default bit cannot be set to 1 if previously cleared.

**Work Around:**

If the watchdog timer power-on reset default bit has been cleared and needs to be reset to 1, use the erase option control register command in either in-application or parallel programming modes.

#### 2. POWER-DOWN SLEW RATE REQUIREMENT IN CRYSTAL MULTIPLIER MODE

**Description:**

The microcontroller may not reset itself following a brownout ( $0.4 < V_{CC} < V_{RST}$ ) if the crystal multiplier mode (CTM = 1) is enabled.

**Work Around:**

Performing a full power-down ( $V_{CC} = 0$ ) clears the condition. In default (1 clock per machine cycle) mode, this erratum does not occur and no work around is required.

If the crystal multiplier, in either 2X or 4X mode, is used, the device must be placed into default sysclk/1 mode before  $V_{CC}$  drops below  $V_{RST}$ . Do this by using the power-fail interrupt as follows:

- 1) Enable the power-fail interrupt before the crystal multiplier is engaged. Do this by setting the EPFI (WDCON.5) bit anytime before the CTM bit is set.
- 2) The first instruction at 0033h (the start of the power-fail interrupt service routine) must be ORL PMR, #80h. This deactivates the crystal multiplier and returns the device to default sysclk/1 mode. A user-defined power-fail interrupt service routine, if present, can follow. If no user-defined power-fail interrupt service routine is specified, the next instruction should be an endless loop.

### 3. MOVC INSTRUCTION DOES NOT FUNCTION PROPERLY IN EXTERNAL MEMORY

**Description:**

The following instructions do not function correctly when  $\overline{EA} = 0$  and the target MOVC location, @A + PC, is located in program memory external to the microcontroller:

```
MOVC A, @A + DPTR  
MOVC A, @A + PC
```

**Work Around:**

Perform all MOVC instructions on memory locations in internal flash memory.

### 4. EXTERNAL MOVX INSTRUCTIONS BLOCKED AT SECURITY LEVEL 4

**Description:**

At security Level 4 (LB3 is cleared to 0; LB2 and LB1 are don't care), internal code cannot access external MOVX memory. The stated definition of Level 4 in the data sheet permits access to external MOVX memory.

**Work Around:**

Verify the level of security required for the application and if possible select a more appropriate security level.

### 5. LOCK BIT SECURITY LEVELS 1, 2, AND 3 DO NOT FUNCTION PROPERLY

**Description:**

Security levels 1, 2, and 3 do not function properly and may not prevent access to internal flash memory if external program memory is used.

**Work Around:**

Use security level 4 if internal flash memory protection is required.