



DS89C420

Ultra-High-Speed Microcontroller

www.maxim-ic.com

REVISION A1 ERRATA

The errata listed below describe situations where DS89C420 revision A1 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS89C420 revision A1 components. Revision A1 components are branded on the top side of the package with a six-digit code in the form yywwA1, where yy and ww are two-digit numbers representing the year and workweek of manufacture, respectively. To obtain an errata sheet on another DS89C420 die revision, visit the website at www.maxim-ic.com/errata.

1. Description:

The execution of instructions with a cycle count that exceeds the byte count can cause incorrect device operation in the following conditions:

- The device is executing from internal (flash) memory, and
- An instruction opcode falls on a 256-byte page boundary (xxFFh), and
- The previous instruction is one of the following:

```

ADDC A, @Ri      DEC @Ri
MUL AB          DIV AB
DA A ORL A, @Ri
ANL A, @Ri XRL A, @Ri
MOVC (all forms) XCH A, Rn
XCH A, direct XCHD A, @Ri

INC direct*    DEC direct*
ANL direct*, A    ORL direct*, A
XRL direct*, A    MOV direct*, A
MOV direct*, Rn    MOV direct1*, direct2
MOV direct*, @Ri  POP direct*
CLR bit        SETB bit
CPL bit
  
```

**These instructions cause a failure only when the SFR is one of these: PSW, SP, DPS, IE, EIE, IP0, IP1, EIP0, or EIP1.*

Work Around:

If programming in assembly language, write the software so that the code does not allow any of the above instructions to occur such that the next opcode falls on the last byte of 256-byte page (xxFFh) boundary. If writing in C, make all routines and functions less than 256 bytes in length and use byte constants placed at xxFFh intervals in the software. This condition will be corrected on revision A2 coming shortly.

2. Description:

The auto-baud routine of the bootstrap loader does not always function reliably (observed as garbled information instead of loader banner). Functionality is better at lower baud rates. Experiments show that the maximum reliable baud rate for any given crystal frequency is given by the equation:

$$f_{\text{OSC}} / 1152 = \text{Max Baud}$$

Work Around:

Use lower baud rates. This condition will be corrected on revision A2 coming shortly.

3. Description:

The signal $\overline{\text{PSEN}}$ is driven by a strong pullup internally, and the component used to pull it down to enter loader mode must be capable of sinking 100mA of current to ground.

Work Around:

None. This condition will be corrected on revision A2 coming shortly.

4. Description:

To enter loader mode, $\overline{\text{PSEN}}$ is sampled after reset is pulled high and $\overline{\text{EA}}$ is pulled low. This dictates that the transition of $\overline{\text{PSEN}}$ from high to low should be delayed from the onset of reset and $\overline{\text{EA}}$ by 8 clock cycles. This timing relationship will be eliminated in future revisions (i.e., signals can be set simultaneously).

Work Around:

Use individual manual switches, passive circuitry (RC combinations), or active counting circuits (driven off of one of the processor's available clocks: ALE preferred) to delay the falling edge of $\overline{\text{PSEN}}$ so it will be sampled correctly (i.e., 8 oscillator clocks or more after reset and $\overline{\text{EA}}$ are set). This condition will be corrected on revision A2 coming shortly.

5. Description:

If the oscillator is stopped or fails for any reason, the oscillator fail detect circuitry will cause a long delay in processor restart even though the oscillator fail detect reset function is disabled.

Work Around:

None. This condition will be corrected on revision A2 coming shortly.

6. Description:

Presently available sample devices (labeled ES) were tested successfully at 5.0V and at room temperature at a clock frequency of 45.0MHz.

Work Around:

None. Operate these devices as close to these conditions as is reasonably possible.

7. Description:

The in-application programming feature is not functional. A design error causes bank 0 to read zeros while bank 1 is being erased or programmed.

Work Around:

None. This condition will be corrected on revision A2 coming shortly.

8. Description:

The in-system programming feature is very frequency dependent. Reduced frequency will yield a high probability of success. Additionally, the feature appears to have some voltage and/or temperature dependencies. No specifics are available at this time.

Work Around:

Perform program and erase functions at lower crystal frequencies for greater success. Repeating the program or erase functions after a complete power down of the part seems to produce better results.

9. Description:

The erase flash command ("K") of the bootstrap loader can only be used once per bootloader session.

Work Around:

Reset the microcontroller before executing another erase flash command.

10. Description:

The erase flash command ("K") of the bootstrap loader may fail to completely erase the flash memory under certain circumstances.

Work Around:

Use the CRC command ("C") after the erase flash command has completed to verify total erasure of the Flash. If completely erased, the CRC command should respond with "CRC = 4400." If the erasure was unsuccessful, reset the microcontroller and repeat the procedure.

11. Description:

To enter loader mode, port pin P3.7 must be pulled high when the pin combination of $RST = 1$, $\overline{PSEN} = 0$, $\overline{EA} = 0$ is applied. When exiting loader mode, port pin P3.7 must be pulled high before the pin combination of $RST = 1$, $\overline{PSEN} = 0$, $\overline{EA} = 0$ is released.

Work Around:

None

12. Description:

The ROM firmware (version 0.9) does not support the 'LB' command nor does it allow the 'R'ead or 'W'rite of the ACON, CKCON, or PMR registers.

Work Around:

None

13. Description:

MOVC instructions executed from internal SRAM (locations 0400h–07FFh), when the internal SRAM is configured as program memory (PRAME = 1), will not execute correctly.

Work Around:

None

14. Description:

In bootstrap ROM loader mode, the ROM code can indicate that the chip is locked when it is not.

Work Around:

Reset the device, press and release the enter key to obtain the “sign-on” banner and then erase the flash (K command). If this does not clear the problem, remove and re-apply power to the device and then perform the steps listed in the preceding sentence. Repeat as needed. This condition will be corrected in the A2 revision.

15. Description:

The device will not fetch from internal flash memory if all three port pins P2.5, P2.6, and P2.7 are held low during a power-on reset.

Work Around:

When internal code fetching is desired ($\overline{EA} = 1$), make certain that at least one of the three pins P2.5, P2.6, or P2.7 is not being held low during a power-on reset.

16. Description:

Any Read-Modify-Write (RMW) instruction that has P0, P1, P2, or P3 as its destination (such as ANL P0, #data) can incorrectly activate the strong internal pullup for two clock cycles. This will only occur if a pin is at a logic 0 state and the result of the RMW instruction writes a logic 1 to the corresponding bit in the port latch, even if the bit was previously 1. If external logic connected to that pin is holding it at a logic 0, the strong internal driver can cause the pin to glitch momentarily to a logic 1. This behavior contradicts the data sheet that indicates that the strong internal pullup should only be activated when a zero-to-one transition is required on a port pin. A complete list of RMW instructions is contained in the *Ultra-High-Speed Flash Microcontroller User's Guide*.

Work Around:

When using a port pin as an input, always make certain that any external device driving a logic 0 can sink sufficient current to keep the pin voltage below +0.8V (V_{IL}) during the temporary activation of the internal pullup (V_{OH2}).

17. Description:

When timer/counter1(2) is configured as a counter that is clocked by an external signal (TMOD.6 = 1 and/or T2CON.1 = 1), the baud rate for the serial ports will be incorrect.

Work Around:

None. Configure timer/counter1(2) as a timer that is clocked by an internal signal (TMOD.6 = 0 and/or T2CON.1 = 0) in order to produce the correct serial port baud rate.

18. Description:

When page mode 1 external memory bus structure has been selected, MOVX operations executed from internal flash memory which access external MOVX memory always generate a page miss memory cycle, regardless of the external MOVX address.

Work Around:

None

19. Description:

The microcontroller may not reset itself following a brownout ($0.4 < V_{CC} < V_{RST}$) if the crystal multiplier mode (CTM = 1) is enabled.

Work Around:

Performing a full power-down ($V_{CC} = 0$) will clear the condition. In default (1 clock per machine cycle) mode, this erratum does not occur and no work around is required.

If the crystal multiplier, in either 2X or 4X mode, is used, the device must be placed into default sysclk/1 mode before Vcc drops below Vrst. This can be done by using the power-fail interrupt as follows:

- 1.) Enable the power-fail interrupt before the crystal multiplier is engaged. Do this by setting the EPFI (WDCON.5) bit anytime before the CTM bit is set.
- 2.) The first instruction at 0033h (the start of the power-fail interrupt service routine) must be ORL PMR, #80h. This deactivates the crystal multiplier and returns the device to default sysclk/1 mode. A user-defined power-fail interrupt service routine, if present, can follow. If no user-defined power-fail interrupt service routine is specified, the next instruction should be an endless loop.

19. LOCK BIT SECURITY LEVELS 1, 2, AND 3 DO NOT FUNCTION PROPERLY**Description:**

Security levels 1, 2, and 3 do not function properly and may not prevent access to internal flash memory if external program memory is used.

Work Around:

Use security level 4 if internal flash memory protection is required.