ERRATA SHEET
71M6531D/71M6531F/71M6532D/71M6532F

Revision A05 Errata

The errata listed below describe situations where 71M6531D/71M6531F/71M6532D/71M6532F revision A05 components perform differently than expected or differently than described in the data sheet. Maxim Integrated Products, Inc., intends to correct these errata when the opportunity to redesign the product presents itself.

This errata sheet only applies to 71M6531D/71M6531F/71M6532D/71M6532F revision A05 components. Revision A05 components are branded on the topside of the package with a six-digit code in the form yywwA05, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively. To obtain an errata sheet on another 71M6531D/71M6531F/71M6532D/71M6532F die revision, visit our website at ***www.maximintegrated.com/errata****.*

1) TIMING RESTRICTIONS EXIST FOR THE SUCCESSFUL WRITE BY THE MPU TO THE RTC REGISTERS

Description:
The MPU can perform a write operation to the time register of the on-chip RTC (*RTC_SEC[5:0]* through *RTC_YR[7:0]*). However, writing to the RTC registers while the *SUBSEC* register has certain critical values can cause the write operation to fail.

Workaround:
RTC time is set by writing to the registers *RTC_SEC[5:0]* through *RTC_YR[7:0]*. Each write operation must be preceded by a write operation to the *WE* register in I/O RAM. The value written to the *WE* register is not relevant. In order to reliably set the registers *RTC_SEC* through the *RTC_YR* , it is important to take into account that the associated write operation must be performed while the *SUBSEC[7:0]* register holds a value ≠ 0x00 and the update operation is loaded before the next 1-second boundary.

SUBSEC[7:0] contains the remaining time, in 1/128 second increments, to the next 1-second boundary. In some data sheets for the 71M653x, the stated value of 1/256s for the *SUBSEC[7:0]* register is not correct.

The suggested methods are the following:

a) RTC Interrupt: This method relies on the one-second interrupt generated by the RTC. The interrupt is generated when the *SUBSEC* register reaches the value of 0x01. Therefore the write operation can be performed before reaching the next 1-second boundary (or *SUBSEC* <63). 63 was chosen because a simple test of bit 6 in *SUBSEC[7:0]* assures that the register value is 63 or less.

b) Polling of the *SUBSEC* register. This method relies on the polling of the *SUBSEC* register. The *RTC_SEC* through *RTC_YR* register are to be updated only under the condition: 63 > *SUBSEC* > 1.

Following are code examples.

Example 1: RTC Interrupt

```
/******************** RTC Interrupt ********************

 NOTE:

1)It is assumed that the SUBSEC is < 63 by the time the ISR is executed
  (500ms).
2)When updating RTC registers, the register writes should be done in the
  order shown below, from lowest significance (seconds) to highest
  significance (year).

*******************************************************/
   Void rtc_isr (void) small reentrant interrupt XFER_RTC_IV
   {
      WE=0, RTC_SEC = second;  // Write to the RTC registers in the
      WE=0, RTC_MIN =  minute; // following order
      WE=0, RTC_HOUR = hour;
      WE=0, RTC_DAY =  day;
      WE=0, RTC_DATE = date;
      WE=0, RTC_MON =  month;
      WE=0, RTC_YEAR = year;
      RTC_CTL = 1;
    }   // clear the SUBSEC to restart the timing.
```

Example 2: SUBSEC Polling

```
   if(SUBSEC > 1 && SUBSEC < 63)
   {
      WE=0, RTC_SEC = second;  // Write to the RTC regs in the
      WE=0, RTC_MIN = minute;  // following order
      WE=0, RTC_HOUR = hour;
      WE=0, RTC_DAY = day;
      WE=0, RTC_DATE = date;
      WE=0, RTC_MON = month;
      WE=0, RTC_YEAR = year;
      RTC_CTL = 1;
   }
```

Refer to ***Application Note 4947: The Real-Time Clocks of the 71M65XX Metering ICs*** for more information about real-time clocks of the 71M65xx metering ICs.

2) SOME 71M653x DEVICES EXHIBIT A TEMPORARY FLICKER IN THE LCD SEGMENTS WHEN TRANSITIONING FROM SLEEP MODE TO BROWNOUT MODE UNDER THE CONTROL OF THE WAKE-UP TIMER

Description:
A small percentage of 71M653x ICs shows an anomaly when transitioning from SLEEP mode to BROWNOUT mode under the control of the wake-up timer: These parts can have unexpected and unwanted voltages on the LCD-related pins which can manifest itself as a temporary flicker of segments occurring for a few milliseconds before the MPU reestablishes proper initialization of the LCD system in BROWNOUT mode.

Transitions from SLEEP mode to BROWNOUT mode under control of the pushbutton (PB) input are not affected.

This anomaly is visual only and does not affect other chip functions. Meters that periodically transition from SLEEP mode to BROWNOUT mode, e.g., to check tamper inputs, and where the LCD is expected to stay blank, may be affected.

When transitioning from SLEEP mode to BROWNOUT mode via the wake-up timer feature, the LCD register reset signal becomes inactive at the same time the power to the registers is being restored. Part to part variation in addition to voltage and temperature can change this relationship. In some cases the reset may become inactive earlier than the supply power, which results in the power coming up too late to preserve reset at the LCD registers. When this happens the starting state of some segments will be indeterminate.

Workaround:
There are two workarounds for the issue:

- Transition from BROWNOUT mode to LCD mode (instead of BROWNOUT mode to SLEEP mode) with the LCDs disabled (*LCD_E* = 0) will maintain the essential settings of the LCD system and avoid flickering of segments when the transition back to BROWNOUT mode occurs. This will result in higher current consumption off the battery due to using LCD mode rather than SLEEP mode.

- A small capacitor from the V3P3D pin to the V2P5 pin will inject enough charge into the yet powered-down circuitry of the LCD system to preserve the reset state until the onboard regulation takes over.

Both workarounds will be discussed below.

<u>LCD MODE</u>:
Battery current is higher in LCD mode than in SLEEP mode. The data sheet specifies the SLEEP mode current as 0.7µA typical. For LCD mode, with the LCD disabled, currents around 9µA were measured. With increased environmental temperature, the current in LCD mode may become higher.

This workaround does not require any hardware changes and may be acceptable in cases where battery current is not much of a concern.

CAPACITOR FROM V3P3D to V2P5:
This workaround might be a good choice where both the V3P3D pin and the V2P5 pin are easily accessible for soldering. A capacitor of nominally 61nF is recommended.

The conditions for the capacitor choice are as follows (see Figure 1-1):

- V2P5, when pulled up by the external capacitor, should be between 1.0V and 1.5V, but never above 2.75V.
- V2P5 is typically bypassed to GND with a 0.1µF capacitor.
- V3P3D can be between 3.0V (minimum voltage to maintain BROWNOUT mode) and 3.6V (maximum specified voltage).
- The internal load on V2P5 is minimal and can be neglected.
- The filter formed by the switch resistance R_S and the external capacitive load (100nF assumed) has a τ of 8µs and can also be ignored for the purpose of this application.

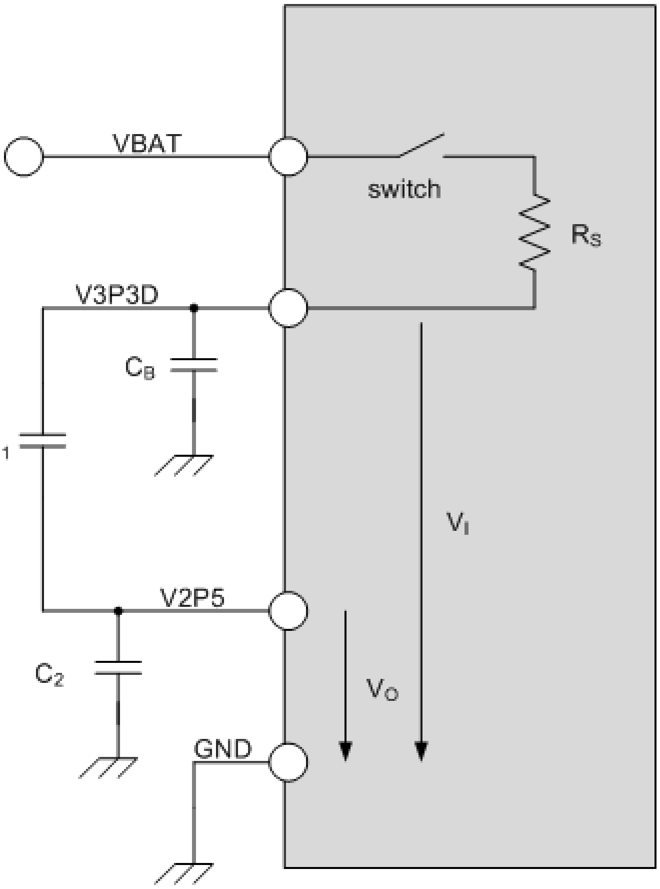

Figure 1-1: 71M653x IC with External Capacitors

The recommended value for the external capacitor C_1 between V3P3D and V2P5 is based on nominal values of VBAT and V2P5, i.e., VBAT = V3P3D is assumed to be in between 3.0V and 3.6V (3.3V) and the target for V2P5 is midway between 1.0V and 1.5V (1.25V). Based on these values, the external capacitor C_1 calculated as follows:

1) C_1 and C_2 form a voltage-divider with the output voltage $V_O = V_I \dfrac{C_1}{C_1 + C_2}$. V_O is the voltage at V2P5, and V_I is VBAT = V3P3D.

2) The nominal value for C_1, i.e., with V3P3D = 3.3V, V2P5 = 1.25V and C_2 = 100nF, is

$$C_1 = \frac{C_2 V_O}{V_I - V_O} = 61nF$$

We now need to consider the cases where C2 is out of tolerance and where VBAT is at the highest and lowest value:

1) The worst case generates the highest voltage at V2P5 and occurs when VBAT = 3.6V and C_2 is at the lowest value (nominal -20%, or 80nF). Then,

$$V_O = V_I \frac{C_1}{C_1 + C_2} = 3.6V \frac{61nF}{61nF + 80nF} = 1.55V$$

2) The other worst case generates the lowest voltage at V2P5 and occurs when VBAT = 3.0V and C_2 is at the highest value (nominal +20%, or 120nF). Then,

$$V_O = V_I \frac{C_1}{C_1 + C_2} = 3.0V \frac{61nF}{61nF + 120nF} = 1.01V$$

The choice of 61nF is acceptable considering deviations for C_2 and VBAT. Since 61nF is not a standard choice for X7R capacitors, C_2 can be increased to 68nF, which increases V2P5 for the minimal case calculated above and increases V2P5 in the maximum worst case to

$$V_O = V_I \frac{C_1}{C_1 + C_2} = 3.6V \frac{68nF}{68nF + 80nF} = 1.65V$$

which is still acceptable.

71M6531D/71M6531F/71M6532D/71M6532F
REV A05 ERRATA

REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/13	Initial release	—