DS3251/DS3252/DS3253/DS3254 Single/Dual/Triple/Quad DS3/E3/STS-1 LIUs

REVISION A2 ERRATA

The errata listed below describe situations where DS3251/DS3252/DS3253/DS3254 revision A2 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS3251/DS3252/DS3253/DS3254 revision A2 components. Revision A1 components are branded on the topside of the package with a six-digit code in the form yywwA2, where yy and ww are two-digit numbers representing the year and workweek of manufacture, respectively. To obtain an errata sheet on another DS3251/DS3252/DS3253/DS3254 die revision, visit our website at **www.maxim-ic.com/errata**.

1. POWER-ON RESET TIMING ISSUE

Description:
If during power-up V_{DD} is ramped too fast or the $\overline{RST}$ pin is asserted at the wrong time, an internal timing problem can cause some LIU ports on some devices to remain stuck in reset. When a port is stuck in reset, the RCLK, RPOS/RDAT, and RNEG/RLCV pins do not toggle, and the TXP/TXN pins either drive no signal or a low-amplitude signal (< 600mV). This condition persists until V_{DD} is ramped down and back up again.

Work Around:
This timing issue can be avoided if two conditions are met:

1) V_{DD} must ramp up with a slew rate of 40µs/V or slower.
2) During power-up, $\overline{RST}$ must not be asserted while V_{DD} < 3.135V.

During power-up, the DS3251/2/3/4 devices are completely reset by their internal power-on reset circuits and do not need to be reset by asserting the $\overline{RST}$ pin. Because $\overline{RST}$ has an internal pullup resistor, one easy way to meet condition 2 above is to leave $\overline{RST}$ floating.