



DS31256 Envoy 256-Channel, High-Throughput HDLC Controller

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REVISION A2 ERRATA

The errata listed below describe situations where DS31256 revision A2 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS31256 revision A2 components. Revision A2 components are branded on the top side of the package with a six-digit code in the form yywwA2, where yy and ww are two-digit numbers representing the year and workweek of manufacture, respectively. To obtain an errata sheet on another DS31256 die revision, visit the website at www.maxim-ic.com/errata.

1. DWORD ALIGNMENT REQUIREMENT

Description:

The DS31256A2 has the following restrictions on the location and size of Tx (transmit) and Rx (receive) buffers in host memory:

- All Tx and Rx buffers must start on DWORD-aligned addresses.
- If a Tx packet is a single buffer packet, then the buffer can be any length from 2 Bytes up to 8191 Bytes.
- If a Tx packet is a multibuffer packet of N buffers in length, then buffers 1 through N - 1 must have a size in bytes that is a multiple of 4. The last buffer can be any size from 1 Byte up to 8191 Bytes.
- Rx buffers must have a size in bytes that is a multiple of 4.
- Rx buffer offsets are no longer supported—Rx DMA configuration RAM dword2[6:3].

The DS3134 does not have these restrictions so this creates a backward compatibility issue. Additionally, **the DS31256B1 will fix the transmit side.**

Work Around:

- Allocate all Rx buffers in memory such that they are DWORD aligned and a size that is a multiple of 4.
- Allocate all Tx buffers in memory such that they are DWORD aligned and a size that is a multiple of 4. Single buffer Tx packets and the last buffer of multibuffer Tx packets do not need to have a size that is a multiple of 4.
- If a Tx packet buffer does not meet the address alignment and size criteria, it must be copied to a new Tx buffer that does.

Implement Rx buffer offsets in software.