



DS26528 T1/E1/J1 Octal Transceiver

www.maxim-ic.com

REVISION A2 ERRATA

The errata listed below describe situations where DS26528 revision A2 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS26528 revision A2 components. Revision A2 components are branded on the top side of the package with a six-digit code in the form yywwA2, where yy and ww are two-digit numbers representing the year and workweek of manufacture, respectively. To obtain an errata sheet on another DS26528 die revision, visit our website at www.maxim-ic.com/errata.

1. SHORT-CIRCUIT PROTECTION MAY NOT ACTIVATE WHEN THE PART IS IN CERTAIN T1/J1 OR E1 OPERATING MODES WITH IMPEDANCE MATCH ON

Description:

When the part is operating in T1/J1 LBO 1, 2, 5, 6 and 7 modes or E1 LBO 1 (120 Ω) mode and impedance match is on, it is possible that the short-circuit protection may not activate. This issue only affects these particular line build-outs with impedance matching on.

Work Around:

None.

2. OPEN-CIRCUIT DETECTION MAY NOT FUNCTION PROPERLY WHEN THE PART IS IN CERTAIN T1/J1 OR E1 OPERATING MODES WITH IMPEDANCE MATCH ON

Description:

When the part is operating with impedance match on in T1/J1 LBO 0 and 1 modes or E1 LBO 0 (75 Ω) mode or E1 LBO 1 (120 Ω) mode, the open-circuit detect function will indicate an open circuit in the LRSR.OCS register bit even when a correct load is present. Additionally, T1/J1 LBOs 2, 3, 4, and 5 are marginally affected, meaning the open-circuit detection circuitry may indicate an open circuit in these modes even under correct loading. This issue is only related to the status bit that indicates an open-circuit; the functionality of the line-driver is unaffected. This problem only occurs with impedance matching on.

Work Around:

None

3. FAILURE TO DETECT J1 LFA (YELLOW ALARM) IN ESF MODE

Description:

The DS21458/455 does not identify the J1 LFA (also called Yellow or RAI) alarms correctly. In J1 ESF mode, the DS21458/455 will not report the LFA alarm when the Japanese JT-G704 LFA pattern of '11111111 11111111' is present in the facilities data link. The DS21458/455 will only respond to the normal G.704 LFA pattern of '11111111 00000000'.

Work Around:

To transmit the Japanese ESF LFA alarm, which is 0xFFFF in the FDL, the following can be done. Set the TFDL register to 0xFF and set the TFDLS bit to a 0. The TFDLS bit is located in the T1TCR1 register.

To receive the Japanese ESF LFA alarm, which is 0xFFFF, the software must monitor the RFDL register. The RFDL register is updated regularly and an update is indicated by the RFDLF status bit. The RFDLF status bit is located in the SR8 register. Since the Japanese ESF LFA alarm pattern is 2 bytes long, the RFDL register has to be read on two consecutive updates for a complete pattern. When 16 consecutive patterns of 0xFFFF appear in the FDL, the alarm will be set. If 14 or fewer patterns of 0xFFFF out of 16 possible appear in the FDL, the alarm will be cleared.

4. PROGRAMMABLE CHANNEL BLANKING MAY LEAD TO DROPPED DATA UNDER CERTAIN IBO OPERATING MODES

Description:

When the part is programmed for channel blanking with channel 1 and channel 2 blanked at the same time data can be dropped if T1 rate data is being mapped onto an E1 rate backplane in byte-interleaved IBO mode.

Work Around:

None.

5. ERROR COUNT REGISTERS COULD ROLL OVER AT 0xFFFFh IN MANUAL UPDATE MODE

Description:

The error count registers can roll over after the counters have saturated in manual update mode (ERCNT.MCUS = 0). This roll over will not occur when the error count registers are not set to be updated manually, they will saturate as stated in the datasheet.

Work Around:

Ensure that the manual error counter update bit is set (ERCNT.MECU = 1) before the registers are allowed to saturate.

6. THE RIM7 (E1 MODE) REGISTER IS NOT ACCESSIBLE

Description:

The RIM7 register (at address 0A6h + (200h x n), where n = 0 to 7 for Ports 1 to 8) is not accessible in E1 Mode. This register indicates changes in state of the Sa bits.

Work Around:

Use the other Sa Bit Access registers to determine a change of state of the Sa bits. The Sa bits can be accessed through either the E1RAF/E1RNAF and E1TAF/E1TNAF registers or the E1RSa4 to E1RSA8 and E1TSa4 to E1TSA8 registers. These registers are covered in detail in the DS26528 datasheet.

7. THE E1RSAIMR REGISTER IS NOT ACCESSIBLE**Description:**

The E1RSAIMR register (at address $014h + (200h \times n)$, where $n = 0$ to 7 for Ports 1 to 8) is not accessible. This register is used to select which Sa bits can cause a change of state interrupt in the RLS7 register.

Work Around:

None.

8. THE RLS7 (E1 MODE) REGISTER IS NOT ACCESSIBLE**Description:**

The RLS7 register (at address $096h + (200h \times n)$, where $n = 0$ to 7 for Ports 1 to 8) is not accessible in E1 mode. This register is used to interrupt when bit changes are observed in selected Sa bit positions.

Work Around:

None.

9. THE SaBITS REGISTER IS NOT ACCESSIBLE**Description:**

The SaBITS register (at address $06Eh + (200h \times n)$, where $n = 0$ to 7 for Ports 1 to 8) is not accessible. This register is used to display the last received Sa bits.

Work Around:

Use the other Sa Bit Access registers to determine the status of the Sa bits. The Sa bits can be accessed through either the E1RAF/E1RNAF and E1TAF/E1TNAF registers or the E1RSa4 to E1RSa8 and E1TSa4 to E1TSa8 registers. These registers are covered in detail in the DS26528 datasheet.

10. THE Sa6CODE REGISTER IS NOT ACCESSIBLE**Description:**

The Sa6CODE register (at address $06Fh + (200h \times n)$, where $n = 0$ to 7 for Ports 1 to 8) is not accessible. This register is used to display the last received Sa6 Codeword as defined by ETS 300233.

Work Around:

Use the other Sa Bit Access registers to determine status of the Sa6 bits. The Sa6 bits can be accessed through either the E1RAF/E1RNAF and E1TAF/E1TNAF registers or the E1RSa4 to E1RSa8 and E1TSa4 to E1TSa8 registers. These registers are covered in detail in the DS26528 datasheet.

11. THE RSYNC PIN DIRECTION DEFAULT VALUE IS INCORRECT**Description:**

The direction of RSYNC at power up or reset is incorrect. The RSYNC pin defaults to an output. The default direction of the RSYNC pin at power up or reset should be as an input as stated in the datasheet. The default direction is set by RIOCR.RSIO bit, which should default to a 1 but incorrectly defaults to a 0 in this revision.

Work Around:

Set the RIOCR.RSIO bit to a 1 after power-up or reset to configure the RSYNC pin as an input.

12. THE T1 AIS (BLUE ALARM) SET AND CLEAR CRITERIA ARE INCORRECT**Description:**

The T1 AIS (Blue Alarm) set and clear criteria are incorrect. The AIS alarm will be set when, over a 3 ms window, 5 or less zeros are received. The AIS alarm will be cleared when, over a 3ms window, 6 or more zeros are received. This alarm should be set when 4 or less zeros are received and cleared when 5 or more zeros are received.

Work Around:

None.

13. TRANSMIT TERMINATING IMPEDANCE MATCH, WHEN ENABLED, MAY RESULT IN TRANSMIT WAVEFORMS THAT FAIL OR ARE NOT CENTERED IN THEIR RESPECTIVE TEMPLATES**Description:**

If enabled via the LIU Transmit Impedance and Pulse Shape Selection Register (LTITSR.6 = 0), the Transmit Terminating Impedance Match feature may result in transmit waveforms that are not centered in their respective templates or fail template completely.

Work Around:

The transmit waveforms can be modified by setting several registers in the part in order to better center the waveforms and remove any template violations. These registers are located at the addresses shown in the table below. Please contact the Telecom Support Group at telecom.support@dalsemi.com for detailed information regarding these errata and the appropriate values with which these registers should be programmed.

PORT #	TXLAA	TXLAB	TXLAC	TXLAD	TXLAE	LTITSR
LIU 1	1008	1009	100A	100B	100C	1001
LIU 2	1028	1029	102A	102B	102C	1021
LIU 3	1048	1049	104A	104B	104C	1041
LIU 4	1068	1069	106A	106B	106C	1061
LIU 5	1088	1089	108A	108B	108C	1081
LIU 6	10A8	10A9	10AA	10AB	10AC	10A1
LIU 7	10C8	10C9	10CA	10CB	10CC	10C1
LIU 8	10E8	10E9	10EA	10EB	10EC	10E1