ERRATA SHEET
DS26324

Revision A1 Errata

The errata listed below describe situations where DS26324 revision A1 components perform differently than expected or differently than described in the data sheet. Maxim Integrated Products, Inc., intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS26324 revision A1 components. Revision A1 components are branded on the topside of the package with a six-digit code in the form yywwA1, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively. To obtain an errata sheet on another DS26324 die revision, visit our website at www.maxim-ic.com/errata.

NOTE: THE FOLLOWING ARE FEATURE ENHANCEMENTS IMPLEMENTED IN REVISION A2 THAT WILL NOT WORK FOR REVISION A1:

1) Programmable corner frequency for the jitter attenuator in E1 mode.
2) Fully internal impedance matching option for RTIP/RRING.
3) Option for system-side deployment of BERT.
4) RESREF pin for receive termination calibration.

1) SHORT-CIRCUIT AND OPEN-CIRCUIT DETECTION DO NOT OPERATE RELIABLY

Description:
When the part is operating in either T1/J1 or E1 mode and impedance matching is on, short-circuit detection and open-circuit detection do not operate reliably. This issue affects all line build-outs with impedance matching on.

Workaround:
None.

2) RPOS, RNEG, AND RCLK PINS DO NOT TRI-STATE

Description:
The RPOS, RNEG, and RCLK pins for all the 16 LIUs do not tri-state as specified in the data sheet.

Workaround:
None.
3) TEMPLATE COMPLIANCE OF OUTPUT WAVEFORMS

Description:
Output waveforms may not be centered in their respective templates leading to possible template violations or less than ideal template compliance.

Workaround:
Table 1 below specifies the address to the ADDP registers and the addresses of the registers within the test bank that needs to be set in order to center the output waveform within the template. The setting depends on whether impedance matching is on or off. Impedance matching can be set or unset using the TIMPOFF bit in Template Select Register (Register Address = 11h).

With impedance matching on, short circuit protection should be disabled to avoid a false detection and thereby shutting down of the device (see Errata #1 on short-circuit and open-circuit detection).

<table>
<thead>
<tr>
<th>ADDRESS TO THE ADDP REGISTER</th>
<th>HEX VALUE TO ENTER IN ADDRESS</th>
<th>WILL ACCESS THE FOLLOWING LIU</th>
<th>WRITE TO THE FOLLOWING ADDRESS WITHIN THE TEST BANK</th>
<th>HEX VALUE TO WRITE IN ADDRESS WITH IMPEDANCE MATCHING:</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>OFF (TIMPOFF BIT = 1)</td>
</tr>
<tr>
<td>1Fh</td>
<td>04h</td>
<td>LIU1</td>
<td>04h</td>
<td>Contact factory for register settings</td>
</tr>
<tr>
<td>1Fh</td>
<td>05h</td>
<td>LIU2</td>
<td>04h</td>
<td></td>
</tr>
<tr>
<td>1Fh</td>
<td>06h</td>
<td>LIU3</td>
<td>04h</td>
<td></td>
</tr>
<tr>
<td>1Fh</td>
<td>07h</td>
<td>LIU4</td>
<td>04h</td>
<td></td>
</tr>
<tr>
<td>1Fh</td>
<td>08h</td>
<td>LIU5</td>
<td>04h</td>
<td></td>
</tr>
<tr>
<td>1Fh</td>
<td>09h</td>
<td>LIU6</td>
<td>04h</td>
<td></td>
</tr>
<tr>
<td>1Fh</td>
<td>0Ah</td>
<td>LIU7</td>
<td>04h</td>
<td></td>
</tr>
<tr>
<td>1Fh</td>
<td>0Bh</td>
<td>LIU8</td>
<td>04h</td>
<td></td>
</tr>
<tr>
<td>3Fh</td>
<td>04h</td>
<td>LIU9</td>
<td>24h</td>
<td>Contact factory for register settings</td>
</tr>
<tr>
<td>3Fh</td>
<td>05h</td>
<td>LIU10</td>
<td>24h</td>
<td></td>
</tr>
<tr>
<td>3Fh</td>
<td>06h</td>
<td>LIU11</td>
<td>24h</td>
<td></td>
</tr>
<tr>
<td>3Fh</td>
<td>07h</td>
<td>LIU12</td>
<td>24h</td>
<td></td>
</tr>
<tr>
<td>3Fh</td>
<td>08h</td>
<td>LIU13</td>
<td>24h</td>
<td></td>
</tr>
<tr>
<td>3Fh</td>
<td>09h</td>
<td>LIU14</td>
<td>24h</td>
<td></td>
</tr>
<tr>
<td>3Fh</td>
<td>0Ah</td>
<td>LIU15</td>
<td>24h</td>
<td></td>
</tr>
<tr>
<td>3Fh</td>
<td>0Bh</td>
<td>LIU16</td>
<td>24h</td>
<td></td>
</tr>
</tbody>
</table>
4) **ALL-ONES INSERTION IN DIGITAL LOOPBACK**

**Description:**
The transmit all-ones logic is inside the digital loopback path. The data looped back to RPOS/RNEG will be overwritten by any transmit all-ones condition.

**Workaround:**
TPOS/TNEG can be looped back to RPOS/RNEG while simultaneously sending all ones on TTIP/TRING. However all-ones will be sent on groups of 1–8 and 9–16 TTIP/TRING outputs. Use the settings in Table 2 to enable this feature. Use these settings instead of the TAOE register.

<table>
<thead>
<tr>
<th>ADDRESS TO THE ADDP REGISTER</th>
<th>HEX VALUE TO ENTER IN ADDRESS</th>
<th>WILL ACCESS THE FOLLOWING LIUs</th>
<th>WRITE TO THE FOLLOWING ADDRESS WITHIN THE TEST BANK</th>
<th>HEX VALUE TO WRITE IN ADDRESS TO TRANSMIT ALL ONES IN DIGITAL LOOPBACK</th>
</tr>
</thead>
<tbody>
<tr>
<td>1Fh</td>
<td>03h</td>
<td>LIU 1–8</td>
<td>07h</td>
<td>07h</td>
</tr>
<tr>
<td>3Fh</td>
<td>03h</td>
<td>LIU 9–16</td>
<td>27h</td>
<td>07h</td>
</tr>
</tbody>
</table>

5) **OUTPUT ENABLE (OEn) BIT**

**Description:**
OEn bit in the output-enable register (register address for LIUs 1–8: 12h and for LIUs 9–16: 32h) is inverted. When OEn bit is high, the transmitter is disabled. When it is low, the transmitter is enabled.

**Workaround:**
None.

6) **RECEIVE IMPEDANCE ON (RIMPON) BIT**

**Description:**
When RIMPON bit (in register TS) is set to 0, receive impedance matching is ON. When RIMPON bit is set to 1, receiver is in high impedance. In default mode, RIMPON = 0 and receive impedance matching is ON.

**Workaround:**
None.

7) **RECEIVE TERMINATION CONTROL (RTCTL) BIT**

**Description:**
RTCTL bit (in GC register) does not work.

**Work Around:**
None.