



DS21552/DS21Q552 5V Enhanced T1 Single-Chip Transceivers

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REVISION A4 ERRATA

The errata listed below describe situations where DS21552/DS21Q552 revision A4 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS21552/DS21Q552 revision A4 components. Revision A4 components are branded on the top side of the package with a six-digit code in the form yywwA4, where yy and ww are two-digit numbers representing the year and workweek of manufacture, respectively. To obtain an errata sheet on another DS21552/DS21Q552 die revision, visit our website at www.maxim-ic.com/errata.

1. TRANSMIT- AND RECEIVE-SIGNALING BUFFERS DO NOT OPERATE CORRECTLY IF INTERLEAVED BUS OPERATION (IBO) IS ENABLED.

Description:

If interleaved bus operation is enabled, hardware signaling using the TSIG and RSIG pins is not available. The receive-signaling change (RSC) interrupt does not operate and signaling reinsertion in the receive path is nonfunctional.

Other functionality associated with interleaved bus operation is still available. The device correctly interleaves the serial data streams at RSER. Signaling is available in the receive-signaling registers.

Work Around:

Changes in signaling states can still be identified in software by reading the receive-signaling registers each multiframe and comparing the contents with the previous multiframe of signaling.

2. FRAME-INTERLEAVED MODE OF INTERLEAVED BUS OPERATION (IBO) DOES NOT WORK.

Description:

The DS21552 contains on-chip control logic to allow the combining of the individual framer's PCM buses—RSER and TSER—into higher-speed serial buses, simplifying transport across the system. An error in the control logic prevents the frame interleave option from working correctly. The channel-interleave option for RSER and TSER works correctly.

Work Around:

None.

3. PROPAGATION DELAYS EXCEED DATA SHEET LIMITS.**Description:**

The propagation delays— T_{D1} , T_{D2} , T_{D3} , and T_{D4} —exceed the limits set forth in the data sheet for the 5V operation. The data sheet specifies 50ns max. T_{D1} and T_{D2} can be as long as 65ns. T_{D3} and T_{D4} are typically 60ns to 90ns.

In applications using the elastic store buffers and an 8.192MHz backplane clock, the RSER output is delayed such that the output could transition during the falling edge of the clock. This could result in other devices on the backplane latching the bit during the transition of the output driver.

Work Around:

It is recommended that the 8.192MHz clock applied to the RSYCLK input pin be inverted. This moves the data one half-clock cycle so the data bits can be latched by other devices on the falling edge of the noninverted clock. Operation at slower backplane clock speeds is unaffected.

4. PAYLOAD LOOPBACK**Description:**

If the transmit elastic store minimum-delay mode is enabled and payload loopback is selected, the outbound signal will contain bit errors and CRC errors.

Work Around:

When using payload loopback, the transmit elastic store minimum-delay mode must be disabled. If CCR1.1 (payload loopback) is set, CCR3.7 (transmit elastic store minimum delay) must be cleared.

5. RECEIVE LEVEL-INDICATOR BITS MAY NOT MATCH SIGNAL INPUT LEVEL.**Description:**

The receive level-indicator bits (RIR3.6, RIR3.7) may not reflect the actual received signal strength.

Work Around:

None.

6. SLC-96 MESS5 MESSAGE CORRUPTION IN T1 D4 FRAMING.**Description:**

When the DS21552 tries to process the following SLC-96 message, the information reported becomes corrupted. The MESS5 message is covered in BellCore TR-TSY-000008 (page 4-5) and Telcordia GR-8 (page 4-7). This message is sent from the RT to the COT every 1.15 seconds.

The first six bits of this message are '000111,' an exact match for the SLC-96 synchronization bits, which are '000111000111.' A normal SLC-96 data stream in the Fs bits of D4 framing would be formatted as follows:

```
'000111000111cccccccc010mmaasss1'
```

With the MESS5 message, the stream becomes:

```
'0001110001110001111111010mmaasss1'
```

The 'c' bits at the start of the message look exactly like the synchronization part of the message. The end result is that the SLC-96 message is reported incorrectly by the DS21552.

Work Around:

None.

7. FAILURE TO DETECT J1 LFA (YELLOW ALARM) IN ESF MODE.**Description:**

The DS21552 does not correctly identify the J1 LFA (also called Yellow or RAI) alarms correctly. In J1 ESF mode, the DS21552 does not report the LFA alarm when the Japanese JT-G704 LFA pattern of '11111111 11111111' is present in the facilities data link. The DS21552 only responds to the normal G.704 LFA pattern of '11111111 00000000.'

Work Around:

To transmit the Japanese ESF LFA alarm, which is 0xFFFF in the FDL, the following can be done. Set the TFDL register to 0xFF and set the TFDLS bit to 0. The TFDLS bit is located in the TCR1 register.

To receive the Japanese ESF LFA alarm, which is 0xFFFF, the software must monitor the RFDL register. The RFDL register is updated regularly. The RFDLF status bit indicates an update. The RFDL status bit is located in the SR2 register. Since the Japanese ESF LFA alarm pattern is two bytes long, the RFDL register has to be read on two consecutive updates for a complete pattern. When 16 consecutive patterns of 0xFFFF appear in the FDL, the alarm is set. If 14 or fewer patterns of 0xFFFF out of 16 possible appear in the FDL, the alarm is cleared.

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