

INTRODUCTION

Telecom application notes can be found in the numerical listing. This index is updated periodically to show by category what is in the numerical listing. There may be application notes in the numerical listing that are not yet referenced by this index.

BERT COMPONENTS/RELATED APPLICATION NOTES													
DS2172/DS21372 BIT ERROR-RATE TESTER													
331	332	333	334	375									
T1 COMPONENTS/RELATED APP NOTES													
DS2141A T1 CONTROLLER													
301	302	306	308	309	310	313	314	315	320	326	328	335	336
338	339	342	345										
DS21Q41 QUAD T1 CONTROLLER													
301	302	309	310	320	336	342							
DS2151 T1 SINGLE-CHIP TRANSCEIVER													
301	303	304	305	307	308	309	310	314	311	312	313	315	316
317	318	323	324	325	326	329	336	337	345	347	349	351	354
370	2713												
DS2152 ENHANCED T1 SINGLE-CHIP TRANSCEIVER													
301	307	309	310	312	317	319	321	323	324	325	336	335	337
342	345	346	349	350	351	353	354	355	360	370	382	2713	
DS21x52 3.3/5V T1 SINGLE-CHIP TRANSCEIVER													
307	309	310	321	323	324	325	335	336	337	342	345	350	351
355	359	360	370	373	374	379	381	382	388	391	394	2713	
DS21Q42 ENHANCED QUAD T1 FRAMER													
309	310	321	335	336	342	345	355	357	373	385	394	2713	

T1/E1 COMPONENTS/RELATED APP NOTES													
DS2148/Q48, DS2149/349, DS21348/Q348/448 T1/J1 SINGLE-CHIP/QUAD LINE INTERFACE UNITS													
324	351	370	382	384	387	388	402	405	407	2706	2713		
DS21x5y, DS21x5y 3.3/5V T1/E1 TRANSCEIVER													
309	310	335	336	345	350	351	361	373	374	382	391	393	394
2713													
DS21Qx5y, DS21Qx5y QUAD 3.3/5V T1/E1 TRANSCEIVER													
309	310	335	336	345	350	351	361	373	374	382	391	393	394
2713													
DS2155, DS21Q55 SINGLE-CHIP/QUAD T1/E1/J1 TRANSCEIVER													
307	324	325	336	337	345	351	370	374	381	382	384	388	389
390	391	393	394	396	397	400	401	2713	2731				
DS2156 T1/E1/J1 SINGLE-CHIP TRANSCEIVER TDM/UTOPIA II INTERFACE													
324	335	381	384	389	391	393	394	2713	2722	2731			
DS3134, DS31256 CHANNELIZED T1/J1 AND UNIVERSAL HDLC CONTROLLER													
356	358	363	364	365	366	368	369	371	372	380	390	392	399
2351													

E1 COMPONENTS/RELATED APP NOTES													
DS2143 E1 CONTROLLER													
301	302	306	308	309	313	314	315	320	326	336	370		
DS21Q43 QUAD E1 CONTROLLER													
301	302	309	320	336	342	356							
DS2153 E1 SINGLE-CHIP TRANSCEIVER													
301	303	304	305	307	308	309	311	312	313	314	315	316	
	317												
318	322	323	324	325	326	327	330	336	340	341	342	347	
	348												
351	352	370											
DS2154 ENHANCED E1 SINGLE-CHIP TRANSCEIVER													
301	307	309	312	317	319	321	322	323	324	325	336	342	
	346												
348	350	351	352	354	355	361	370	393					
DS21x54 3.3/5V E1 SINGLE-CHIP TRANSCEIVER													
307	309	321	322	323	324	325	336	342	350	351	355	359	
	361												
370	373	374	379	381	384	388	391	393	394				
DS21Q44 ENHANCED QUAD E1 FRAMER													
309	321	336	342	355	356	370	373	393	394				

T3/E3 COMPONENTS/RELATED APP NOTES

DS3150, DS315X T1/J1 SINGLE/DUAL/TRIPLE/QUAD DS3/E3/STS-1 LINE INTERFACE UNITS

362 380 397 398 404 2696

DEVICE HISTORY

Highlights the hardware and software differences between the various generation devices.

348	▪ DS2154L vs. DS2153Q
349	▪ DS2152L vs. DS2151Q
350	▪ Provision Your DS2152 or DS2154 Design for the Next Generation Devices
356	▪ DS21Q44 vs. DS21Q43
357	▪ DS21Q42 vs. DS21Q41
360	▪ DS21x52 vs. DS2152
361	▪ DS21x54 vs. DS2154
403	▪ DS2155 and DS26401 Software Comparison
2351	▪ DS31256 and DS3134 HDLC Controller Comparison

DEVICE OPERATION

Detailed information into device operation.

352	▪ General Network Interface Design Criteria for the DS2153 and DS2154
353	▪ General Network Interface Design Criteria for the DS2151 and DS2152
354	▪ Clock Map of DS2152 and DS2154

PCM INTERFACE

301	▪ 8MHz System Clock Operation
302	▪ 8MHz System Clock Operation
303	▪ Interfacing to the ADSP-2181
304	▪ Interfacing to the AT&T T7270
305	▪ Interfacing to the Bt8221, Bt8222
306	▪ 3-Channel Drop/Insert
307	▪ 3-Channel Drop/Insert
308	▪ Interfacing to the SGS Thomson M3488
309	▪ Fractional T1 and E1
310	▪ D4 Framing and Signaling
311	▪ Interfacing to the Hitachi HD64570
312	▪ Interfacing to the Siemens PEB20320
313	▪ Interfacing to the Mitel MT8980D

PCM INTERFACE	
314	▪ Per-Channel Loopback
315	▪ Interfacing to the Siemens PEB2045
316	▪ Interfacing to the PMC-Sierra PM7345
317	▪ Interfacing to the Siemens PXB4220
318	▪ Interfacing to the MC68MH360
319	▪ Interfacing to the MC68MH360
320	▪ Interfacing to the MC68MH360
321	▪ Interfacing to the IGT WAC-0210C
359	▪ Interfacing to the TI DSP TMS320540X Family

NETWORK INTERFACE	
322	▪ Selectable 120Ω and 75Ω Interface
323	▪ Line Monitor
324	▪ Secondary Overvoltage Protection

COMPONENT SELECTION	
325	▪ Crystal Selection
351	▪ Transformer Selection

CONTROLLER	
326	▪ Interfacing to a Nonmux Bus
358	▪ PCI Bus Utilization

CSU	
327	▪ Creating a T1/E1 Channel Service Unit
328	▪ Creating a D4/ESF Channel Service Unit

PROGRAMMING	
335	▪ Controlling the FDL
336	▪ Transparent Operation
337	▪ ANSI T1.231-1993 Implementation
338	▪ Alarm Set and Clear Criteria
339	▪ D4 Framing Applications

PROGRAMMING

340	▪ ETS 300 011 Alarm Generation
341	▪ Device Identification
342	▪ Initialization and Programming
345	▪ SLC-96 Operation
2731	▪ DS2155, DS21Q55, DS2156 Programming SLC-96

DESIGN KITS

The demo kits can be easily converted between T1 and E1 operation.

346	▪ Converting the DS2152/DS2154 Demo Kits
347	▪ Converting the DS2151/DS2153 Demo Kits

SPECIAL MODES AND TEST REGISTERS

Device features not covered in the data sheets.

329	▪ DS2151 Special Modes
330	▪ DS2153 Special Modes
355	▪ Test Registers

BIT ERROR-RATE TESTER

331	▪ V.54 Modem Test Patterns
332	▪ Simplified Receiver Operation
333	▪ Repetitive Pattern Operation
334	▪ Interfacing to T1 and E1 Framers
389	▪ DS2155 Internal BERT Programming

LAYOUT AND DESIGN

324	▪ T1/E1 Network Interface Design
350	▪ Provision Your DS2152 or DS2154 Hardware Design for the Next Generation Devices
376	▪ Simple, Low-Cost, 4-Port E1 Design Using DS21Q50
384	▪ T1/E1/J1 Dual Connector Interface
398	▪ T3/E3/STS-1 LIU Secondary Surge Protection Design
400	▪ DS2155 Monitor Mode Design
401	▪ Extended System Information Bus (ESIB) Control Application
402	▪ Additional Pulse Amplitude Settings for DS2148, DS21348, DS21Q48, DS21Q348 and DS21448
404	▪ Modifying the Pulse Shape of the DS3150 and DS315x

LAYOUT AND DESIGN	
405	▪ Power-Fault Protection Layout
2696	▪ Redundancy Protection for T3/E3/STS-1 Networks

JTAG BOUNDARY SCAN	
406	▪ DS21Qx5y BSDL Scan Chain Mapping