Application Note 243
Increasing DS276X ESD Protection Levels

Introduction
The standard application circuits shown in the DS276X datasheets are designed to allow the DS276X to SURVIVE IEC1000-4-2 testing specifications of 8k contact and 15k air (at 330Ω, 150pF). For applications where the DS276X is required not only to survive but also continue to operate during an ESD event, additional external protection components are recommended. Board layout becomes very critical as well.

Solution Circuit
Typically the pack's exposed contacts are susceptible to ESD events. The AC component of this ESD energy will normally leave the pack through its largest surface area: the battery. This energy will have to pass through the IC during this process, causing it to possibly reset. The addition of external components to allow the energy to flow around the IC instead of through it improves operation during ESD events.

Figure 1. Maximum ESD protection Circuit

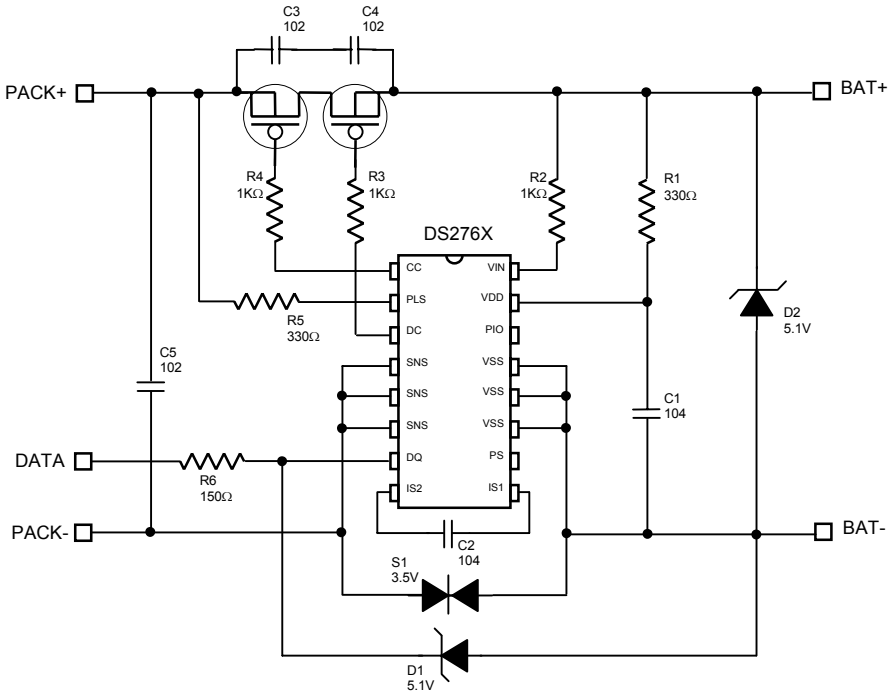


Figure 1 shows the recommended ESD protection circuit. This circuit is the recommended datasheet circuit with the additions of S1, D1, and D2. The VDD and PLS resistor values have also been increased. Components S1, D1, and D2 allow ESD strikes on the external pins (PACK+, PACK-, and DQ) to flow to the pack ESD exit point, the battery case (BAT+ or BAT- in Figure 1), without passing through the DS276X device.

Circuit Layout

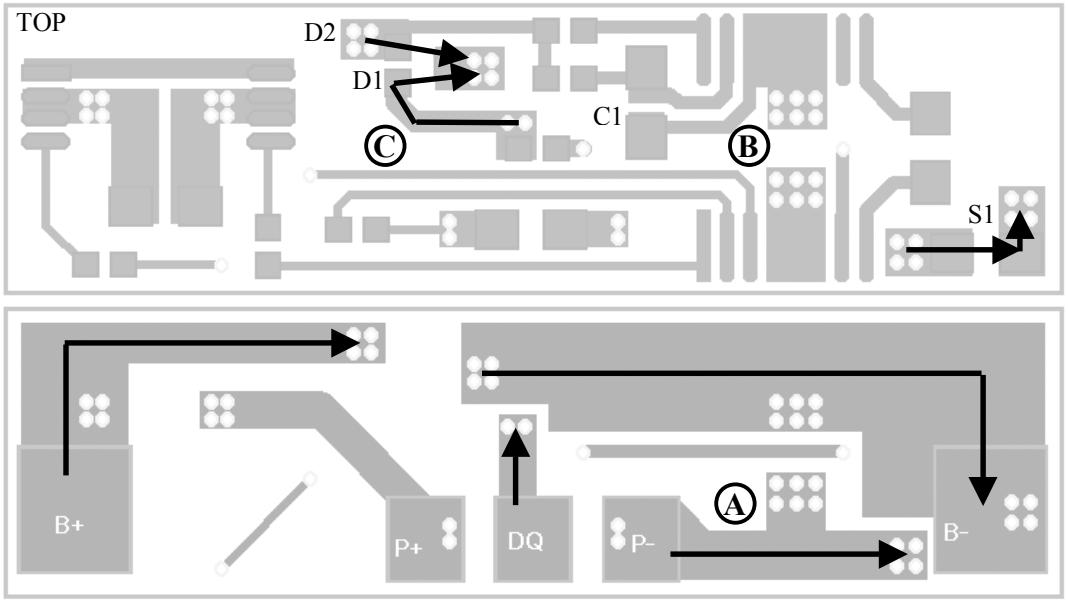
The layout of the DS276X protection circuit is just as important as the additional components themselves. Board inductance should be minimized so that ESD energy will flow through the external protection paths and not through the chip. Figure 2 shows a two level board layout of the circuit in Figure 1 using a DS276X with internal sense resistor in a TSSOP package. The black arrows show the path that ESD current will take through the protection components D1, D2, and S1. Important design considerations are described below:

(A) The path from PACK- to BAT- through S1 should be as low inductance as possible. The path should be straight and wide and limit the effects of via resistance.

(B) Positioning of the VDD capacitor C1 is extremely important. The trace lengths from V_{DD} and GND to C1 should be as short as possible and not run through any vias. The gap between the two traces should also be kept to a minimum to limit inductance.

(C) The paths for D1 and D2 should follow the same layout rules as for S1: large low inductance traces. These paths are not as critical and the layout of (A) and (B) above should not be compromised for these traces.

Figure 2. Board Layout



Summary

The DS276X's ability to function during ESD events can be increased with proper design of the external protection circuit. Components can be added externally to allow ESD energy to flow around the IC, not through it. Minimized inductance in the circuit encourages ESD energy to take these alternate paths.