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TUTORIAL 5693

DC ERROR CHARACTERISTICS OF AN OP AMP AND THE EFFECT ON HIGH-PRECISION APPLICATIONS

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Abstract: This article discusses the DC limitations of operational amplifiers and their effects, including input bias currents, input offset voltage, CMRR, PSRR, and input impedance. The article will provide the reader with a better understanding of how these limitations can create accuracy issues in high-precision applications.

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Introduction

Operational amplifiers, or op amps, are two-port integrated circuits (ICs) that apply precise gain on the external input signal and provide an amplified output as: input × closed-loop gain. Precision op amps behave close to ideal when operated at low to moderate frequencies and moderate DC gains. However, even under these conditions, op-amp performance is influenced by other factors that can impact accuracy and limit performance. Most common among these limitations are input referred errors that predominate in high-DC gain applications.

In this article we discuss the effects of input referred errors on op amps. These errors include input bias current, input offset current, input offset voltage, CMRR, PSRR, and finite input impedance. In reality, all these errors will occur at the same time. We also explain why a designer should be wary that the op-amp performance specifications described in the EC Table of a data sheet are only guaranteed for the conditions defined at the top of that table, unless otherwise noted as a specific characteristic. In reality, the effects of these DC errors change when the supply voltage, common-mode voltage range, and other conditions change.

Errors Caused by Input Bias and Input Offset Currents

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We are all familiar with potential dangers around us, and we engineers tend to forget that there are also dangerous traps to avoid when designing. Let’s see how this affects op amps (**Figure 1A** and **1B**).

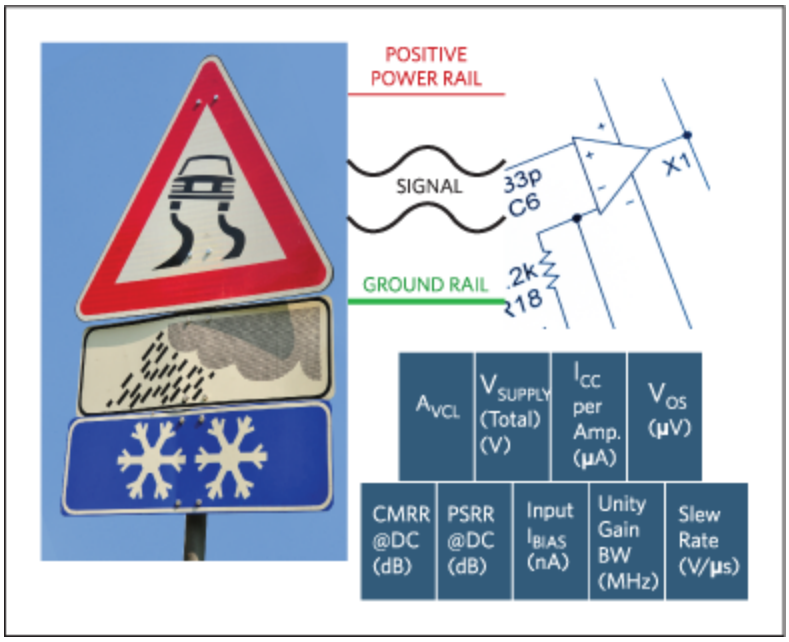

Figure 1A. A roadside danger sign, warning of an automotive skid hazard under certain conditions (rain and snow); Figure 1B on the right is an op-amp "alert sign," constructed from data sheet parameters and the specifications, warning that the signal must be contained between the power and ground rails.

We start with two basic equations:

$I_B = (I_{BP} + I_{BN})/2$ ….. (Eq. 1)
$I_{OS} = I_{BP} - I_{BN}$ ….. (Eq. 2)

where:
I_B is average input bias current flowing into input pins;
I_{BP} is input bias current flowing into the positive input;
I_{BN} is input bias current flowing into the negative input;
I_{OS} is the input offset current.

Input bias and input offset currents are two of the most critical characteristics in many precision amplifier applications; they affect the output with resistive and capacitive feedback. Many of the inverting, noninverting, summing, and differential amplifiers reduce to **Figures 2A** and **2B** once their active inputs are set to zero. For this analysis, we set all input signals as zero to assess the effect of input currents on the output accuracy. We will analyze resistive feedback (Figure 2A) and capacitive feedback (Figure 2B) circuits separately.

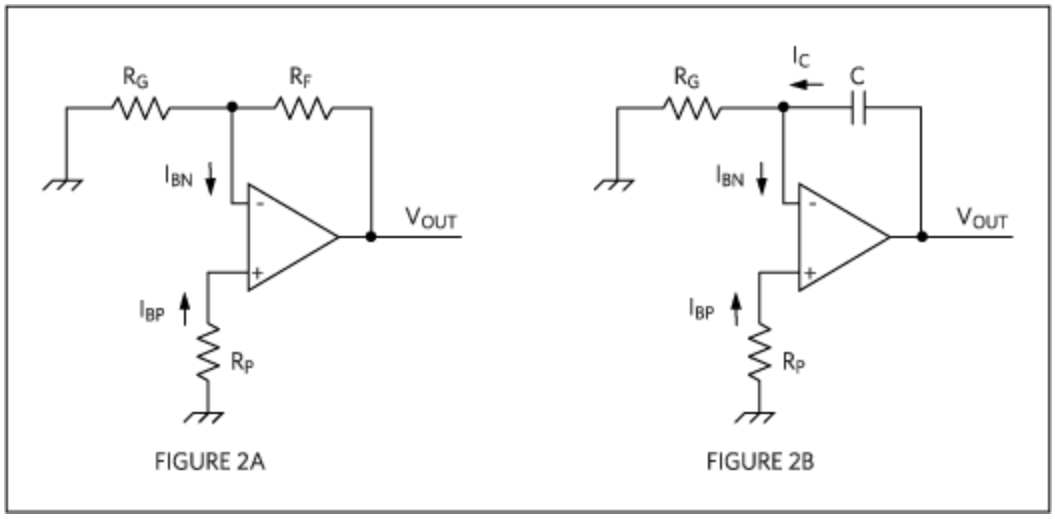

Figure 2A. Operational amplifier with resistive feedback. Figure 2B. Operational amplifier with capacitive feedback. Example devices are the MAX9620 and MAX4238 op amps.

Applying the superposition theorem on Figure 2A yields:

$$V_{OUT} = (1 + R_F/R_G) \times [(R_F//R_G) \times I_{BN} – R_P \times I_{BP}] \ldots\ldots \quad \text{(Eq. 3)}$$

The following inferences can be made from Equation 3:

- Without any input signal, the circuit yields a finite output voltage. This unwanted output error is also called **output DC noise**.
- Output voltage is produced by amplifying the **input error** or **input DC noise** by $(1 + R_F//R_G)$.
- **Input DC noise** has two components: voltage drop as I_{BP} flows through R_P, and voltage drop because I_{BN} flows through a combination of $R_F//R_G$.

Depending on the level of precision needed in the application, we must make some careful choices for both passive component values and the op amp itself. This is the best way to nullify the effect of input bias current on output accuracy. Therefore, selecting $R_P = R_F//R_G$ yields:

$$V_{OUT} = - (1 + R_F/R_G) \times (R_F//R_G) \times I_{OS} \ldots\ldots \quad \text{(Eq. 4)}$$

Selecting $R_P = R_F//R_G$ helps us reduce the output error in order of magnitude. But for high-precision applications where sensor interfaces are made with large gain (> 100V/V), it is still preferable to select low-input-offset-current op amps. Also, it is not always feasible to add R_P. Finally, both input bias currents and resistance sizing play important roles in output error. For these situations designers should select op amps with low input-bias current, low input-offset voltage, a low speed-to-power ratio, and high CMRR and PSRR, such as the MAX44260, MAX9620, and MAX4238.

Output error can be further reduced by choosing lower R_F and R_G which, in turn, increase the circuit's power dissipation. A careful trade-off between output error and power dissipation needs to be maintained when choosing the size of resistances.

We return now to Figure 2B. Voltages on both positive and negative inputs produce:

$$V_{IN+} = V_{IN-} = -R_P \times I_{BP} \quad \text{(Eq. 5)}$$

where V_{IN+} is the voltage at the noninverting input, and V_{IN-} is the voltage at the inverting input.

Applying Kirchhoff's current law on inverting input yields:

$$V_{IN-}/R_G + I_{BN} - I_C = 0\ldots.. \quad \text{(Eq. 6)}$$

We eliminate V_{IN-} in Equation 6 by substituting Equation 5, which yields Equation 7 for input bias currents and current through a feedback capacitor:

$$I_C = (R_G \times I_{BN} - R_P \times I_{BP})/R_G \ldots.. \quad \text{(Eq. 7)}$$

Now apply Michael Faraday's capacitance law:

$$V_C = 1/C \int I_C \, dt \quad \text{(Eq. 8)}$$

where V_C is voltage across the capacitor, which is also V_{OUT}. Substituting Equation 7 into Equation 8 yields:

$$V_{OUT} = 1/(R_G \times C) \times \text{Integral}(R_G \times I_{BN} - R_P \times I_{BP})dt\ldots.. \quad \text{(Eq. 9)}$$

Equation 9 provides the output voltage error in Figure 2B. To minimize this error, one can select $R_P = R_G$, and that reduces Equation 9 to:

$$V_{OUT} = -1/(C) \times \text{Integral}(I_{OS})\, dt \ldots.. \quad \text{(Eq. 10)}$$

Since C and I_{OS} are relatively constant, integrating Equation 10 over time would yield:

$$V_{OUT} = -I_{OS} \times t/C \ldots\ldots \quad \text{(Eq. 11)}$$

Equation 11 implies a voltage ramp that drives the op amp into saturation.

Errors Caused by V_{OS} and TCV_{OS}

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We will now explain the effect of input offset voltage on both the typical resistive and capacitive feedback in op-amp circuits.

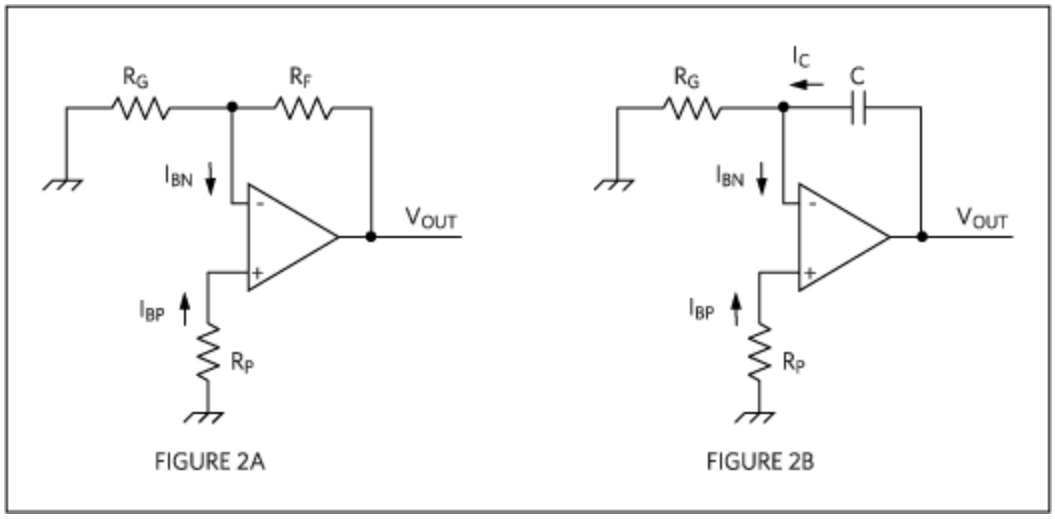

Figure 3A. Operational amplifier with resistive feedback. Figure 3B. Operational amplifier with capacitive feedback.

From **Figure 3A**, the output voltage error is:

$V_{OUT} = (1 + R_F/R_G) \times V_{OS}$ ….. (Eq. 12)

where $(1 + R_F/R_G)$ is DC noise gain. The bigger the resistances, the larger is the error.

From **Figure 3B**, we have I_C = IRG for op amps with negligible input bias current; for $V_{IN-} = V_{OS}$, we have $I_C = IRG = V_{OS}/R_G$. Using Faraday's capacitance law yields:

$V_{OUT} = \text{Integral}(V_{OS})\, dt/(R_G \times C)$ ….. (Eq. 13)

Again, if we integrate Equation 13 over time, the op-amp output is saturated to either rail depending on the polarity of the V_{OS}.

An important conclusion can be made from Equations 12 and 13: for given values of passive resistances and capacitances, the offset voltage is the main contributor to the accumulated output-voltage error.

It is time for an example. Thermal drift of offset voltage (TCVos) and input offset voltage play a very critical role in precision applications where temperature variation is common. To emphasize the significance of TCV_{OS} for an op amp in precision applications, we compare a typical op amp (maximum TCV_{OS} = 5µV/°C and maximum V_{OS} = 50µV) with the MAX9620 (maximum TCV_{OS} = 0.12µV/°C and maximum V_{OS} = 10µV). We can say that:

Maximum $V_{OS}(T) = \max V_{OS}(+25°C) + \text{maximum } TCV_{OS} \times (T\text{-}25°C)$ (Eq. 14)

Now we can use the MAX9620 op amp as an example. Assume that in a given application the temperature goes from room temperature (+25°C) to +125°C and that the maximum V_{OS} due to thermal drift is:

Maximum $V_{OS}(T) = 10\mu V + 0.12\mu V/°C \times (100°C) = 22\mu V$ …. (Eq. 15)

In contrast, an op amp with a 50µV maximum offset and 5µV/°C maximum TCV_{OS} yields:

Maximum $V_{OS}(T) = 50\mu V + 5\mu V/°C \times (100°C) = 550\mu V$ …. (Eq. 16)

These results show the importance of thermal drift for input offset voltage where high accuracy in applications is desired.[2]

Errors Caused by CMRR and PSRR Limitations

Finite common-mode rejection ratio (CMRR) in typical op amps degrades precision by introducing an offset voltage at the input. The higher the CMRR of the amplifier, the more insensitive it is to input offset-voltage change over the rated input common-mode voltage. In applications where the input signal is very small, i.e., in the order of mV ranges, high CMRR is absolutely critical.

The CMRR of an amplifier is the ratio of differential gain (A_{DIFF}) to common-mode gain (A_{CM}). CMRR can also be expressed in terms of the change in the input offset voltage with respect to change in the input common-mode voltage (V_{CM}) by 1V. Therefore:

$V_{OUT} = A_{DIFF} \times [(V_{IN+} - V_{IN-}) + A_{CM} \times V_{CM}/A_{DIFF}]$ (Eq. 17)

Equation 17 can also be termed as:

$V_{OUT} = A_{DIFF} \times (V_{IN+} - V_{IN-}) + A_{CM} \times V_{CM}$ ……. (Eq. 18)

Also:

$CMRR = A_{DIFF}/ A_{CM} = \text{delta } (V_{CM})/\text{delta}(V_{OS})$ (Eq. 19)

Finite power-supply rejection ratio (PSRR) also plays an important role in introducing additional input offset voltage with respect to change in the power-supply voltage. A change in the power-supply voltage (V_{CC}) alters the operating points of internal transistors which, in turn, affects the input offset voltage. The higher the PSRR, the more insensitive the amplifier will be to the change in input offset voltage when the power-supply voltage is changed.

$PSRR = \text{delta } (V_{CC})/\text{delta } (V_{OS})$ (Eq. 20)

The CMRR and PSRR specs provided in the Electrical Characteristics (EC) table of an amplifier data sheet are specified at a particular input common-mode voltage and power-supply voltage range, respectively, unless otherwise noted. The CMRR spec provided is not the same over the entire power-supply range, and the PSRR spec provided is not the same over the entire input common-mode range. [3]

Errors Caused by Input Impedance Limitations

Finite input impedance (R_{IN}) of an op amp will form a voltage-divider with the source impedance (R_S) driving the amplifier and introducing gain error. Consequently, a very high input impedance on the order of tens of 10^9 ohms is required to ensure negligible error.

In the above situation the amount of input signal (V_{IN}) that the amplifier sees from a source depends on the input impedance parameter defined as:

$$V_{IN} = V_{SOURCE} \times [R_{IN}/(R_{IN}+R_S)]\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad \text{(Eq. 21)}$$

From Equation 18 if $R_{IN} >>> R_S$, then $V_{IN} = V_S$.

Summary

In conclusion, if DC errors like input offset voltage, input bias currents, and finite input impedance are not addressed, op-amp measurements will simply not be accurate. That performance is not acceptable in high-precision applications where accuracy is paramount. It is also essential that designers understand the significance and limitations of the op-amp performance specs defined in data-sheet EC tables. Following the guidelines presented here, designers can select both the correct op amp and the right passive components with the correct configurations for their applications. Ultimately, using the best op amp for a design will eliminate op-amp errors and ensure the highest accuracy possible.

References

1. Sergio Franco, *Design with Operational Amplifiers and Analog Integrated Circuits*, Third Edition.
2. The MAX44250 and MAX4238 families of amplifiers also provide maximum input offset voltages in the order of 6µV and 2µV, respectively, which are needed for high-precision mV signal-level amplification in weigh scale and other sensor front-end applications.
3. The MAX44246, MAX44250, and MAX9620 families of amplifiers provide CMRR of 158dB, 140dB, and 135dB, respectively, and PSRR of 166dB, 145dB, and 135dB, respectively. Very high values of CMRR and PSRR are crucial in applications where high-precision DC performance is desired.

Related Parts		
MAX4138	1-Input/4-Output Video Distribution Amplifiers	
MAX44246	36V, Low-Noise, Precision, Single/Quad/Dual Op Amps	Free Samples
MAX44250	20V, Ultra-Precision, Low-Noise Op Amps	Free Samples
MAX44260	1.8V, 15MHz Low-Offset, Low-Power, Rail-to-Rail I/O Op Amps	Free Samples
MAX9620	High-Efficiency, 1.5MHz Op Amps with RRIO	Free Samples

More Information
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Application Note 5693: http://www.maximintegrated.com/en/an5693
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