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TUTORIAL 5450

Successful PCB Grounding with Mixed-Signal Chips - Follow the Path of Least Impedance

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Abstract: This tutorial discusses proper printed-circuit board (PCB) grounding for mixed-signal designs. For most applications a simple method without cuts in the ground plane allows for successful PCB layouts with this kind of IC. We begin this document with the basics: where the current flows. Later, we describe how to place components and route signal traces to minimize problems with crosstalk. Finally, we move on to consider power supply-currents and end by discussing how to extend what we have learned to circuits with multiple mixed-signal ICs.

A similar version of this article appears in three parts on [EDN](#), [August 27, 2012](#), [September 11, 2012](#), and [September 17, 2012](#).

Introduction

Board-level designers often have concerns about the proper way to handle grounding for integrated circuits (ICs), which have separate analog and digital grounds. Should the two be completely separate and never touch? Should they connect at a single point with cuts in the ground plane to enforce this single point or "Mecca" ground? How can a Mecca ground be implemented when there are several ICs that call for analog and digital grounds?

This tutorial discusses proper printed-circuit board (PCB) grounding for mixed-signal designs. For most applications a simple method without cuts in the ground plane allows for successful PCB layouts with this kind of IC. Next, we learn how to place components and route signal traces to minimize problems with crosstalk. Finally we move on to consider power supply-currents and end by discussing how to extend what we have learned to circuits with multiple mixed-signal ICs.

Follow the Current

Remember that we call a collection of connected electrical or electronic components a "circuit" because currents always flow from a source to a load and then back via a return path—a circle of sorts. Keeping in mind where the current flows, both in the direction intended to do the desired job as well as the resultant return current, is fundamental to making any analog circuit work well. And, yes, all digital circuits are analog circuits; they are a subset for which we assign meaning to only two states. The transistors and other components, as well as the currents and voltages within the circuit, still operate by the same physical



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principles as other analog circuits. They will induce return currents in the same way as any other circuit.

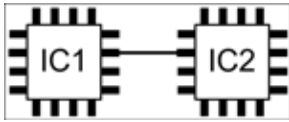


Figure 1. A simple connection is a direct connection from one IC to another.

Figure 1 illustrates the simplest of connections in a design: a direct connection from one chip to another. Taken as an ideal circuit in an ideal world¹, the output impedance of IC1 would be zero and the input impedance of IC2 would be infinite. Therefore, there would be no current flowing. In the real world, however, current will flow from IC1 and into IC2, or the reverse. What happens to this current? Does it just fill up IC2 or IC1? That is a facetious rhetorical question.

Actually, there must be another connection between IC1 and IC2 to allow the current flowing into IC2 from IC1 to return to IC1 and vice-versa. This connection is usually ground and is often not indicated in a digital section of a schematic (Figure 1). It is at most implied by use of ground symbols as shown in Figure 2A. Figure 2B shows the full circuit for current flow.

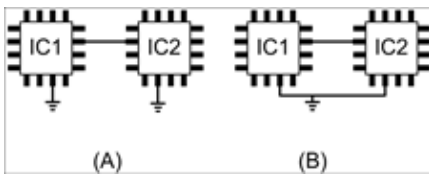


Figure 2. The simple circuit of Figure 1 with ground implied (2A) and with the ground current path indicated (2B).

Of course, the ICs themselves are not the sources of current. The power supply for the circuit is. To keep things simple, we assume a single power rail and think of the supply as a battery. To be complete, we bypass the supplies to ICs with capacitors.

All DC currents ultimately start and end at the power source. Figure 3 shows the complete circuit with DC current flow when IC1 is sourcing the current indicated.

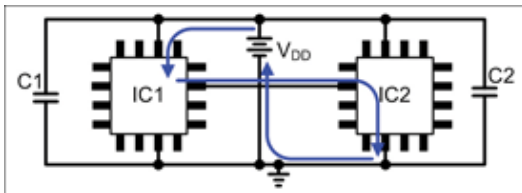


Figure 3. IC1 sourcing DC current.

For high-frequency signals ("high" largely determined by the bypass capacitance and power-source impedance), the current starts and ends with the bypass capacitor. Figure 4 shows the high-frequency signal current flow.

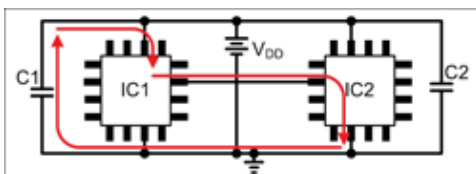


Figure 4. IC1 sourcing the high-frequency signal current.

It is important to remember that an output is not always the source of currents. For example, consider the case where an output from IC1 is connected to an input of IC2 which has a pullup resistor to V_{DD} . **Figure 5** shows transient (high frequency) current flow for this situation with the current coming from C2 through the pullup in IC2 over to the low-side FET in IC1, which is on, and then through the ground lead of IC1 to the ground lead of C2. While IC1 is the "driving" device, sinking current at its output pin by shorting it to ground with a FET, the current source is from C2 through IC2.

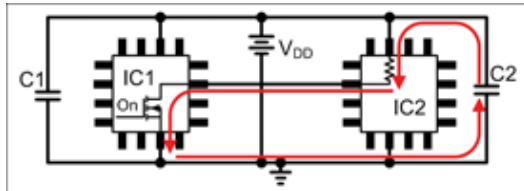


Figure 5. IC2 sourcing the high-frequency current.

If the output pin of IC1 in Figure 5 stays low for a long time, then the static current that will be drawn will come directly from the power source (**Figure 6**).

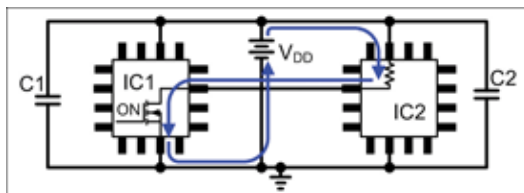


Figure 6. IC2 sourcing DC current.

To this point in our discussion of the basics, the model has been somewhat simplistic. We conveniently divided signals into low frequency and high frequency as if there were a well-defined boundary between the two. The truth is that both paths are always involved. In Figure 6, at the initial transition of the IC1 output to the low state, the current comes from the bypass capacitor at IC2. This is because the output of IC1 is "demanding" a near-instantaneous current from the input pin of IC2, which pulls this current from its power pin.

We placed a bypass capacitor at IC2 with very short connections to its power and ground pins precisely to supply the fast current demands. The power source cannot provide this transient current as it is not very close to the IC. Thus, it has substantial resistance and, more importantly, inductance between it and the power pin of IC2. This is the whole reason for placing bypass capacitors at the ICs: to supply the transient (high-frequency) currents that the power supply cannot. As the transient settles out, more and more current comes from the power source and less and less comes from the bypass capacitor.

We simplify this concept further by saying that the DC current comes from the power source and the AC current comes from the bypass capacitor(s). We know, of course, that it is a bit more complex than this explanation.

As we consider more dynamic situations, we find that all the currents flow through a combination of the above four paths. The common path in either direction starts with the power pin of the sourcing component (IC1 or IC2), proceeds through that component and through the interconnect to the other component (IC2 or IC1), and then through the second component to its ground pin. How the current completes its circuit from ground to the power pin of the sourcing component depends on the speed of the signal. The DC current will all return to the ground lead of the power source; it will flow from the power lead of the power source to the power pin of the sourcing component. High-frequency signal current will instead return to the ground lead of the sourcing component's bypass capacitor, which also supplies the current to the power pin. In reality, both paths are always involved, with the DC path dominating for low-frequency signals. Keep in mind that even if a digital signal transitions at a slow rate (for example, a 1Hz square wave), the state transitions that cause the

transient currents are just as fast as with a much higher frequency signal. They simply do not occur as often.

Of course, we are dealing with a good design here, so the bypass capacitors and the IC power and ground pins are very close. Proper bypassing like this makes a designer's job much easier. We can usually just think of the bypass capacitor and the IC as one entity when considering the flow of signal currents across a PCB.

Notice, finally, that the power current for high-speed AC signals travels a very short distance from a bypass capacitor to the IC that it is bypassing. The paths through the ICs themselves, of course, are short. The vast majority of the distance of the current loop is in the interconnect from the output of one chip to the input of the other and the ground return path. Review Figure 4 and Figure 5 and consider what happens if the ICs are separated by a greater distance. The bypass capacitors stay close to their respective IC, and all the distance is added to the interconnect and the ground return. For higher-speed signal currents, this is where we will see problems...if they occur.

Digital and Analog Supplies and Grounds

In the circuit diagrams above we have not identified the ICs and signals as digital or analog. IC1 could be an op amp with the low-side FET as the lower part of an output stage; the pin on IC2 could be the input to an analog-to-digital converter (ADC). IC1 could just as easily be a microcontroller with a push-pull output for a standard I/O pin; the IC2 input could be a control pin on a digital-to-analog converter (DAC).

We mention ADCs and DACs as these are typically the components that cause concerns with grounding for both the analog and digital signals.

Analog circuits tend to work with signals that vary in a smoother, continuous fashion and for which small changes in voltage or current are meaningful. Digital circuits tend to transition abruptly from one state to another, generating pulses of currents; they tend to have a wide window of voltage which maps to a single state. It is these relatively large, sharp pulses of digital current during transitions that can overwhelm the precise analog signals if the two are not adequately separated from each other.

The Path of Least Impedance

It is such a well-understood principal that current flows in the path of least resistance that the concept has made its way into everyday language. Unfortunately, this is only true for DC currents. A more complete and accurate way of stating the principle is that the current flows in the path of least impedance.

For DC, only the resistive part of impedance matters. In the case of a solid ground plane, the proverbial straight line is the path of least resistance. In fact current will flow in more indirect paths as well. The amount of current through any particular path will be inversely proportional to the distance because the ground-plane resistance per unit length is very uniform. Therefore, the most current will flow in the straight-line path of least resistance, and progressively less current will flow through paths that deviate more and more from that straight-line path. For simplicity we will indicate DC currents as flowing in the straight line path, with the understanding that there is a fairly wide spread of currents with the largest current moving along that straight line.

For the signals that matter most to us here, the AC signals of some speed, we have to consider the reactive portion of impedance as well.

For a PCB with a ground-plane layer adjacent to the signal layer, we have a well-defined impedance that is determined by the geometry of the trace, the thickness of the board layer that separates the trace from the ground plane, the board material, and the frequency of the signal. All the mathematical details for these

givens are beyond the scope of this tutorial. Fortunately, it is not necessary to work through all the math in order to use the concepts and get good results. The [References](#) at the end of this tutorial cover the details well.

Consider our original very simple example of a single trace between two ICs (Figure 1). This time we show them positioned on a PCB with the trace taking an indirect route (**Figure 7**).

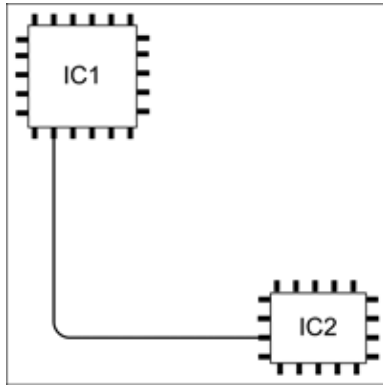


Figure 7. Simple indirect trace.

Assume now a solid ground plane with the ground connection at each IC near the trace connection point. The return currents have to go from the ground connection of one IC to the ground connection of the other. Since we have a solid ground plane, the path of least resistance, and thus the path of DC current, will be a straight line (the blue arrow in **Figure 8**). At high frequency the mutual inductance between the trace and the ground plane beneath it make the ground path of least impedance directly under the trace (the red trace in Figure 8).

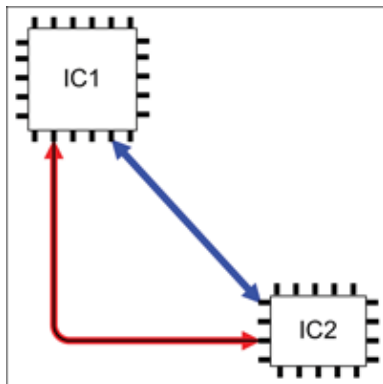


Figure 8. Ground-return current paths show the path of least resistance (blue) and path of least impedance (red).

But what is "high frequency?" A common guideline² is that frequencies of a few hundred kHz and above have return currents which follow the path under the signal trace. The actual frequency above which we consider to be "high" is determined by the trace, board geometries (trace width, space between layers), and board material (dielectric constant). For the return current to follow the trace, in most common cases we need not worry about exactly what frequency this is.

Mathematical treatments of this phenomenon are extremely complex and, to this author, very confusing. Fortunately, Dr. Bruce Archambeault has published on this matter³ and has graciously provided the following figures which visually demonstrate this subject far better than a page full of equations can ever do.

Figure 9 shows the geometry of an example "U"-shaped trace over a ground plane.

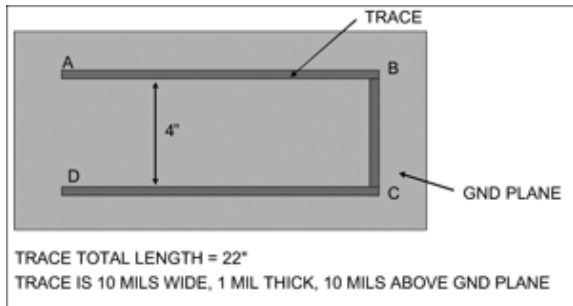


Figure 9. Physical geometry for this example. (Drawing courtesy of Dr. Bruce Archambeault.)

Dr. Archambeault then ran electromagnetic simulations for signals of different frequencies to see by what paths the current would flow. The forward signal currents for each case, of course, are constrained to the trace. However, the return ground currents can flow anywhere on the ground plane.

Figure 10 shows how the currents for a 1kHz signal flow. The ground current primarily flows directly from the load to the source in a straight line, as indicated by the narrow yellow line. A small amount of the ground current flows along the signal path (light blue), while even smaller amounts flow in between these two paths as indicated by the darker blue color of much of the plane.

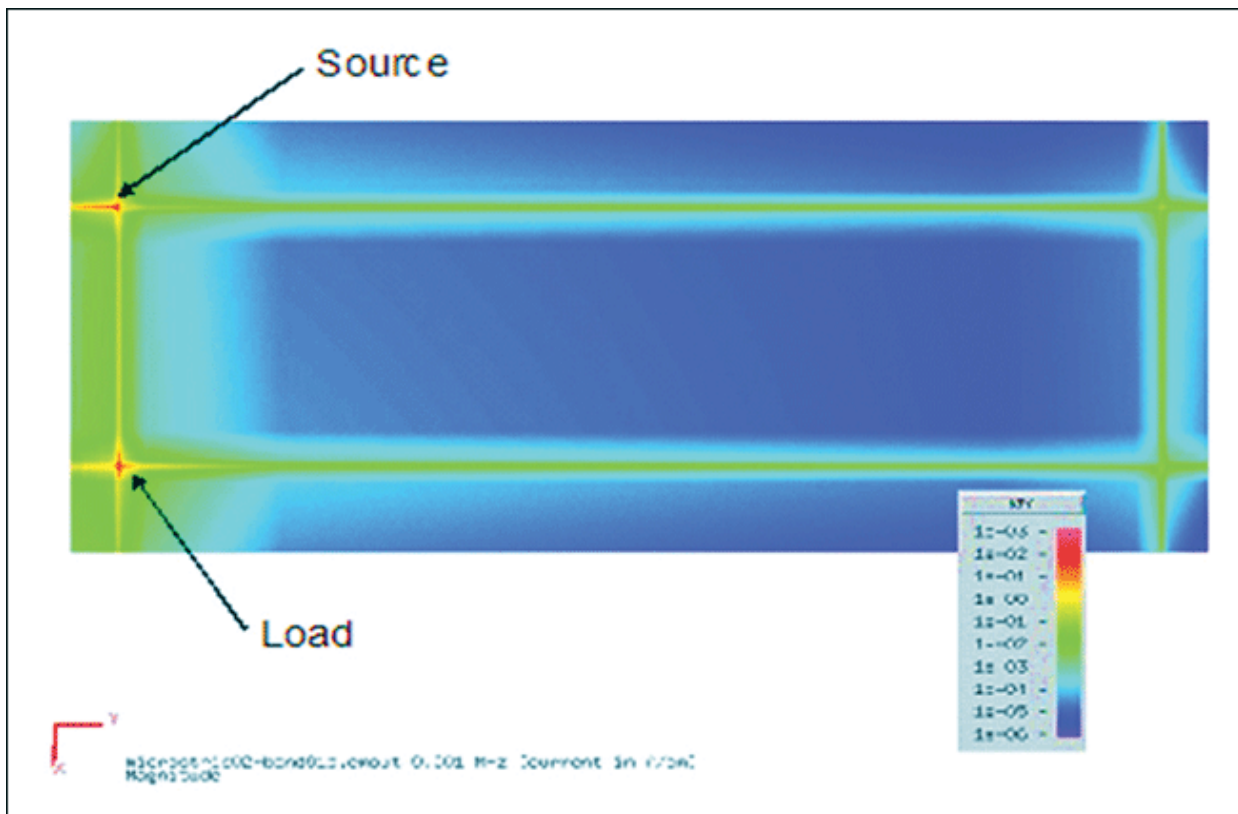


Figure 10. 1kHz ground current flows from load to source in a straight line. (Drawing courtesy of Dr. Bruce Archambeault.)

Figure 11 shows current for a 50kHz signal flowing primarily along the signal trace (the wide green line following the path of the trace) and, to a lesser extent, directly from load to source (the fainter, wide, green line from the two ends of the trace) and in between. The middle area is light blue and not dark blue, indicating

minimal current flow.

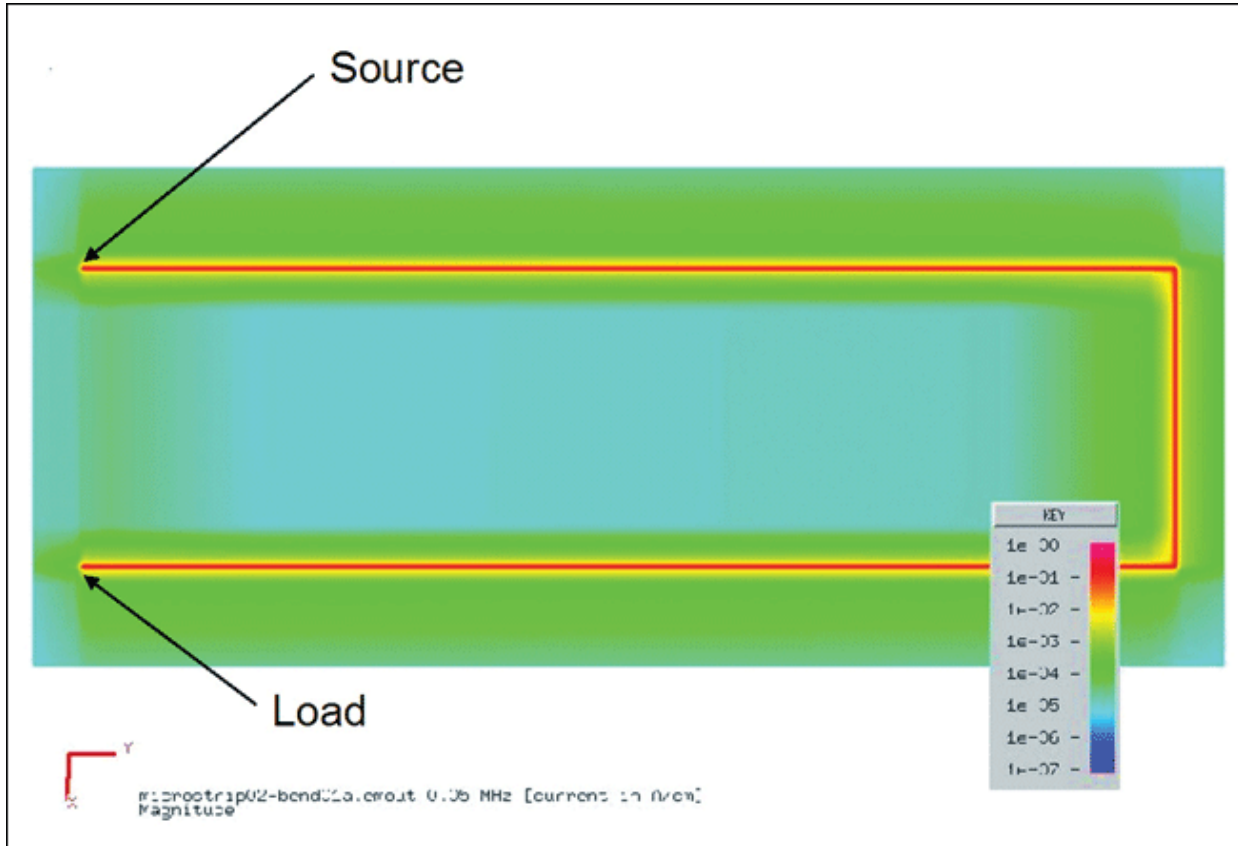


Figure 11. 50kHz ground current flows everywhere. (Drawing courtesy of Dr. Bruce Archambeault.)

Finally, **Figure 12** shows the current paths with a 1MHz signal. Virtually all the return ground current is flowing along the path of the signal trace.

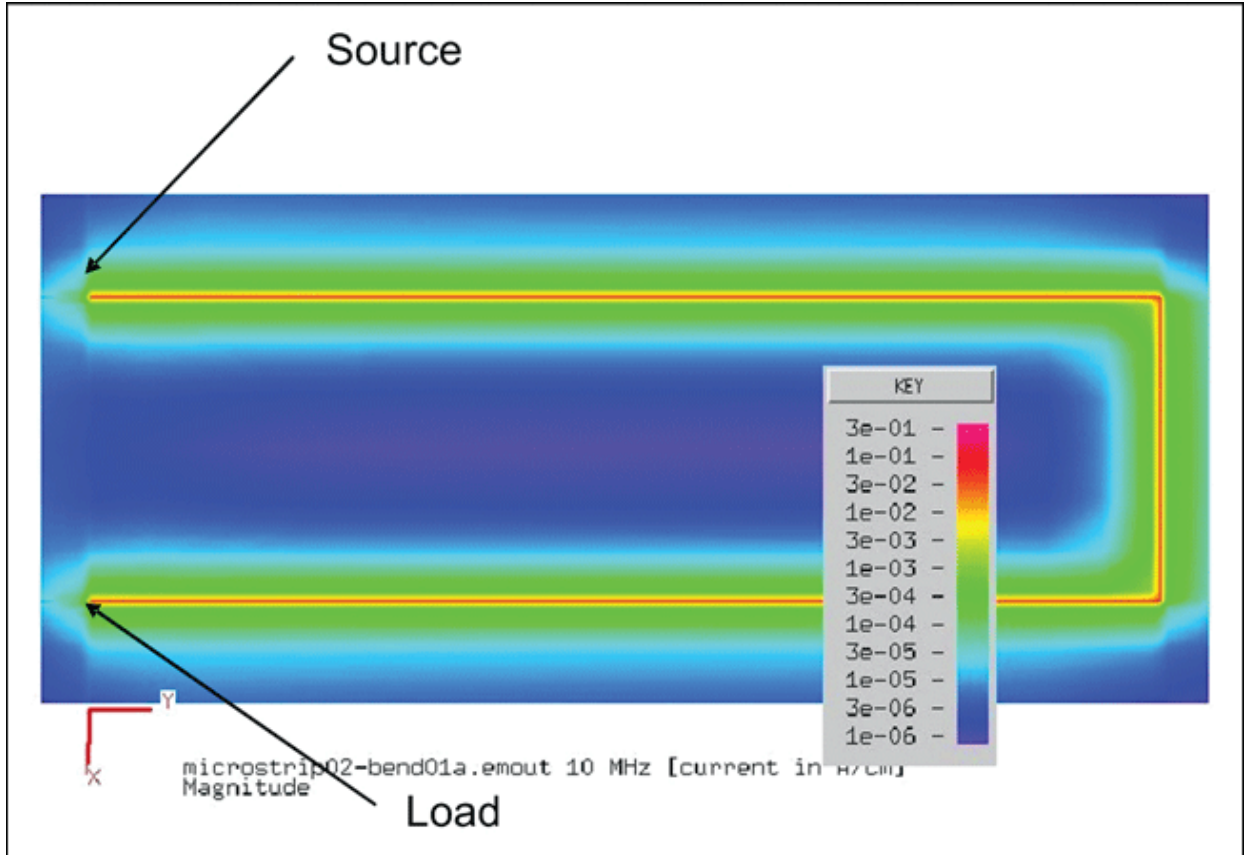


Figure 12. 1MHz ground current follows the signal trace. (Drawing courtesy of Dr. Bruce Archambeault.)

As one would expect, return current does spread out on the plane wider than the trace itself. The distribution of current for these higher frequencies is given by the following equation.⁴

$$J(x) = \frac{I}{w\pi} \left[\tan^{-1} \left(\frac{2x-w}{2h} \right) - \tan^{-1} \left(\frac{2x+w}{2h} \right) \right] \quad (\text{Eq. 1})$$

Where:

J(x) is the current density;

I is the total current;

w is the trace width;

h is the board layer thickness (the height the trace is above the plane);

x is how far from directly under the trace we measure the current, as shown in **Figure 13**.

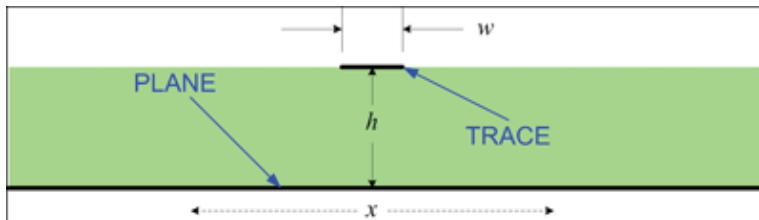


Figure 13. Cross section of board.

It is important to note that Equation 1 is independent of frequency (again, assuming that the frequency is high enough, as discussed above). When we evaluate Equation 1, we get a Gaussian-looking distribution with a peak directly under the center of the trace. If we sum the current between $x = -h$ to $x = h$, we find that 50% of the total current is in this range. Further, 80% of the current is between $x = -3h$ and $x = 3h$. As one would expect intuitively, the thinner the board layer (i.e., the closer the trace is to the plane), the tighter the current distribution will be.

Bypass Capacitors Are Important

As mentioned earlier in the tutorial, a more complete description of the current flow in any circuit includes the bypass capacitor at each IC and the power source. We start with the simplified two-IC circuit example from Figure 8. We then include the bypass capacitors in **Figure 14**. This diagram shows the current paths with IC1 sourcing. In this example there is a solid ground plane on a layer adjacent to the signal layer, which is assumed to be the component layer. Power is distributed on this top layer with the large metal traces shown in gray. Connections to the ground plane are made with vias from the green metal section on the signal layer to the ground plane.

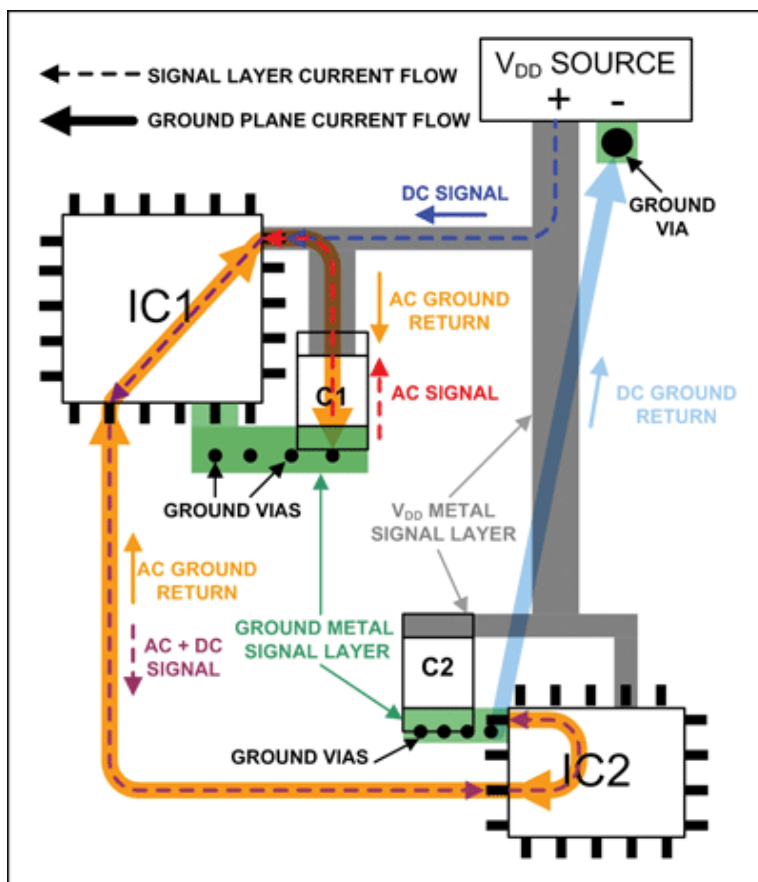


Figure 14. Complete current paths, IC1 is sourcing.

The signal currents on the signal/component layer are shown with dashed lines. They are the easiest to understand, as they are strictly confined to the signal traces that we choose to place. The return currents have an entire plane over which they can flow. Since DC currents will flow through the path of least resistance, we know that the DC return path will go directly from the ground pin of the load device, in this case IC2, to the ground connection of the power source by the shortest distance, a straight line. The high-frequency (transient)

currents will flow under the signal trace with a distribution determined by the geometry of the trace and board.

We can dig deeper into the current flow for signals that are in-between cases. Start with frequencies low enough that a significant portion of the current flows from the power source, rather than virtually all of the current flowing from the capacitors. In this case there is still mutual inductance that will force the current to return under the signal trace, but the distribution will, of course, be much wider. Also, once the return current under the trace reaches the IC, it will not all return to the capacitor ground. Instead, a percentage of the current sourced from the capacitor will return to its ground, while the rest will return to the power source ground. Finally, as the frequency gets lower the mutual inductance will have less and less affect; more current will flow through the DC path.

Fortunately, this in-between case is already managed by our efforts to handle the high-frequency and DC cases, as long as we also do a good job of both bypassing the ICs and distributing power properly. These later two items are really two facets of the same effort. As the power source is moved farther away from the IC that it powers, the impedance—both resistance and inductance—between the two will increase. This also happens as the trace connecting the two decreases in width. The more impedance between the power source and the IC (remember to include the return impedance) that is exhibited by the interconnect, the more the bypass capacitor will be relied on for supplying lower frequency currents. Thus more capacitance is needed as the power source impedance increases.

So once again we must satisfy the requirement of adequate bypassing of power at the ICs.

For completeness, **Figure 15** shows the current flow when IC2 is sourcing.

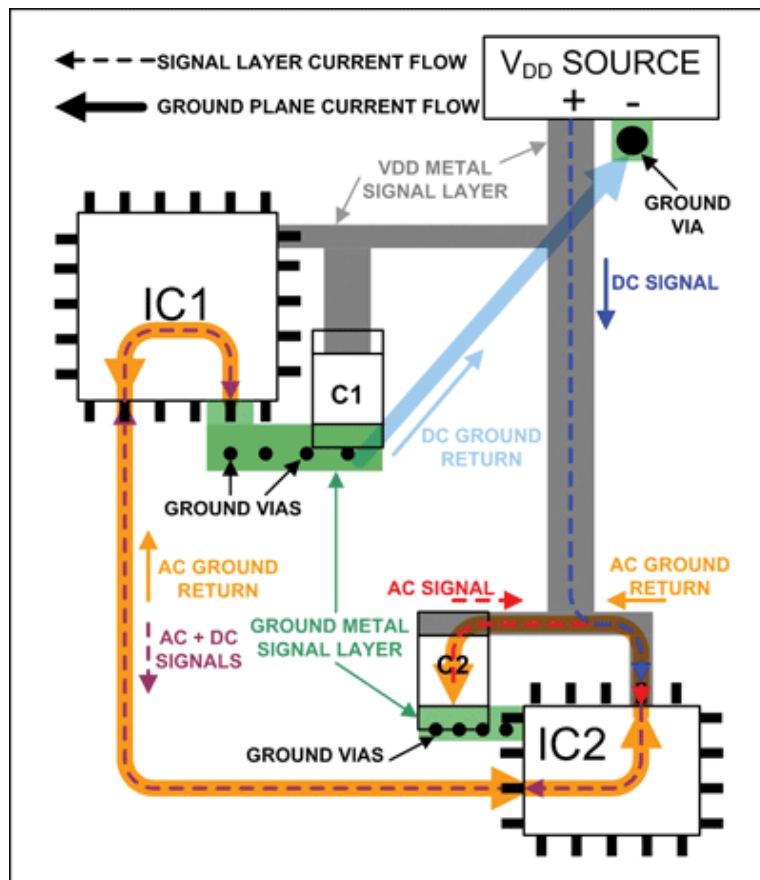


Figure 15. Complete current paths, IC2 sourcing.

Notice the interconnecting trace on the signal/component layer. We only changed the direction of the arrows for the signal current and the AC return current. In this case it is C2, the bypass capacitor for IC2, which supplies the AC signal current through IC2's V_{DD} pin to the signal pin on IC2. The signal current delivered to IC1 goes to ground through IC1's ground pin; the AC portion returns on the ground plane under the signal path and the DC portion returns in a straight line to the power source.

Ground Is Not an Equipotential

At this point it is important to understand that a ground plane, despite what we were taught in EE101, is *not* an equipotential. First of all, no matter how thick the copper is for your ground plane, it does have resistance. Therefore, if the analog and digital return currents (or any two currents) share a portion of the ground plane (i.e., their currents flow through the same metal) there will be crosstalk between the two as the copper resistance causes IR voltage drops. Think of it this way: the ground pins of two different components connect to the ground plane at nearly the same point and their currents return to a single point at the other end of the board. Assume that the copper resistance of the plane along this path is 0.01Ω and that component A is sourcing 1A while the current from component B is $1\mu\text{A}$. At the end where these components connect, the ground voltage will be 10mV greater than the ground voltage at the point where the currents return. Even component B, which is only putting out $1\mu\text{A}$, will experience a 10mV rise over the return point. If the current from component A alternates from 1A to 0A, any voltage referenced to component B will vary up and down by 10mV along with this current.

Shared return paths often cause problems when digital circuits co-reside with analog circuits. The sharing can interfere with proper operation of a precision analog circuit.

Another cause of nonuniform voltages across a ground plane is electrical length. At higher frequencies the length of the current paths through the plane can be a significant percentage of the wavelength of the signals propagating on the board. We will not pursue this fact in this tutorial. It is enough to say that shorter is better.

Putting It All Together

With the basics of current flow on a PCB understood, we can start using this knowledge to properly handle the grounding of mixed analog-digital ICs. Ultimately, the goal is to ensure that the digital and analog currents do not share portions of the same return path.

By now you realize that the whole objective is to minimize commonality of return paths for the digital and analog signals. This is, in fact, the goal. If we do this, we will eliminate the major cause of problems when the "nasty" digital signals corrupt the "pristine" analog signals.

A common assumption is that one should cut the ground plane into a digital section and an analog section. This is a good starting point. As you will see, if we lay out everything properly, we can just fill in the cuts with no change in performance.

Cut the Ground Plane...for Now

We start with a generic ADC on a board as the only component with both analog and digital circuitry. Then we will determine where to cut the ground plane for a single point ground.

Figure 16 shows the pin connections for our ADC chip. Only the power and ground pins are labeled explicitly. The other labeling just indicates whether the connection is for an analog or digital pin; their specific functions are unimportant. An analog pin may be one of several signal input pins or a reference input or output. A digital

pin may be part of a serial or parallel interface, a control pin, or a chip select. For our discussion, we treat them the same regardless of their specific function.

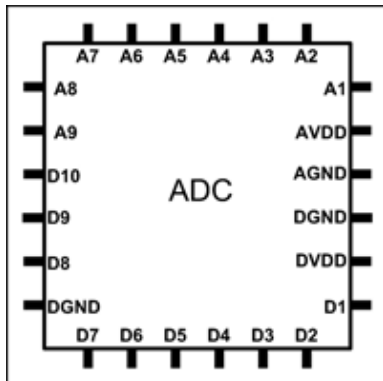


Figure 16. An ADC IC.

Note that the digital pins are contiguous, as are the analog pins with analog and digital ground adjacent. This is not uncommon, because chip designers must manage the same realities as board designers. Note also that there are two digital ground pins. This is sometimes necessary so that the ground currents in the chip do not cause problems as they run from one end of the chip to the other.

Since the analog and digital pins are grouped nicely here, it is very easy to decide where to put the (temporary) ground plane cuts.

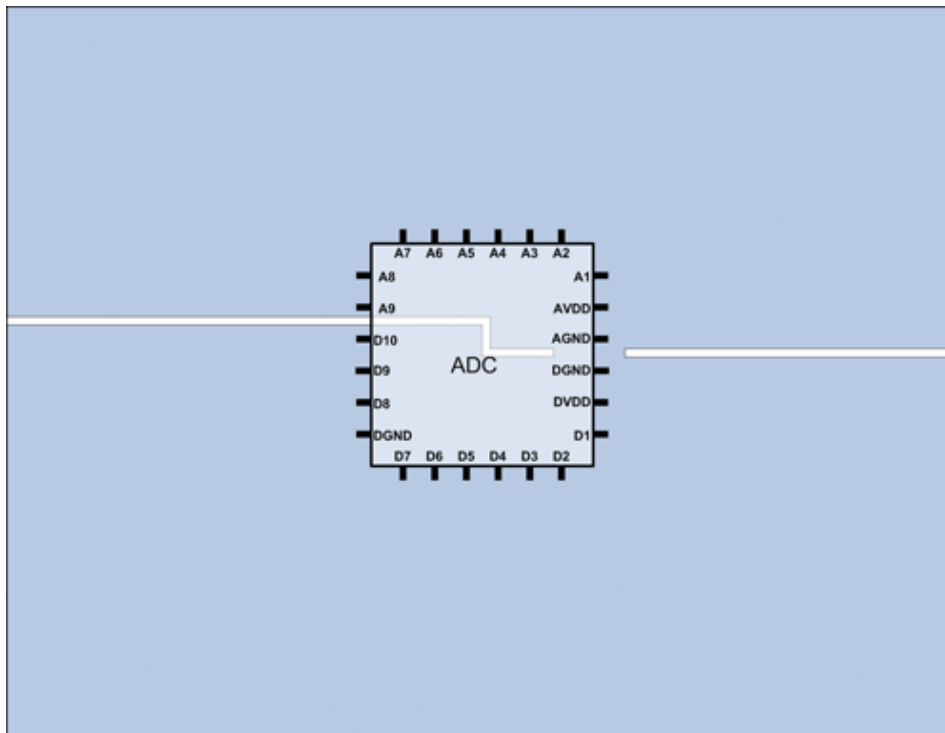


Figure 17. ADC with cut ground plane.

We see the ground plane in blue in **Figure 17** with the single-point ground right at the adjacent analog and digital ground pins. Generally when a cut ground plane is to be used like this, the designer puts all the digital chips and related components on one side of the cut and all the analog chips and related components on the

other side. In this way their ground pins can connect to the correct portion of the ground plane. Recall that for this example our ADC is the only device with both analog and digital pins and signals.

Assume now that we did a fine job on this, that all the digital components are completely over the digital portion of the ground plane, and that all the analog components are over the other portion. We are not done yet. We have to consider the routing of signal traces.

Routing the Signal Traces

We begin with a digital signal from one of the other ICs in this design routed as shown in **Figure 18**.

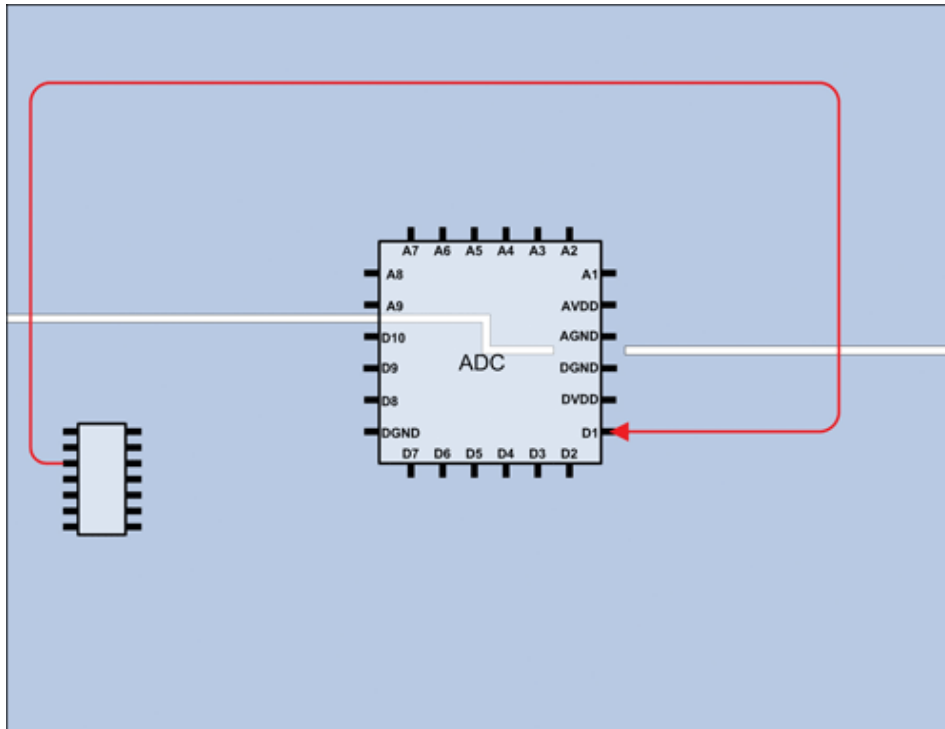


Figure 18. Bad routing of a digital trace.

This trace is routed over much of the analog section and crosses the ground cut in two places. Most designers would recognize this as bad form because it results in a digital trace in the analog area which can, therefore, contaminate analog signals. While that is true, the extent of the problem is often not fully appreciated. Consider where the AC current would return.

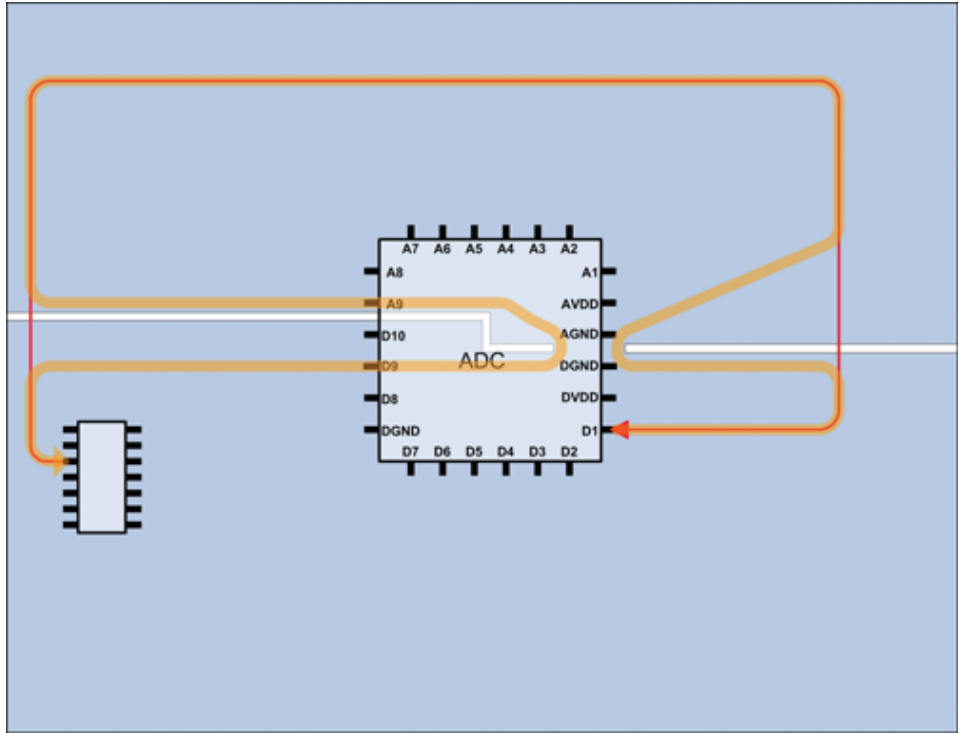


Figure 19. Ground return for the bad digital trace.

Figure 19 shows the return current in orange. Notice how it follows the signal trace until it encounters a cut. At that point it can only return through the single-point ground to get to the other side of the cut. Consequently, we not only have the digital current with its high-frequency content running through the analog circuitry's ground—something we were trying to avoid—but we also have created two nice loop antennas that will radiate these signals.

For our ground cut method to work, we must ensure that the digital and analog components stay on their respective side of the cut and that the traces do too.

What happens when we meet this requirement? **Figure 20** shows all of the signal traces routed without crossing any ground cut. The return currents flow under the signal traces, minimizing the loop area because the only thing separating the signal traces from the ground plane is the thickness of the PCB itself.

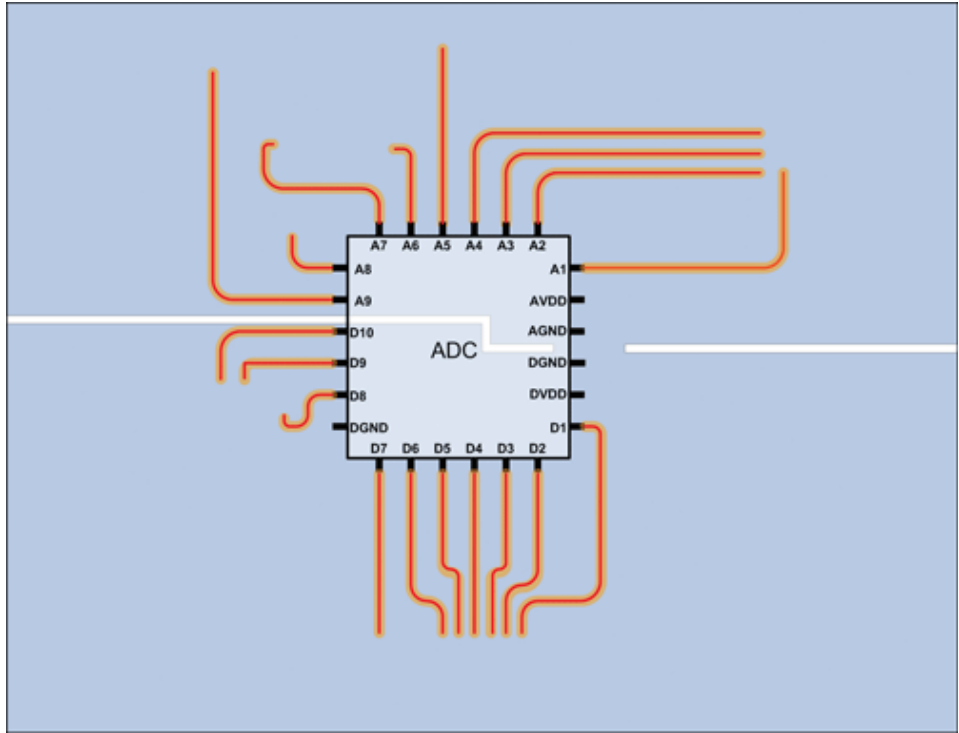


Figure 20. All traces routed on the proper side.

Take a close look at the ground current in Figure 20. None of the currents "wants" to cross the ground plane cuts. This is because we have been careful to place components so that all the connections, digital or analog, are over their respective ground areas. Then we routed all traces to stay in the appropriate area. Since no currents are crossing the cuts, the cuts are serving no purpose and thus can be eliminated (i.e., filled in with metal).

What About the Power?

We decided to eliminate the ground cuts in our example layout because there are no signal return currents that "want" to cross the cuts. We do, however, have to consider the power connections. If both analog and digital power is from the exact same supply, then the source and its return *must* be on one side of the cut or the other (Figure 20). In this case all the DC return currents (and frequencies low enough that significant current comes from the supply and not the bypass capacitors) from the other side of the cut must funnel through the narrow ground bridge rather than going straight to the power return connection. This makes their path longer, the resistance that they encounter larger, and thus the voltage drops greater.

This layout is no problem for return ground currents where the pins on the ADC sink the signal current, because these currents return from the ground pins which are both at the bridge. However, currents from ground pins on other components have to take an indirect route. **Figure 21** illustrates these currents.

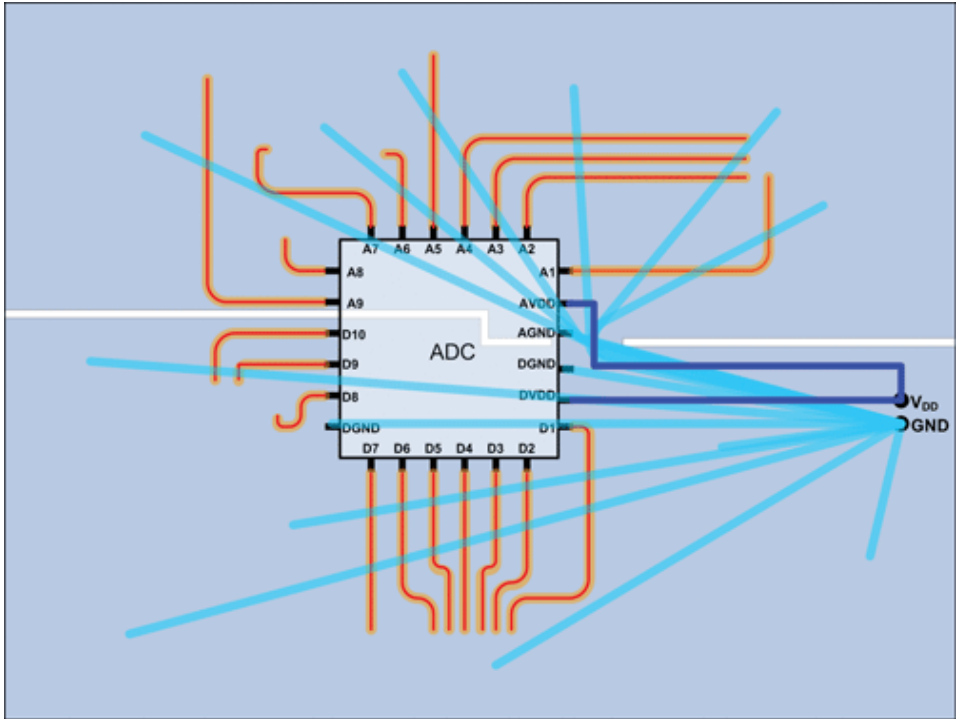


Figure 21. DC ground currents with cuts.

Removing the Cuts

If we remove the cuts, the DC return currents can flow more directly, with lower resistance and thus lower voltage drops. **Figure 22** shows the same ground currents but with the cuts removed.

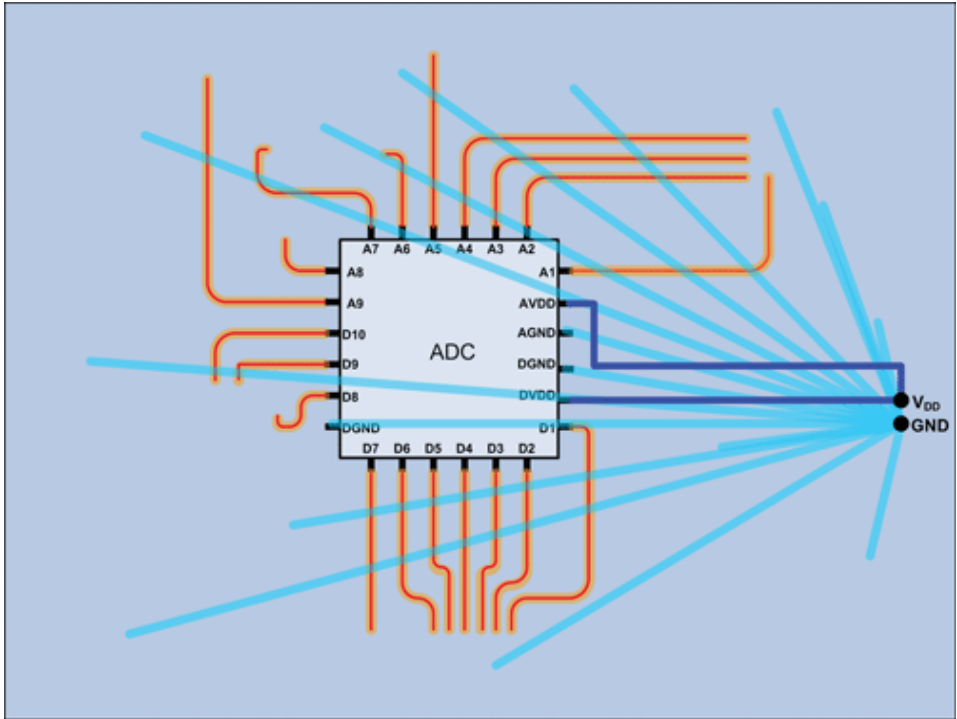


Figure 22. Circuit of Figure 21 with the ground cuts removed.

The same thinking can be extended to the situation where there are multiple rails. We just have to remember where the return currents will flow and take the multiple rails into account, just as we have done with the single rail.

Grounding Challenge of Multiple Mixed-Signal ICs

The problem with cut ground planes becomes more apparent when considering a design with more than one IC requiring both analog and digital grounds. Assume that we have two of the same ADCs discussed above. **Figure 23** shows this configuration and how it is not feasible to obtain the desired single point ground.

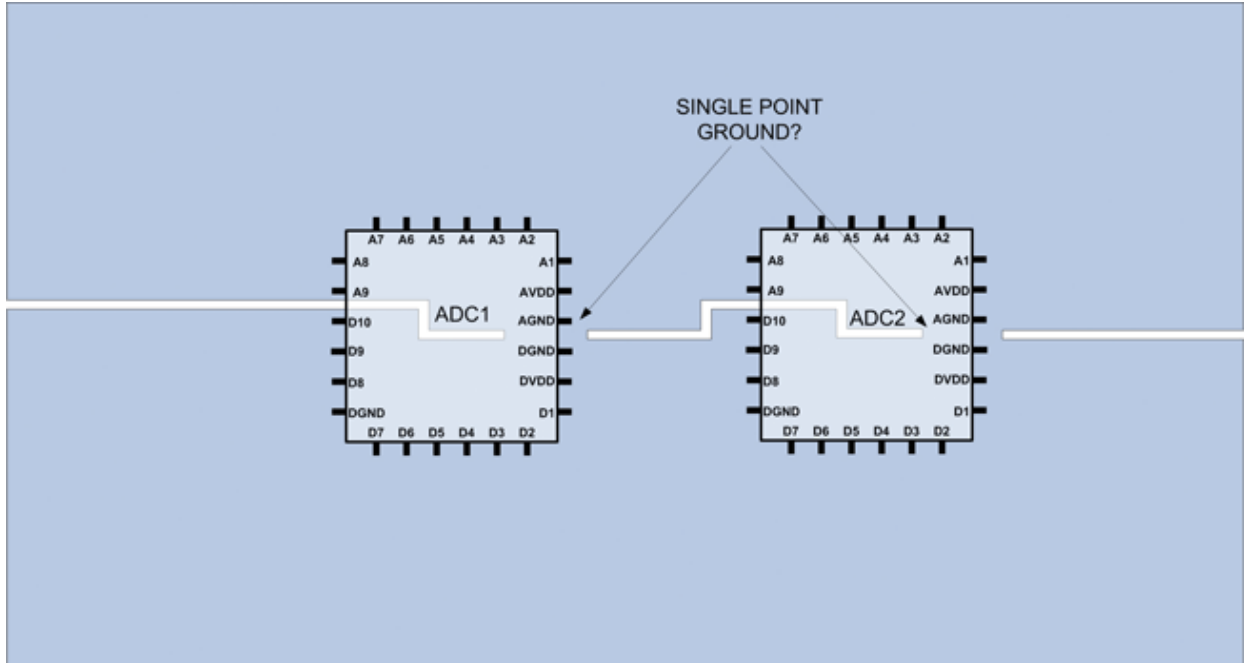


Figure 23. Two ADCs with a cut ground plane.

An immediate reaction to this situation could be to rotate one of the ADCs by 180 degrees, thus merging the two into a single point ground. However, that would put the digital portion of one circuit north of the ICs with the analog section south of the ICs; the arrangement would be flipped for the other circuit. The result would be chaos—a mess of analog and digital signals in each other's way. Even if this could be made to work, it does not solve the problem of three or more chips with both analog and digital grounds.

Fortunately, we can apply the same grounding principles for a single mixed-signal IC. We imagine that the cuts are there, or we temporarily insert them if we are imagination challenged. Then we place components and route so that we do not allow traces to cross the cuts. We may also need to keep ADC1's analog signals from sharing ground paths with ADC2's analog signals. This is usually easy to do, as we will naturally be placing the components for each ADC's circuit closer to it than to its neighbor. **Figure 24** shows what this might look like with the signal currents shown as red lines and the AC return currents shown as orange lines.

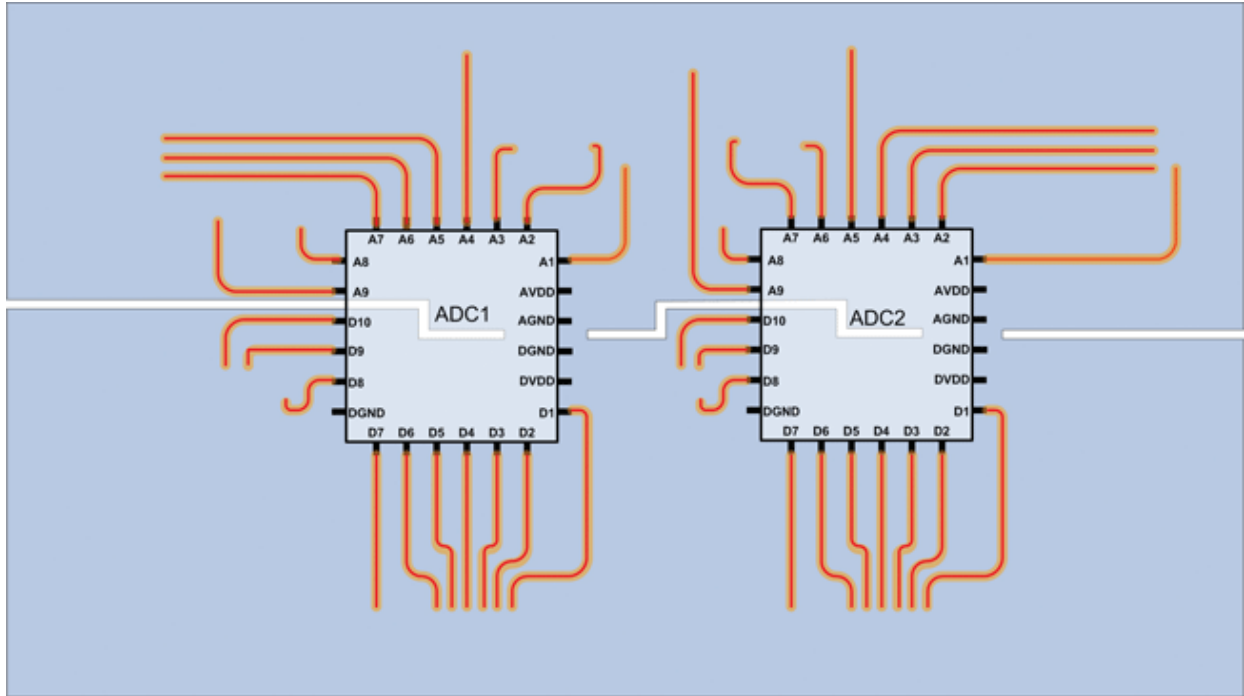


Figure 24. All traces routed on the proper side of the cuts.

As with the example of a single mixed-signal IC, none of the currents "wants" to cross the cuts so the cuts can be eliminated.

The same thinking can be extended to more complex situations. In general, it is just a good idea to think about where the current will flow for any signal and how it could interfere with, or be corrupted by, other currents flowing through the same metal. This is enough for most applications.

Sometimes Cuts Can Be Useful

There are situations where various mechanical constraints, such as the desired locations of connectors, make it difficult to keep current flow, particularly low-frequency or DC currents, away from circuits that we want to protect. In these cases we may have to resort to judiciously placing cuts in the ground plane.

The desire to avoid such complications is good motivation for considering mechanical placement of connectors along with PCB component placement and routing early in a project. If connectors are placed with consideration for the layout at the outset of a design, it can make the final layout much easier, cleaner, and most importantly, successful.

Even when we carefully consider the interaction between mechanical placements and signal flow, we can easily have situations where external requirements force us to put interfaces in places that make it hard to keep some currents from going where we do not want them to go.

Figure 25 shows a board with digital, analog, and power interfaces in specific locations because of system requirements. We did a good job of placing the noisy digital content adjacent to, but separate from, our sensitive analog circuitry. As noted above, any chips that are both analog and digital are judiciously placed in the bordering area.

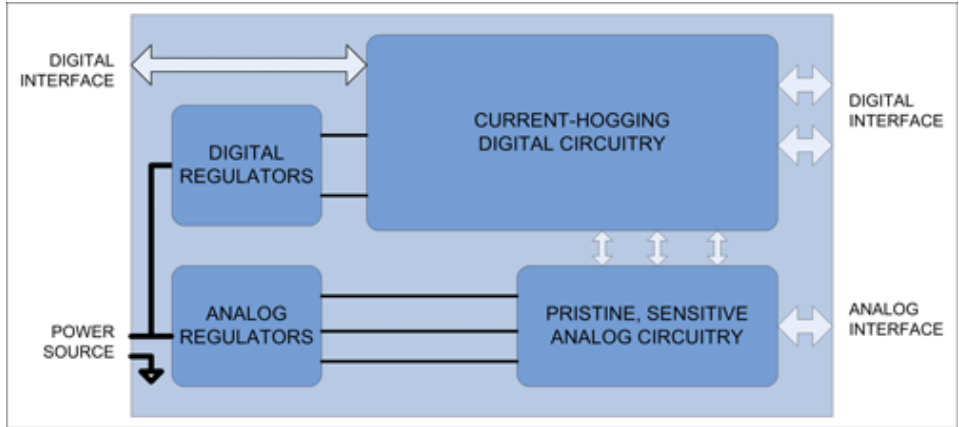


Figure 25. A digital and analog board with fixed external interface locations.

We have even done a good job of positioning the power regulators so that the higher-frequency ground returns for analog and digital will not tend to share paths. However, remember that DC and low-frequency power currents will all return to the power source ground which is in the lower left corner by the path of least resistance: a straight line.

The result is that large DC and low-frequency currents from the lower right region of the digital section will run straight through the sensitive analog circuitry. We could fix this by placing a horizontal cut between the analog and digital circuit sections that extends to the right edge of the board. However, we would not want to run the interface signals between the digital to the analog sections across this cut. Routing these traces around the cut would cause them to take a long, indirect route which could be quite impractical, especially if there are a lot of them or if they are particularly fast.

Another idea would be to place a vertical cut between the analog circuitry and the analog regulators, forcing the digital power return current to flow away from the analog circuitry. This would also require us to route the analog power around the cut. **Figure 26** shows how this would be done.

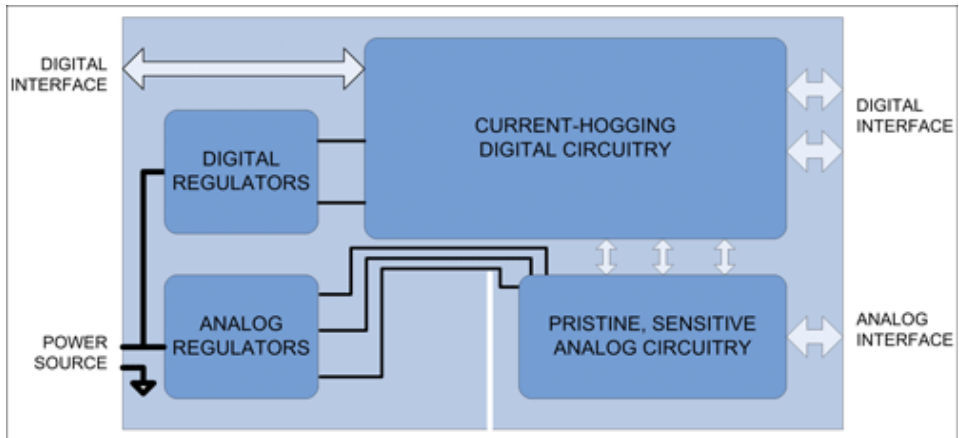


Figure 26. Analog and digital board with ground cut.

The DC path of least resistance from the digital circuitry to the power source ground is now no longer a straight line. It is, instead, a path that passes above the cut, thus bypassing the analog circuitry (in all its pristine majesty). This arrangement might be adequate. However it can also be cumbersome if there are several analog supply rails as shown.

In some cases the analog regulators themselves are sensitive with low noise necessary for proper operation of

the analog circuitry. **Figure 27** shows a different arrangement. The concept is the same as for Figure 26, except that the analog regulators are on the same side of the cut as the analog circuitry.

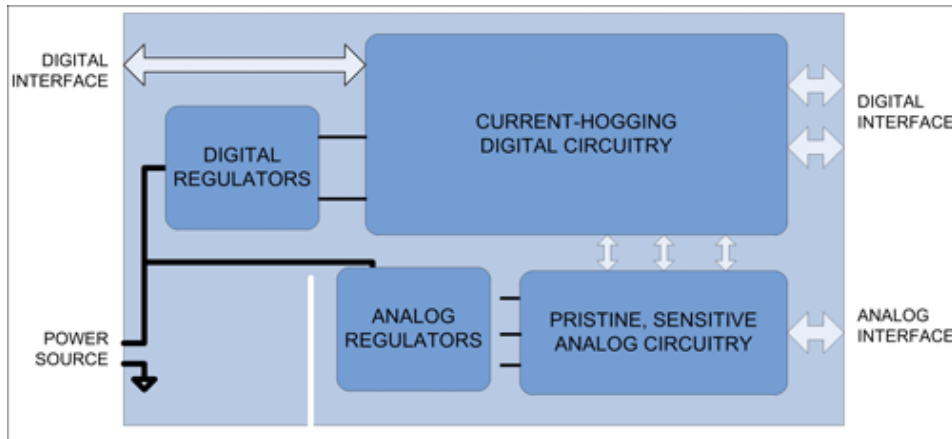


Figure 27. The same board with the analog regulators moved.

Sometimes there will be noisy switching regulators followed by filtering and low-noise linear regulators for the analog circuitry. Similar thinking is employed to decide where the noisy switching regulators are placed, always considering where the currents will flow.

Another situation that board-level designers increasingly encounter is the signal integrity of high-frequency signals. As frequencies get higher into the GHz range, we find crosstalk between traces that run close and parallel to each other. This makes things more complicated. As we have learned earlier, in the simple case of a single trace over a ground plane and as seen in Dr. Archambeault's simulation for 1MHz signals (Figure 12), the return currents are not contained within the area directly under the signal traces but are much wider. It is easy to see how close parallel traces will have their return currents comingle. As the frequencies increase and the traces become a more significant percentage of a wavelength, the signals are more likely to corrupt each other.⁵

Conclusion—Pay Attention to Where the Current Flows

Many problems with mixed-signal PCB design can be avoided by following this simple advice: pay attention to where the current flows. For most cases all we have to do is remember two basic principles: DC and low frequencies flow mostly in the straight-line path of least resistance between source and load; and high-frequency signals follow the path of least impedance, which is directly under the signal trace. In-between frequencies flow by both paths and in between the two paths.

The idea of using cuts to prevent interaction between different circuits is most often unnecessary, as long as we wisely place components and route traces to prevent this from happening. Sometimes a ground plane cut is needed because we are not always free to choose where components are placed. Again, place the cut wisely, considering all the current flows. We also must remember that no signal should ever cross a cut on any layer.

Keep track of where those pesky electrons want to flow and you will make your job a lot easier. Finally, remember that, "while you can always trust your mother, you should never trust your 'ground.'"⁶

Citations

1. In an ideal world, this would be all that we would need to understand. The ideal world does not exist or,

at least, the one we are dealing with seems not to be ideal.

2. Ott, Henry W., **Electromagnetic Compatibility Engineering**, John Wiley and Sons, Hoboken, NJ, 2009. p 393.
3. Archambeault, Bruce, **IEEE® EMC Society Newsletter**, Fall 2008, Issue 219, "[Part II: Resistive vs. Inductive Return Current Paths](#)," pp 81-83.
4. Ott, p 392
5. This extremely important subject is beyond the scope of this article but is well covered in the references and many other books on signal integrity.
6. Brokaw, Paul, "An IC Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change," Analog Devices application note AN-202.

References

1. Application note 4636, "[Avoid PC-Layout 'Gotchas' in ISM-RF Products](#)."
2. Johnson, Howard W., Ph.D. and Graham, Martin, Ph.D., **High-Speed Digital Design: A Handbook of Black Magic**, Prentice-Hall, Upper Saddle River, NJ, 1993.
3. Ott, Henry W., **Electromagnetic Compatibility Engineering**, John Wiley and Sons, Hoboken, NJ, 2009.

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