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TUTORIAL 5283

PCB Design Considerations and Guidelines for 0.4mm and 0.5mm WLPs

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Abstract: Using a wafer-level package (WLP) can reduce the overall size and cost of your solution. However when using a WLP IC, the printed circuit board (PCB) layout can become more complex and, if not carefully planned, result in an unreliable design. This article presents some PCB design considerations and general recommendations for choosing a 0.4mm- or 0.5mm-pitch WLP for your application.

A similar version of this article appeared in Korean on [EE Times Korea](#), December 8, 2011.

Introduction

When designing a system-level circuit, printed circuit board (PCB) real estate can come at a premium. One method of reducing a design's required PCB area is to use a smaller IC package, such as a wafer-level package (WLP). This can free up a lot of area on your PCB and can also save you in cost, if you plan accordingly.

WLPs are much smaller than their predecessors because the package is built up directly on the silicon substrate and no bond wires are used. This in turn saves cycle time and packaging costs. However, to keep PCB costs at a minimum, some layout considerations need to be taken. This tutorial will present some general PCB layout guidelines to follow when using WLPs. These guidelines are provided as an aid for developing a PCB layout design to increase the chance that your design can be reliably manufactured.

Note: $1\text{mil} = 1/1000\text{in} = 0.0254\text{mm}$

SMD and NSMD Pads

Before any routing is started, the first consideration should be the design of the WLP footprint. The WLP drawing will provide most of the information (package dimensions, tolerances, pin-pitch) needed to create the PCB footprint. Another aspect to consider when creating the WLP footprint is the type of pad to use for the IC pins. The pad options are solder mask defined (SMD) and nonsolder mask defined (NSMD), both shown in **Figure 1**.

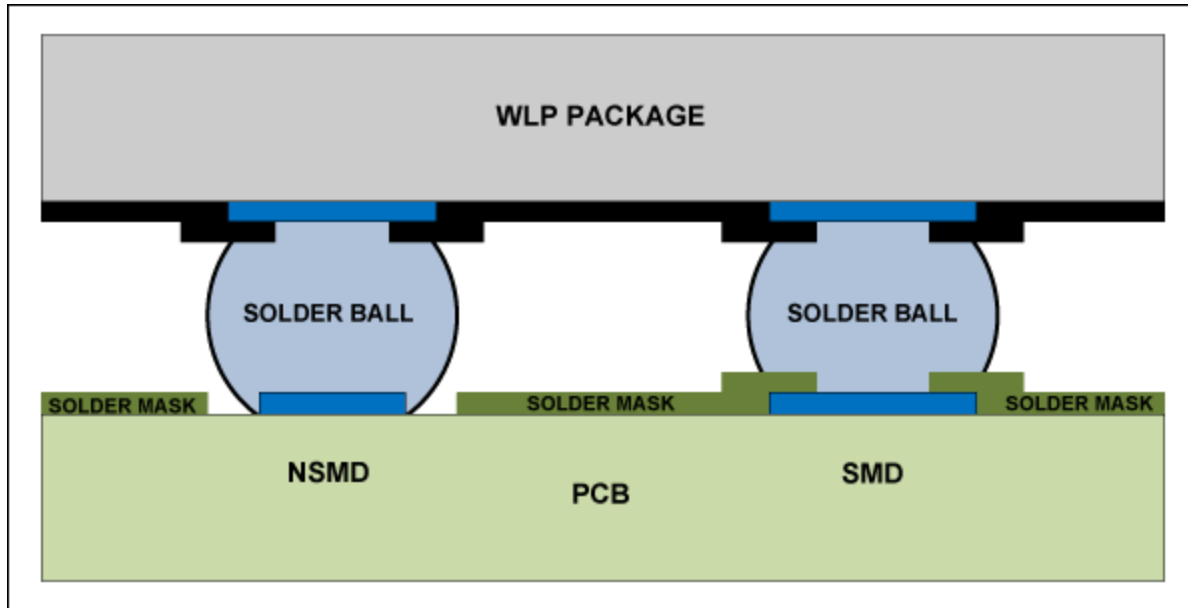


Figure 1. When creating the WLP footprint, consider the type of pad you want to use for the IC pins, either the solder mask defined (SMD) or the nonsolder mask defined (NSMD).

The SMD pad uses, as the name suggests, a solder mask to define the pad area to which the solder ball will be soldered. This method reduces the likelihood of the pad lifting during the soldering or desoldering process. The disadvantage, however, is that this method reduces the amount of copper surface area available for the solder ball connection, and reduces the space between adjacent pads. This limits the thickness of the traces between pads and may affect the use of vias.

The NSMD pad uses copper to define the pad area to which the solder bump will be soldered. This method provides a larger surface area for the solder ball connection and provides more clearance (compared to SMD) between pads, allowing for wider trace widths and more flexibility in the use of vias. The downside of this method is that it is more susceptible to pad lifting during the soldering and desoldering processes.

The most recommended pad type is NSMD. This pad type lends itself to a better solder connection, allowing the solder joint to encapsulate the pad. When starting a PCB design with WLPs, both pad types should be considered and their pros and cons weighed with the target application in mind. Note that both methods can be used on a single WLP footprint.

Pitch Size

Maxim offers a wide array of WLP ICs that are available in a 0.4mm or 0.5mm pitch. The pitch size refers to the distance between the solder balls (i.e., pins) on the IC. The distance is measured from center-to-center of two adjacent solder balls. The larger the pitch, the more space there is between pads to route traces.

A 0.5mm-pitch design offers a little more breathing room than its smaller counterpart, the 0.4mm. The 0.5mm pitch gives you approximately 19.7 mils of space between solder balls from center-to-center. A typical pad size is 8.7 mils, giving you 11 mils between pads to route traces. Using a trace-to-solder-ball clearance of 3.5 mils, you can comfortably fit a maximum trace width of approximately 4 mils between

two defined solder ball pads. With a 4-mil trace using 1oz copper (Cu), you are limited to approximately 220mA current through the trace. With 2oz Cu, you can drive 380mA through a 4-mil trace. The spacing and dimensions for a 0.5mm-pitch WLP are shown in **Figure 2**. For an example of a 0.5mm-pitch WLP PCB layout, refer to the [MAX8896 evaluation \(EV\) kit data sheet](#) on Maxim's website.

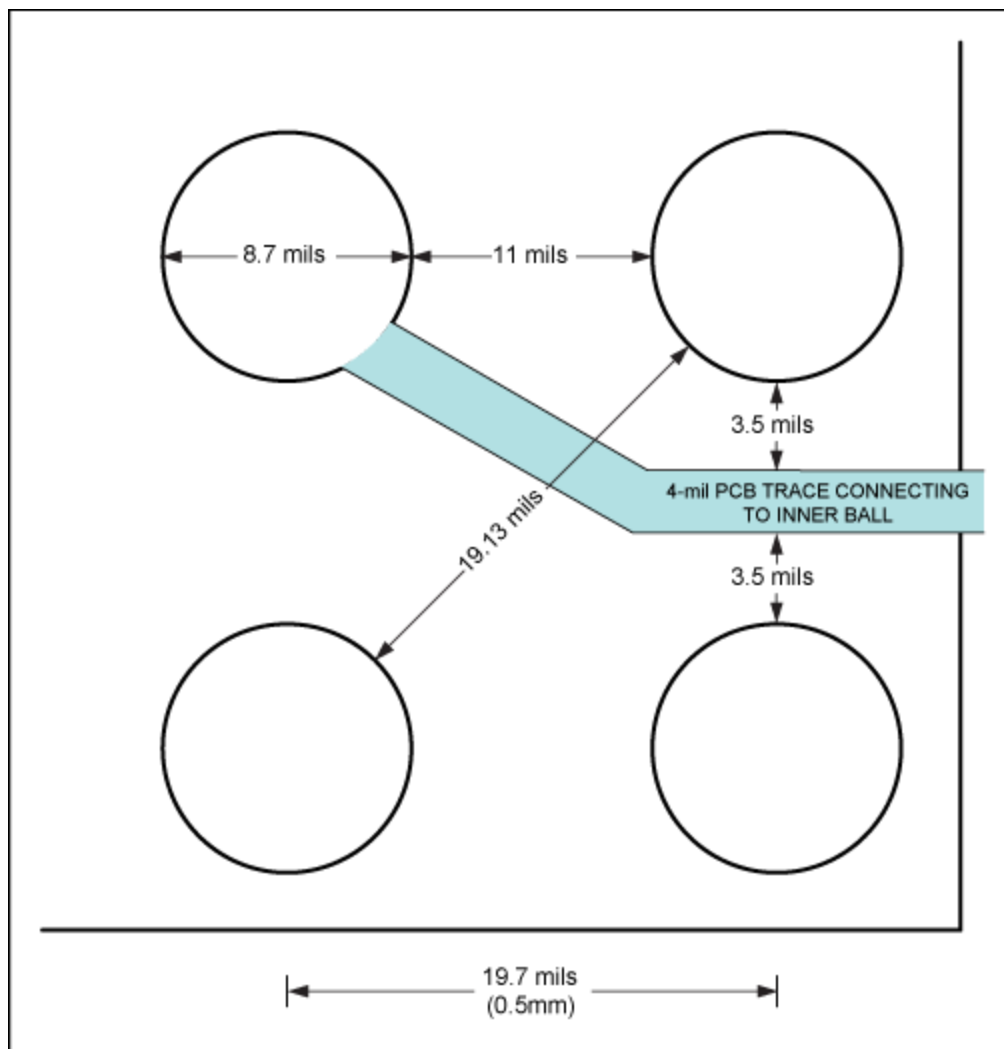


Figure 2. Spacing and dimensions for a 0.5mm-pitch WLP.

A 0.4mm (15.7-mil) pitch design can be a bit trickier than a 0.5mm design. There is a lot less space to route traces between solder balls, which means more restriction and less flexibility. A typical pad size is 7 mils, leaving you with 8.7 mils between pads to route traces. When using a 3-mil space on each side of an inner trace, you are only left with a maximum trace width of ~2.7 mils. The spacing and dimensions for a 0.4mm-pitch WLP are shown in **Figure 3**. With a 2.7-mil trace using 1oz copper (Cu), you are limited to approximately 160mA current through the trace. For smaller pitch such as 0.4mm, using thicker copper can be a concern, since the trace width is less than the copper width (e.g. 2oz Cu = 2.8 mils). This can result in a net trace width of less than 2.7 mils after the etching/plating process. **Table 1** provides a recommendation of trace width to copper thickness from a common PCB fab house.

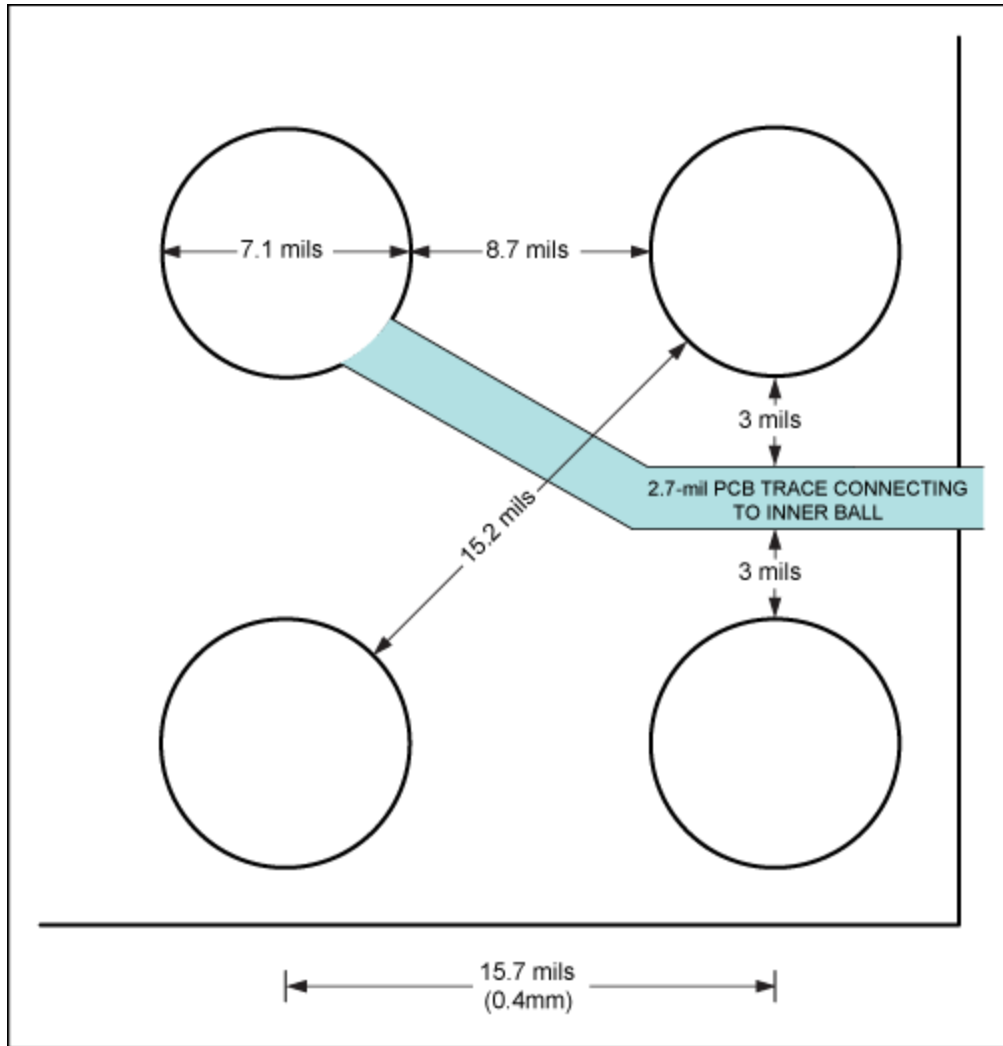


Figure 3. Spacing and dimensions for a 0.4mm-pitch WLP.

Table 1. Recommended Trace Widths		
Copper Weight	Copper Thickness	Recommended Trace Width
0.5oz	0.7 mils	3 mils to 5 mils
1oz	1.4 mils	4 mils to 7 mils
2oz	2.8 mils	8 mils to 10 mils

Routing Alternatives

If using a thinner trace between WLP pads does not work for your design, as is such for smaller-pitch WLPs (i.e., 0.3mm), other options can be used, but they each have their own disadvantages. One option is to use a laser-drilled via, which comes at a premium PCB cost. A laser-drilled via is needed because mechanical drills have equipment limitations (like a 10-mil minimum drill-bit size), and because of the spacing constraints between adjacent and diagonal pads of the WLP IC footprint. Laser-drilling is a PCB

fab process where a via is laser-drilled directly into or offset from the WLP pad and then refilled, allowing a trace to be run on an inner layer. If you have an application where the PCB already uses a laser-drilled via (such as high-end audio applications or cell phones), then the PCB cost may not be an issue. However, if you have an application where the PCB must be lower cost (like for some LCD displays), then the extra cost may not be justified.

Another less common alternative is to use a staggered-bump-array WLP. By staggering the balls on the WLP chip, you can create more room to route larger traces. Not all WLP chips offer the luxury of staggered bump arrays, and this will need to be carefully planned during the initial stages of your design. Alternatively, you can use a WLP bump array that is missing a few inner/outer pins. This will also give you more space to either drop in a via or route a larger trace to the inner layers. Again this will need to be carefully thought out very early in your design, while also considering any possible second source requirements for your part.

Conclusion

In this tutorial, some basic guidelines and design considerations have been presented to aid in the design of a PCB layout when using 0.4mm- and 0.5mm-pitch WLP ICs. The pad type (SMD and NSMD), allowable maximum trace widths between pads, and alternatives to routing between pads (laser vias, staggered-array WLP, etc.) have been discussed to raise awareness when designing with WLPs.

Related Parts

[MAX8896EVKIT](#)

Evaluation Kit for the MAX8896

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