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Parasitic Inductance Effects in the Design of 10Gbps Optical Transmitters

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1 Introduction

Successful 10Gbps optical transmitter design demands careful attention to the sources and effects of parasitic inductance. The addition of even 0.1nH of inductance can cause significant degradation to the rise/fall times, overshoot/ringing, and jitter in the optical output (for reference, a 0.5mm bond wire adds approximately 0.4nH).

Figure 1 is a simplified block diagram of the output stage of a laser driver connected to a laser diode. In the actual system there are many distributed parasitic inductances due to bond wires, die pads, etc. For simplicity, in the model of Figure 1, the distributed inductances have been lumped into two locations; L_{OUT} at the output of the driver (cathode of the laser diode), and L_{ANODE} at the anode of the laser diode. The transient behavior of the switching current due to the inductors affects the optical output of the laser diode in a number of ways.

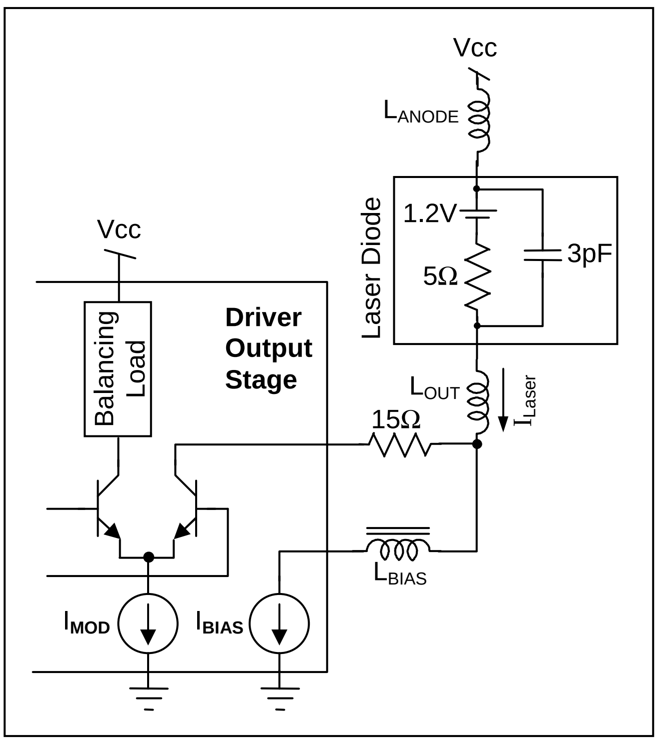

Figure 1. Simplified model of a laser driver connected to a laser diode

2 Voltage Headroom

The driver modulation output transistor requires a minimum specified voltage in order to switch properly. An example requirement is for a minimum of 1.55V at the modulation output. Operating below the minimum will cause sub-optimal transistor switching that will result in increased jitter and other distortions to the optical output. Parasitic inductance can play a major role in decreasing voltage headroom during switching.

For example, assume V_{CC} = 5V, I_{BIAS} = 20mA, and I_{MOD} = 60mA in the model of Figure 1. In steady state, the voltage at the output will be 5V – 1.2V – (20+60mA)(5Ω) - (60mA)(15Ω) = 2.5V, which is above the 1.55V minimum requirement. During switching, however, the voltage drop across the inductors is L di/dt. If we assume L_{OUT} = L_{ANODE} = 0.5nH and that the 20%-80% rise time is 25ps (i.e., a 60% change in current in a 25ps time period), then the approximate total transient voltage drop across the inductors is 2 × 0.5nH × (.6)(60mA) / 25ps = 1.44V. When this transient voltage drop is subtracted from the steady state output voltage, the resulting 1.06V is well below the required minimum of 1.55V.

3 Rise/Fall Times

If we neglect the effects of parasitic capacitance and assume a greatly simplified single time constant (STC) model, then the rise and fall times can be calculated using the L/R time constant. For a 20%-80% rise time we can use the relationship $2\pi\tau \approx t_{rise}/0.22$ (where τ = L/R represents the time constant) to calculate a value for L. If we let R = 20Ω, then $L \approx 14.5 \times t_{rise}$. Using this relation with a typical 10Gbps rise time of 25ps results in L ≈ 0.36nH. While this result is far from exact (it is based on a greatly simplified model) it gives a good idea of the approximate level of inductance that can be tolerated without significantly affecting the rise/fall times.

4 Overshoot and Ringing

If we include parasitic capacitance to the model in Figure 1, we can use basic control theory to predict overshoot and ringing that result from an overdamped or underdamped LRC circuit. To eliminate overshoot and ringing, the circuit must be critically damped, where $R_{critical} = 2\sqrt{\frac{L}{C}}$. From this equation we can see that as the parasitic inductance increases, the critical resistance will also increase.

Assuming that the actual resistance stays constant, increasing the inductance will result in an increasingly underdamped system and increase the overshoot and ringing. On the other hand, if the resistance is increased to match the critical resistance criteria, the headroom will be negatively impacted. This means that, in order to meet the headroom requirements and keep the circuit critically damped, the parasitic inductance must be minimized.

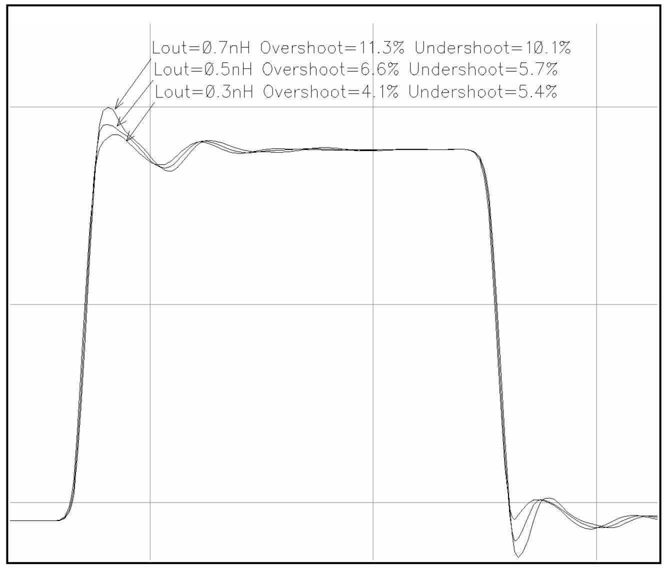

Figure 2. Simulated laser current vs. L_{out}

5 Simulation Results

Computer simulation using a detailed model (more complex than the one shown in Figure 1) illustrates the effects of various values of parasitic inductance on rise time, fall time, overshoot, undershoot, and deterministic jitter. Figure 2 is one example of simulation results for three different values of L_{OUT}. Table 1 summarizes the numerical results of the simulations using various values of L_{OUT} while keeping L_{ANODE} constant. For reference, a 0.5mm length of bond wire represents approximately 0.4nH of parasitic inductance, while a 1mm length adds approximately 0.8nH.

The simulation results demonstrate that precise understanding and strict control of the electrical parasitic environment in every part of the 10Gbps transmitter system is critical to success in module design and development.

Table 1. Simulation with varied L_{OUT}

L_{OUT} = L_{ANODE} =	0.3nH 0.25nH	0.5nH 0.25nH	0.7nH 0.25nH
Rise Time	29.0ps	27.1ps	27.0ps
Fall Time	28.4ps	26.8ps	26.7ps
Overshoot	4.1%	6.6%	11.3%
Undershoot	5.4%	5.7%	10.1%
Det. Jitter	3.0ps	3.54ps	4.3ps