



## Abstract

Cable access is evolving at a rapid pace to keep up with consumers' thirst for bandwidth. With the advent of Full-Duplex DOCSIS (FDX), multiple-system operators (MSOs) are struggling to find solutions which will allow them to add functionality and features while maintaining system performance as measured by modulation error ratio (MER) and bit error ratio (BER) and also improving power efficiency (or staying within their power limitations). To support such needs, an open-loop cable digital predistortion (DPD) system is described in this paper, where MER and BER improvements are demonstrated, as well as a 24% efficiency improvement in power.

## Introduction

One of the biggest challenges for cable service providers is their ability to quench the thirst of their customers for increased bandwidth. Network capacity is a major concern for their ability to meet this increased demand and stay competitive vis-à-vis alternate technologies like fiber or fixed wireless. As a result, cable access technologies have been evolving at a rapid pace, with FDX nipping at the heels of DOCSIS 3.1.

The primary objective of FDX is to increase system capacity and provide upstream bandwidths that can be throttled up to half the bandwidth currently available for downstream in DOCSIS 3.1. Thus, the name of Full Duplex, where the available bandwidth between upstream and downstream is now balanced and flexible. See Figure 1 for the spectrum details.



*Cable service providers are striving to meet increasing demand for bandwidth*

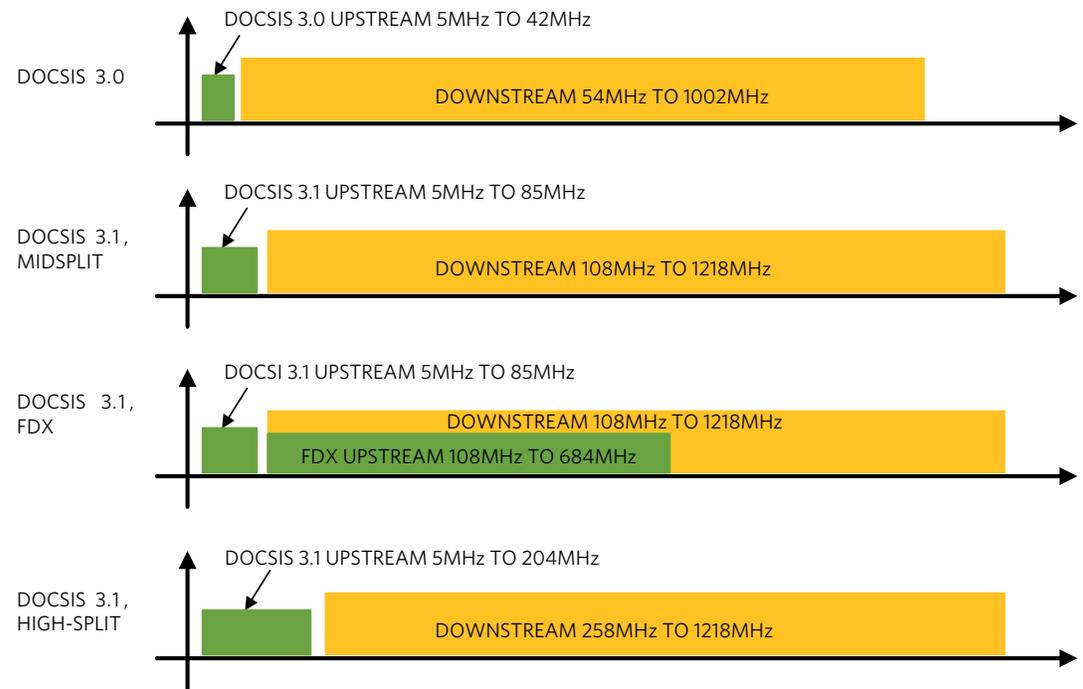


Figure 1. DOCSIS and FDX frequency band evolution.

Of course, in order to achieve such upstream and downstream speeds, the legacy hybrid fiber-coaxial (HFC) network architecture will need to be modified. Legacy HFC networks cannot support the required performance of DOCSIS 3.1 and, instead, distributed architectures via remote physical layer (PHY) and remote medium access control (MAC)/PHY are needed. With this change in architecture, a fiber deep (node+0) will extend the digital network closer to the subscribers. See Figure 2 for these architecture changes.

While they are able to support the additional bandwidth, these distributed architectures come with their own sets of challenges. Since a higher power amplifier (PA) output is required for the longer distances, both increased power dissipation and signal quality will need to be addressed.

## Broadband, High PAR, and Tilt

In order to reach the cable distances needed, downstream PAs are driven way past their linear region. That does allow for better efficiency (versus a fully linear PA), but at a high cost of signal quality degradation. A tried-and-true method in the wireless world to improve signal linearity is DPD. DPD in the cable world differs in that the bandwidth to linearize is ~1.2GHz wide (unlike the ~100MHz in the cellular world) and has an instantaneous peak-to-average ratio (PAR) of ~16dB. The DPD algorithm will need to contend with improving both BER degradation due to hard clipping and MER degradation.

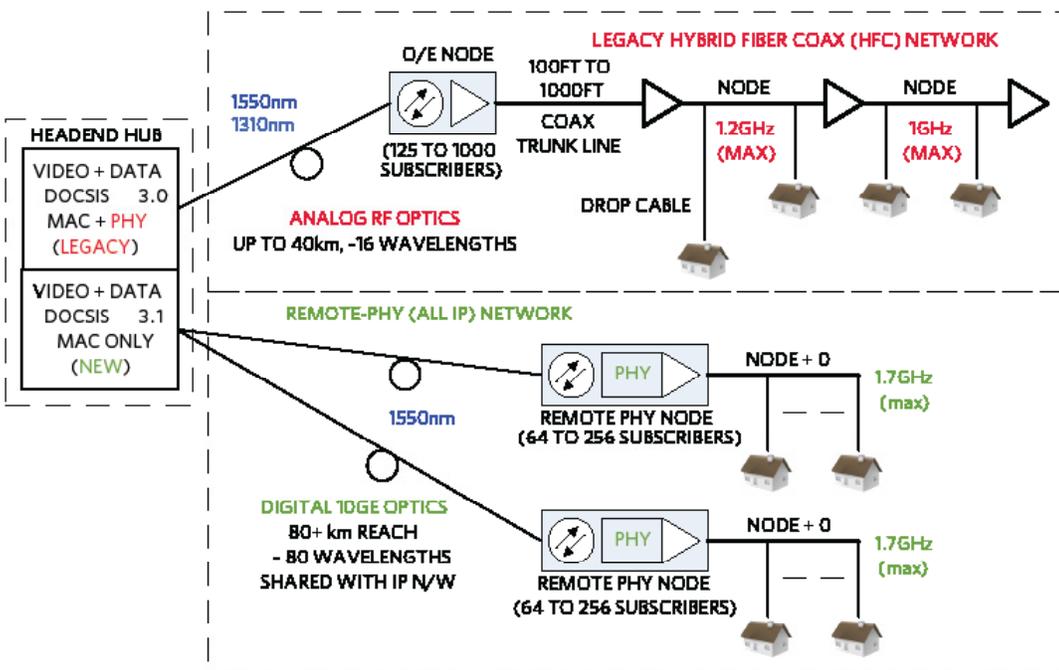
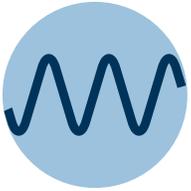


Figure 2. HFC to remote PHY networks.



*BER and MER are key metrics for gauging a DPD solution's performance*

Another challenge of the architecture is the frequency-dependent loss in the coax cable. For example, in a 350-foot RG6 cable segment, there is about a 20dB difference of loss from 54MHz to 1218MHz. Analog up-tilt equalizers are used to compensate for this cable loss.

## RPD RF Path Block Diagram

Below is a block diagram of the remote PHY device (RPD) RF path. The output from a single RF digital-to-analog converter (RF-DAC) is typically split into four separate PAs, each capable of delivering 76.8dBmV of composite power into the cable. In order to maintain equivalent paths, these PAs should be well balanced so that all four PAs can share a common predistorted signal source.

## Performance Requirement

The performance of any DPD solution will be measured by BER and MER. While efficiency improvement is quite important, it cannot come at the expense of MER or BER degradation.

A typical list of requirements is provided below:

- TCP: 76.8dBmV (73.8dBmV at F-connector)
- Tilt: > 21dB
- Efficiency improvement: +20%
- 256QAM/B: pre-RS BER < 1e-8, MER > 41 dB
- DOCSIS3.1: modulation-order dependent, MER > 45 dB for 4096QAM

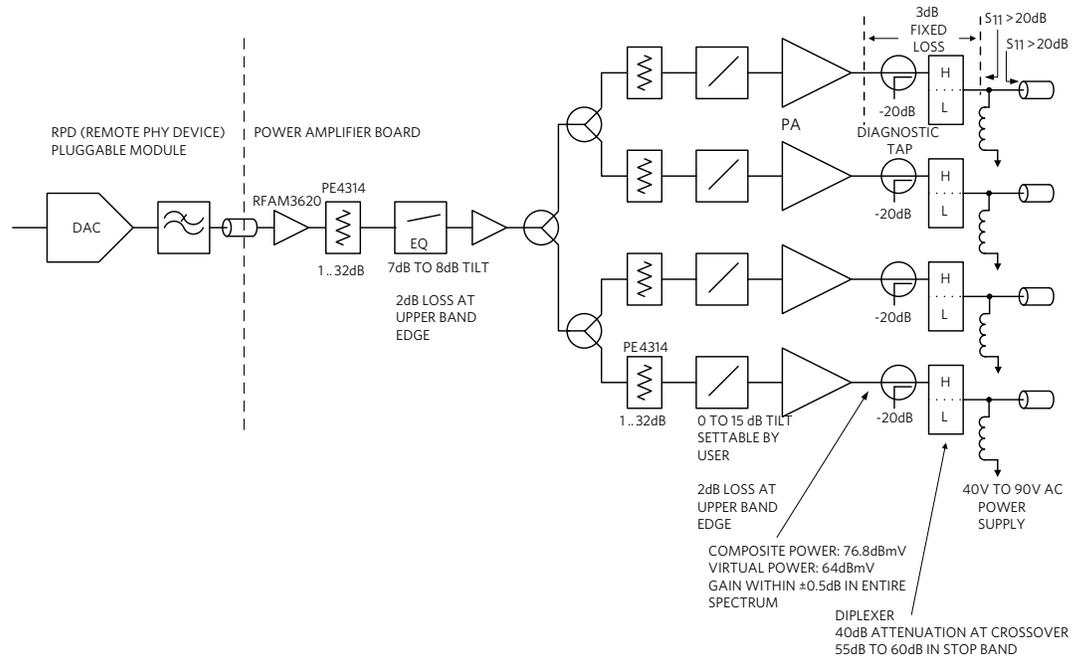


Figure 3. RPD RF path.

## Open-Loop DPD Algorithm

In the following plots, the results of Maxim's DPD implementation are presented with a commercially available PA. MER measurements were taken with the MAXPACS system. This system, which allows for the generation of the DPD-IP coefficients, contains an RF-DAC and RF analog-to-digital converter (RF-ADC) system, along with the software and MATLAB processing. A signal, from 108MHz to 1218MHz, is loaded into a data source for the RF-DAC to transmit. The signal then goes through the RPD RF path from the pre-amp, equalizer, and through the PA and 350-ft RG6 cable segment for RF-ADC system capture. It is important that the signal power levels are set appropriately through this data path to result in the expected power and tilt at the output of the PA. This signal is analyzed to determine the required coefficients for the DPD algorithm. With the coefficients loaded into the data source, the signal would then be predistorted to account

for the non-linearities of the PA. This improvement on the signal then allows for the PA power to be reduced yet provide similar performance to the full power with distortion.

The generated coefficients are then loaded into the DPD-IP core registers that reside in an FPGA design. Resource usage and power dissipation impose a limit on the complexity of the DPD implementation. The current implementation would cost ~3.6W in FPGA power. The result is the predistorted data provided to the RF-DAC in the signal chain, such as the [MAX5850](#) (14-bit 3072Msps RF-DAC supporting the RPD structure). With a real data path and the DPD-IP core, the BER measurement can be captured for performance comparison.

## MER Measurements

In Figure 4, MER results for eight PAs are plotted versus frequency. With a full bias of 530mA, the MER improves 3dB to 7dB depending on the frequency, enabling us to reduce the bias and save power, while maintaining the same MER, as shown in Figure 5.

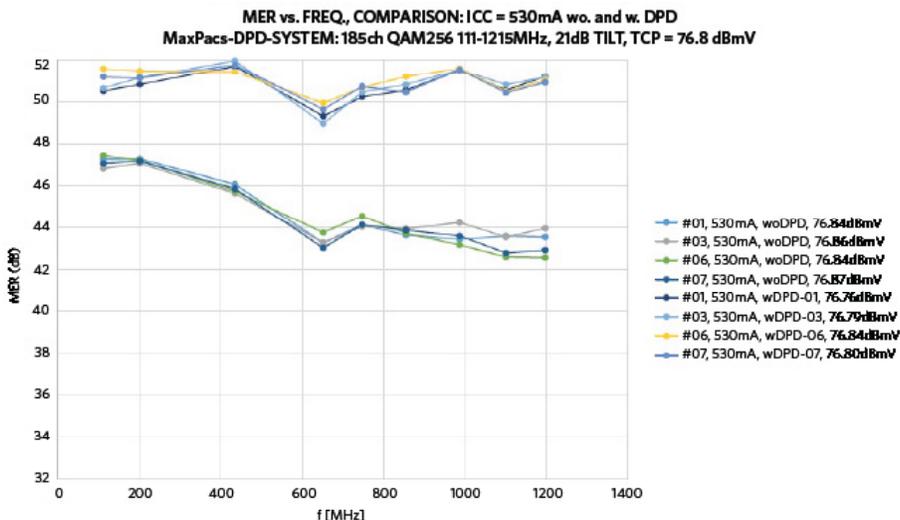
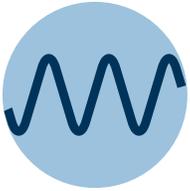


Figure 4. MER measurements – full bias.

In Figure 5, we are able to reduce the bias current of the PA down to 400mA with DPD, and the MER is improved from an unacceptable ~37db back to 44db, thus improving efficiency by 24%.

This measurement reveals the benefits of the Maxim DPD on the MER.



*A DPD solution can reduce bias current and improve MER*

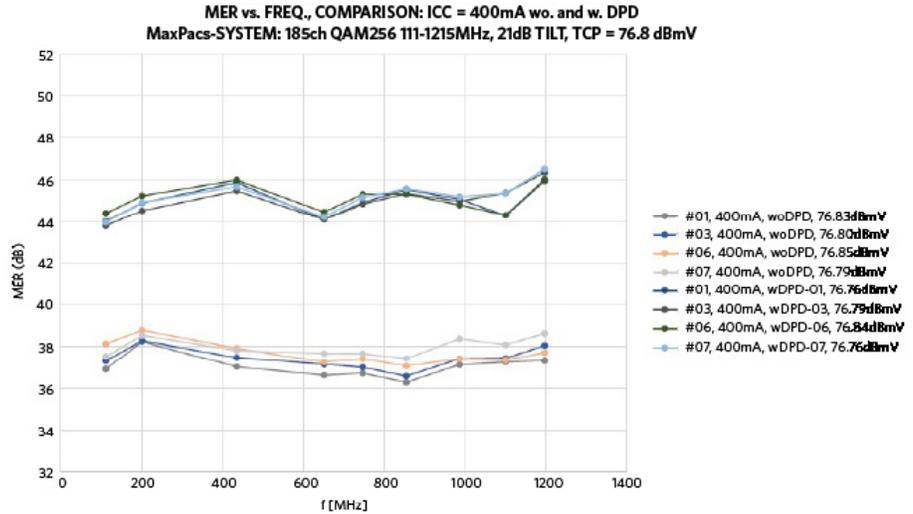


Figure 5. MER measurements – reduced bias.

Figure 6 summarizes the MER measurements for full bias without DPD and the reduced bias of 400mA with DPD.

This demonstrates the comparable performance of the original signal to the DPD signal at a much lower power consumption.

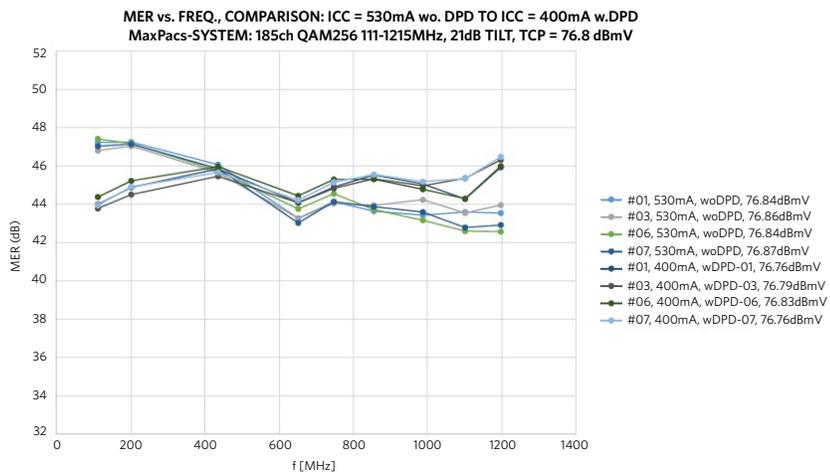


Figure 6. MER measurements – full versus reduced.

## BER Measurements

To obtain BER measurements, the RF-DAC data source must be a 'real' data set. Maxim was able to make use of an industry leader's FPGA design to feed the RF-DAC data, enabling the critical BER measurements. The FPGA design was limited in digital resources and, therefore, in QAM channel capacity. As a result, the BER testing was conducted with a gap in the spectrum between 396MHz and 738MHz. Figure 7 shows the results of this BER measurement under the same 400mA reduced bias conditions as the MER plot. Note: for logarithmic plotting, a zero value in the pre-RS BER value is presented as 1E-11 in the plot. As can be seen, the worst-case BER value is improved by 10x when running the DPD-IP.

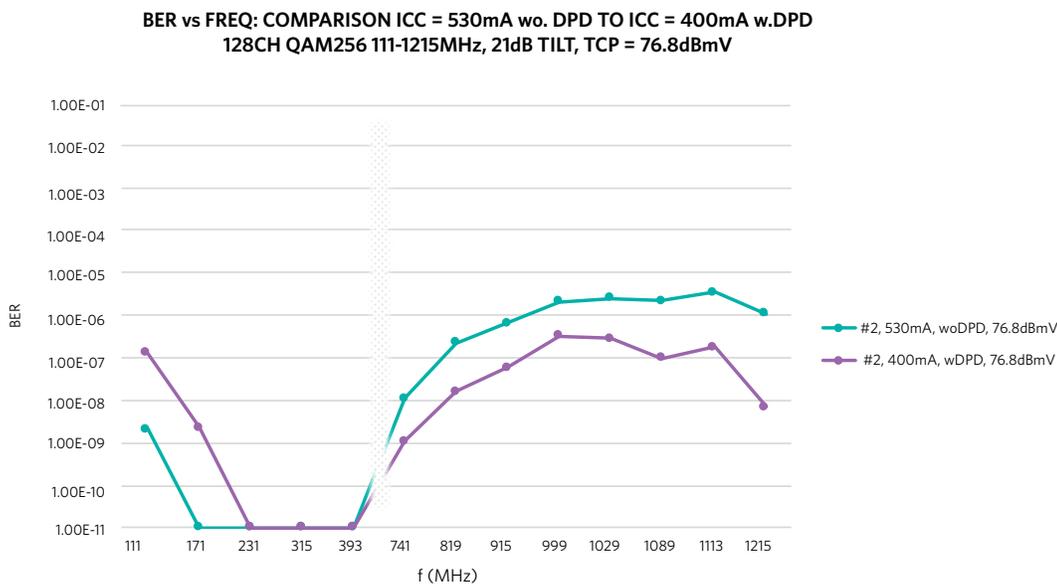


Figure 7. BER results - full versus reduced.

## Conclusion

With the added pressures of higher performance and better power efficiency, Maxim's DPD solution allows customers to beat MER and BER requirements, while achieving 24% or better efficiency on their PAs. With the RDP path often containing four PAs within the system, the efficiency adds up to a tremendous power savings. This allows more power budget for the other complexities of the FDX architecture or simply just power savings within the system. And because it is an open-loop solution, it provides this at a lower cost of competitive solutions.

For more information, visit:  
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