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APPLICATION NOTE 6826

HOW TO PROGRAM STARTUP AND SHUTDOWN SEQUENCE WITH MAX77812

Abstract: The MAX77812 is a quad-phase, high-current, step-down (buck) converter for high-end gaming consoles, VR/AR headsets, DSLR cameras, drones, network switches and routers, and FPGA systems that use multicore processors. The MAX77812 has factory-programmable OTP (one-time programmable) options for customizing the startup sequence and separate register sets for the shutdown sequence. This document explains how to program those registers and provides an example.

Introduction

The MAX77812 supports programmable startup and shutdown between the master phases. The startup and shutdown sequence is initiated by either the EN pin or GLB_EN function of GPIs. The startup and shutdown delay times between the master phases are programmable from 0ms to 62ms (32 steps) with a 1ms/2ms delay time step.

Startup and Shutdown Sequence Setting

The startup sequence is set by STUP_DLYx registers and the default values are factory-programmed options (see the Ordering Information section in the data sheet for details), while the default values of shutdown delay registers (SHDN_DLYx) are fixed, having no delay time between the master phases by default.

While the CE pin is high (standby mode), the user can override both startup and shutdown registers through a serial interface.

Note that the M1 (Master 1) is always turned on as soon as a startup sequence is initiated—there is no programmable delay.

In case any master phase is turned on by the EN_Mx bit or Mx_EN function of GPI0/1 before initiating startup or shutdown sequence, a startup or shutdown event is transparent to the master phase already turned on.

For example, if we want to have 10ms of delay time between the master phases in 1+1+1+1 phase configuration, STUP_DLYx registers can be programmed as below (with register programming details in Table 1 through Table 7):

- Delay time step: 1ms by setting DLY_STEP = 0
- Delay time from M1 to M2: 10ms by setting M2_STUP_DLY[4:0] = 01010b
- Delay time from M1 to M3: 20ms by setting M3_STUP_DLY[4:0] = 10100b
- Delay time from M1 to M4: 30ms by setting M4_STUP_DLY[4:0] = 11110b

The diagram in Figure 1 shows a typical startup and shutdown sequence.

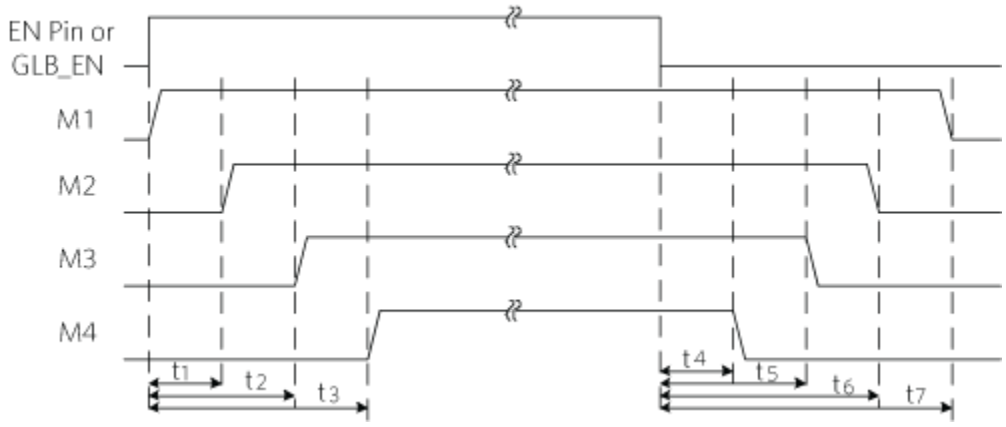

Figure 1. Startup and shutdown sequence.

Table 1. STUP_DLY1 Registers

Address 0x07	Mode R/W	Type: O	Reset Value: 0x00 (OTP)
Bit	**Name**	**POR**	**Description**
7	DLY_STEP	0	Delay Time Step Selection 0: 1ms 1: 2ms
6:5	RESERVED	00	
4:0	M2_STUP_DLY[4:0]	0 0000	Buck Master 2 Startup Delay Time Setting (Delay from Rising Edge of EN Pin or GLB_EN) **0 0000b = 0ms** 0 0001b = 1 x DLY_STEP 0 0010b = 2 x DLY_STEP . . . . . . 1 1110b = 30 x DLY_STEP 1 1111b = 31 x DLY_STEP

Table 2. STUP_DLY2 Registers

Address 0x08	Mode R/W		Type: O	Reset Value: 0x00 (OTP)
Bit	**Name**	**POR**	**Description**	
7:5	RESERVED	000		
4:0	M3_STUP_DLY[4:0]	0 0000	Buck Master 3 Startup Delay Time Setting (Delay from Rising Edge of EN Pin or GLB_EN) **0 0000b = 0ms** 0 0001b = 1 x DLY_STEP 0 0010b = 2 x DLY_STEP . . . . . . 1 1110b = 30 x DLY_STEP 1 1111b = 31 x DLY_STEP	

Table 3. STUP_DLY3 Registers

Address 0x09	Mode R/W		Type: O	Reset Value: 0x00 (OTP)
Bit	**Name**	**POR**	**Description**	
7:5	RESERVED	000		
4:0	M4_STUP_DLY[4:0]	0 0000	Buck Master 4 Startup Delay Time Setting (Delay from Rising Edge of EN Pin or GLB_EN) **0 0000b = 0ms** 0 0001b = 1 x DLY_STEP 0 0010b = 2 x DLY_STEP . . . . . . 1 1110b = 30 x DLY_STEP 1 1111b = 31 x DLY_STEP	

Table 4. SHDN_DLY1 Registers

Address 0x0A	Mode R/W		Type: O	Reset Value: 0x00 (OTP)
Bit	**Name**	**POR**	**Description**	
7:5	RESERVED	000		
4:0	M1_SHDN_DLY[4:0]	0 0000	Buck Master 1 Shutdown Delay Time Setting (Delay from Falling Edge of EN Pin or GLB_EN) **0 0000b = 0ms** 0 0001b = 1 x DLY_STEP 0 0010b = 2 x DLY_STEP . . . . . 1 1110b = 30 x DLY_STEP 1 1111b = 31 x DLY_STEP	

Table 5. SHDN_DLY2 Registers

Address 0x0B	Mode R/W		Type: O	Reset Value: 0x00 (OTP)
Bit	**Name**	**POR**	**Description**	
7:5	RESERVED	000		
4:0	M2_SHDN_DLY[4:0]	0 0000	Buck Master 2 Shutdown Delay Time Setting (Delay from Falling Edge of EN Pin or GLB_EN) **0 0000b = 0ms** 0 0001b = 1 x DLY_STEP 0 0010b = 2 x DLY_STEP . . . . . . 1 1110b = 30 x DLY_STEP 1 1111b = 31 x DLY_STEP	

Table 6. SHDN_DLY3 Registers

Address 0x0C	Mode R/W		Type: O	Reset Value: 0x00 (OTP)
Bit	**Name**	**POR**	**Description**	
7:5	RESERVED	000		
4:0	M4_SHDN_DLY[4:0]	0 0000	Buck Master 4 Shutdown Delay Time Setting (Delay from Falling Edge of EN Pin or GLB_EN) **0 0000b = 0ms** 0 0001b = 1 x DLY_STEP 0 0010b = 2 x DLY_STEP . . . . . . 1 1110b = 30 x DLY_STEP 1 1111b = 31 x DLY_STEP	

Table 7. SHDN_DLY4 Registers

Address	Mode		
0x0D	R/W	Type: O	Reset Value: 0x00 (OTP)
Bit	**Name**	**POR**	**Description**
7:5	RESERVED	000	
4:0	M3_SHDN_DLY[4:0]	0 0000	Buck Master 3 Shutdown Delay Time Setting (Delay from Falling Edge of EN Pin or GLB_EN) **0 0000b = 0ms** 0 0001b = 1 x DLY_STEP 0 0010b = 2 x DLY_STEP . . . . . . 1 1110b = 30 x DLY_STEP 1 1111b = 31 x DLY_STEP

Related Parts		
MAX77812	20A User-Configurable Quad-Phase Buck Converter	Samples

More Information
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