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APPLICATION NOTE 6609

# HOW TO OPTIMIZE USE OF CONTROL ALGORITHMS IN SWITCHING REGULATORS

*Abstract: In this application note, we'll examine three basic control algorithms for switching regulators. We'll discuss pros and cons of each and provide guidance on the right loop compensation strategy to obtain a fast and stable response.*

*A similar version of this application note appeared on Power Electronics on December 28, 2017.*

## Introduction

Since at least the 17th century, we've had feedback control schemes for linear systems. They've been used to regulate pressure and distance between millstones and then, famously, to control James Watt's steam engines. These earlier techniques apply to the control of linear voltage regulators used today. When it comes to power conversion today, switching technology is the preferred option. That's why it's important to consider controlling output voltage, typically with pulse-width modulation (PWM) techniques. This application note examines three common control methods—constant on-time, voltage mode, and current mode—along with their pros, cons, and implementations.

## The Easiest Control Method: Constant On-Time

Constant on-time may be the simplest control method used in a buck converter circuit. This method provides bursts of energy for fixed periods to the output. To maintain constant output voltage, the repetition rate of the bursts is varied. **Figure 1** depicts a one-shot, or monostable, which provides the fixed-length pulse, causing current in the output inductor to rise linearly from its average DC value and charging the output capacitor. Following the pulse, the capacitor voltage drops. By initiating the next on-pulse when the voltage drops below a reference value, we can effectively regulate the output voltage, with light loads producing longer off-times. With its positive feedback, the circuit acts like a power oscillator, so it's sometimes called a "bang-bang" or "ripple" regulator. Because of the variable off-time, the circuit is inherently variable frequency.

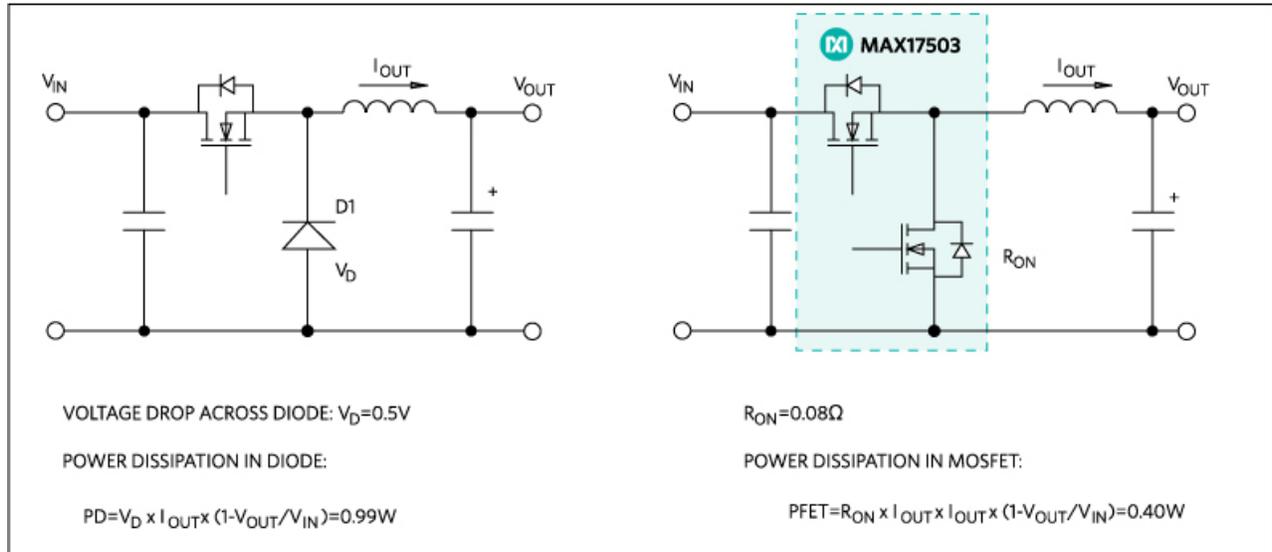


Figure 1. Constant on-time control.

Since this method comes without negative feedback, loop compensation is not needed, and the circuit can react immediately to load changes. Also, given the low-frequency operation at light loads, efficiency can be high across the load range.

In addition to variable frequency, however, there are some downsides to this method. The circuit does depend on voltage ripple being present, so a compromise is needed to provide ripple that is low enough for the load but high enough so that the control comparator isn't unduly affected by switching noise. There is also a lack of inherent overload protection—with excessive load, the frequency just increases further, which is high across the load range.

In addition to variable frequency, however, there are some downsides to this method. The circuit does depend on voltage ripple being present, so a compromise is needed to provide ripple that is low enough for the load but high enough so that the control comparator isn't unduly affected by switching noise. There is also a lack of inherent overload protection—with excessive load, the frequency just increases further, which adds to switching losses. This is why there's usually a minimum off-time limit formed by the block in the figure labeled "min off."

## A Fixed-Frequency Control Method: Voltage Mode

Voltage mode typically operates at fixed frequency with PWM. In **Figure 2**, the output voltage is compared with a reference, and an error signal  $V_E$  is generated to directly control the width of the on-time pulse from the power switch. It's a linear negative feedback loop, which is bandwidth-limited to avoid instability, so at least switching frequency noise is filtered out.

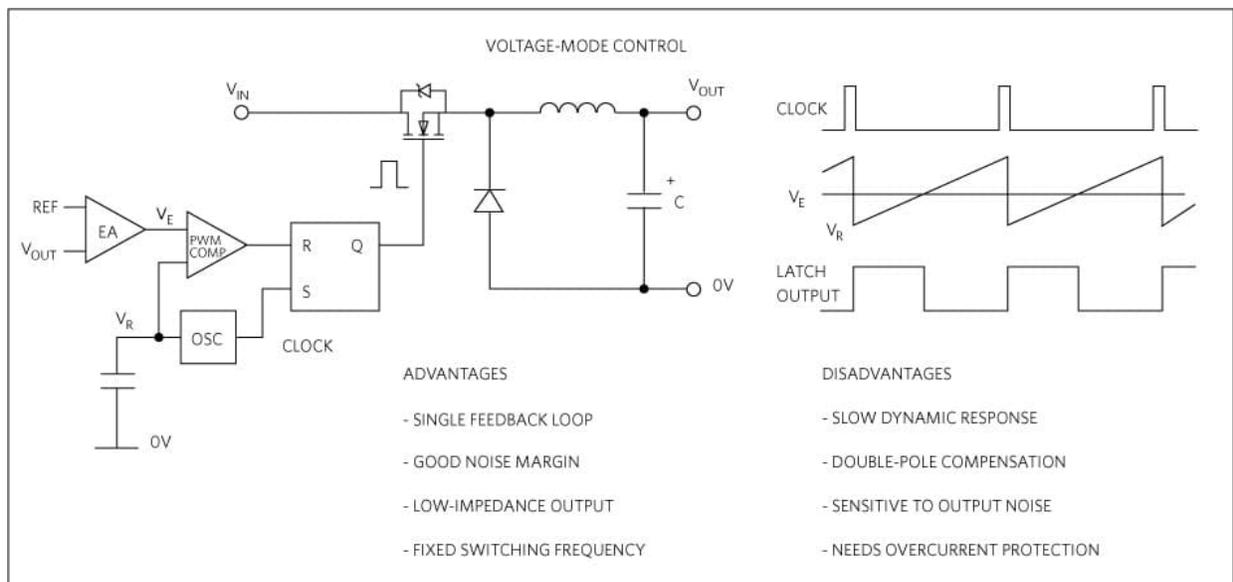


Figure 2. Voltage-mode control.

However, in a buck converter with its LC output filter, there is a 180-degree phase shift in small signal response above its resonant frequency, which might be only a few hundred Hz. This, coupled with the inherent 180-degree shift of a negative feedback loop, gives us 360 degrees of shift, leading to certain instability if there is any loop gain at that frequency. This would force us to roll off the gain in the error amplifier at such a low frequency that the loop would be painfully slow. The output capacitor ESR can be helpful here, partly because above the corner frequency of the capacitance and its ESR, the ESR dominates so the output circuit turns into an LR network, which has less phase shift than an LC. This enables the loop bandwidth to be usefully extended. The problem does, however, return with the use of ceramic output capacitors, which have virtually no ESR.

In any case, for the best loop speed and output accuracy, the error amplifier needs careful tailoring of its frequency response. Although we've been focused on buck converters, this technique can be easily used in other topologies as well, such as boost, buck-boost, and all types of isolated converters except push-pull circuits.

## A Method for Higher Loop Bandwidth: Current Mode

Cecil Deisch is credited with inventing current-mode control initially to prevent "staircase saturation" of transformers in push-pull circuits found with voltage-mode control. Before long, though, this technique became recognized as beneficial when applied to most converter topologies. As shown in **Figure 3**, this implementation is similar to voltage mode except the sawtooth ramp is not separately generated; it's derived from the inductor current ramp during the switch on-time. This means that we are turning the switch off when a particular peak current is reached and on again with a clock signal. This method offers several benefits. The output filter is now driven from a controlled current source, which makes it a single-pole response. This has just 90 degrees of phase shift above its corner frequency, allowing much higher loop bandwidth before the overall phase delay reaches 360 degrees. The error-amplifier compensator network becomes much less critical and can be more easily integrated into control ICs.

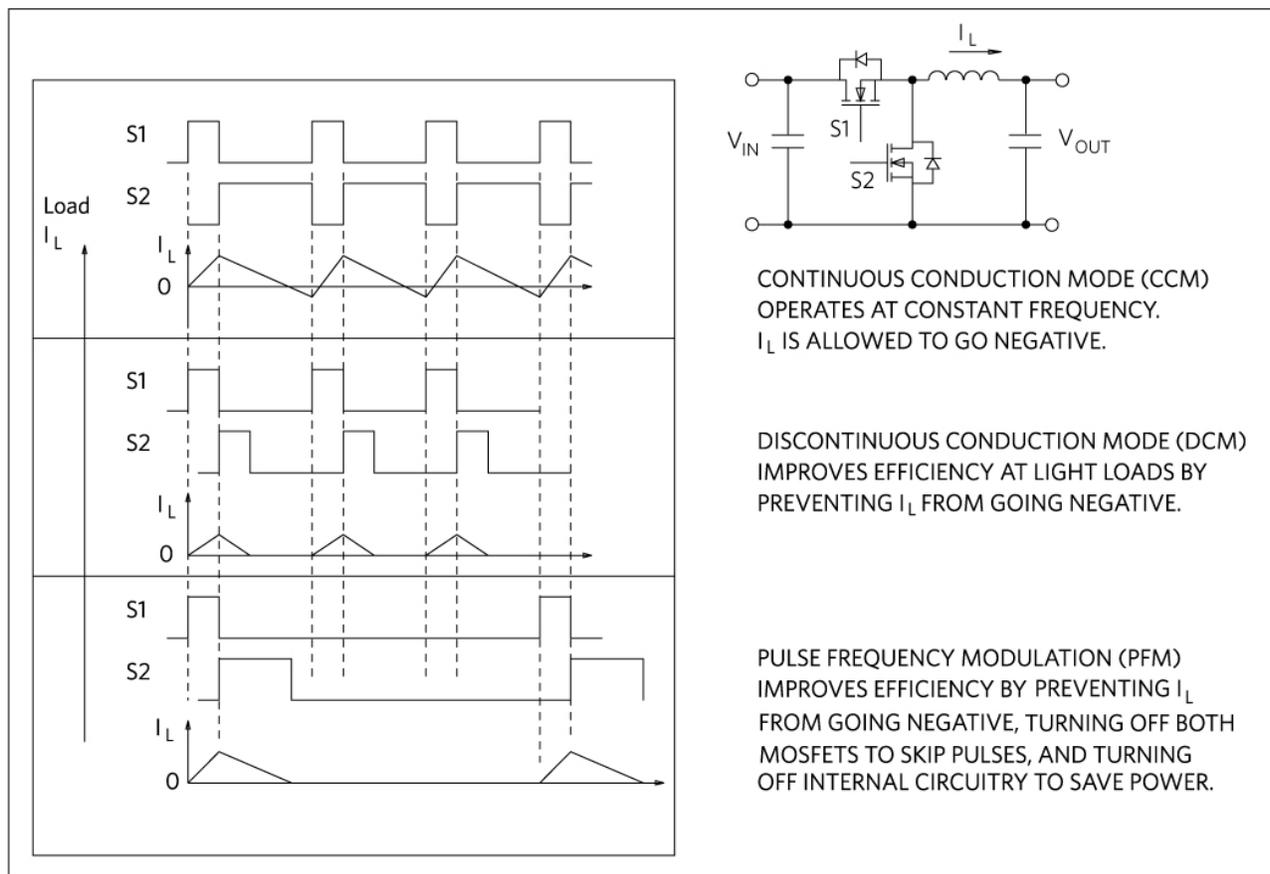


Figure 3. Current-mode control.

Because the peak current is directly sensed, the switch current can be limited to a safe value with overloads on a pulse-by-pulse basis. As a result, you can work closer to the magnetic saturation limit of the inductor, knowing that there is a quick current limit available. Lastly, there is an automatic feed-forward mechanism that directly controls the pulse width for changes in input. In a voltage-mode circuit, you have to wait for an input voltage change to propagate through the power stage to the output and back through the error amplifier before it is corrected. In current mode, an input voltage change directly affects the slope of the inductor ramp according to:

$$\Delta L = \frac{(V_{IN} - V_{OUT})t_{ON}}{L}$$

A higher input voltage produces a faster ramp, which means you can get to the switch-off threshold sooner and get a shorter pulse—just what you need to correct for the higher voltage. Line regulation is, therefore, very good in current mode-controlled circuits.

Load current sharing is another benefit of current-mode control. If the same error signal  $V_E$  is applied to several identical converters, then the peak currents of the converters are maintained equal and, by extension, so are the average currents of the converters.

What are the downsides of current mode control? If the circuit is operated above 50% duty cycle, an effect called sub-harmonic oscillation emerges. This effect can appear to be caused by gain peaking of the current loop at half the switching frequency. This manifests itself as alternate narrow and wide power pulses. The fix is quite simple, though—the ramp slope from the inductor current is artificially increased by adding in a ramp derived from the system clock. Increasing the sensed current slope by a value greater than half of the downslope of the inductor current does the trick. Too much slope compensation does, however, turn the loop back into voltage mode, so more is not better in this case.

Current mode works well in all topologies except half bridge, which needs extra complexity to avoid runaway imbalance in the series bridge capacitors.

### **A Reminder About Poles and Zeros**

In control loops we talk about poles and zeros. These are maxima and minima of a transfer function occurring at particular frequencies and represent turning points in a plot of gain versus frequency.

## Fair Compensation

To guarantee stability and for the fastest, most accurate control of output voltage, the voltage-mode and current-mode schemes need error-amplifier frequency response tailoring or compensation. Three schemes, called Type I, Type II, and Type III, have covered all practical applications. The type number corresponds to the number of poles in the error-amplifier response.

**Figure 4** shows the arrangements. You might recognize the Type I compensator as an integrator with a gain that drops at 20dB/decade from its maximum value at DC. The phase shift is a constant 270 degrees (90 degrees integrator plus 180 degrees from the op amp). The circuit would keep some loops stable but with very poor loop bandwidth.

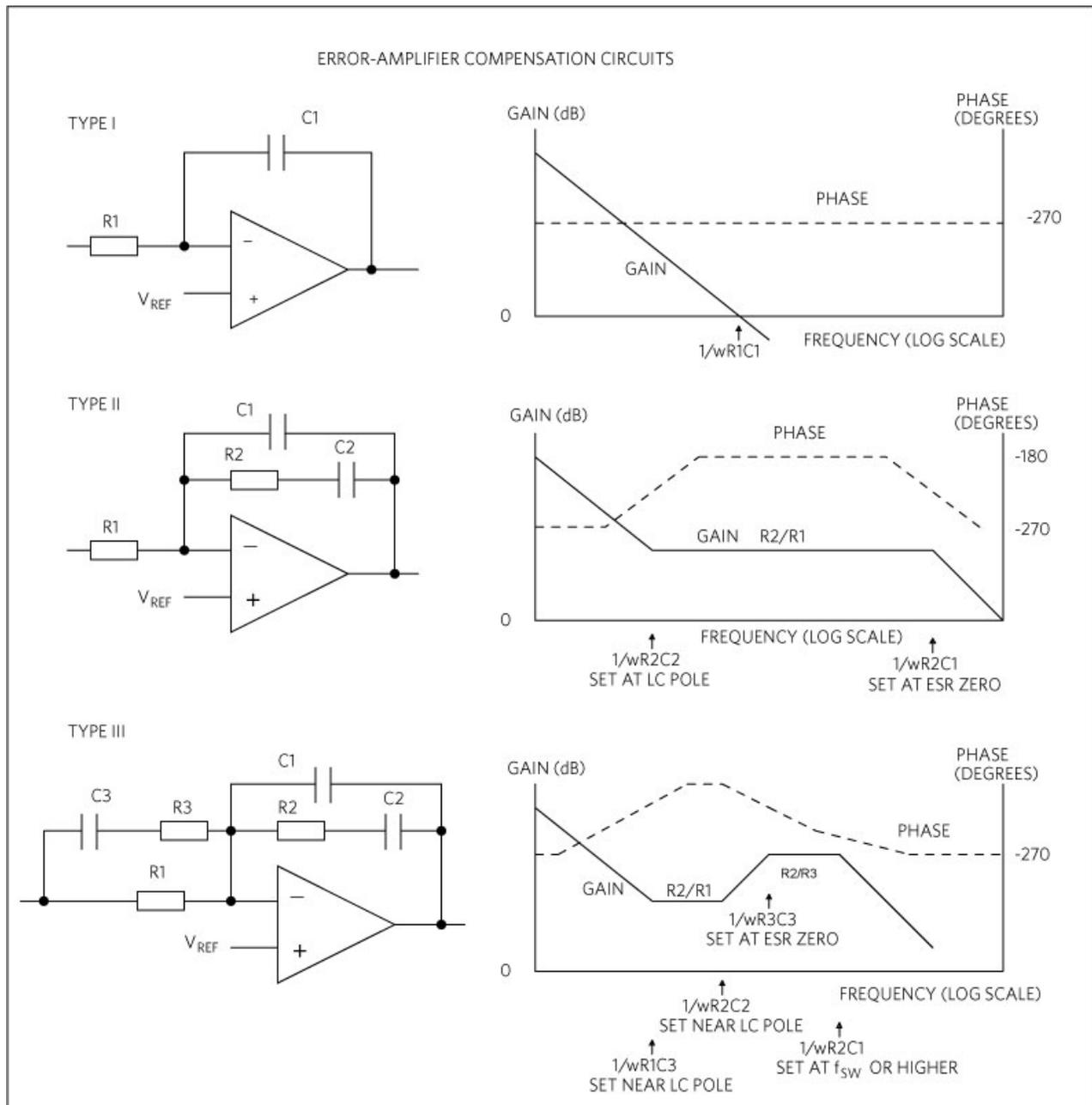


Figure 4. Error-amplifier compensation circuits.

Used in current-mode converters, Type II compensators have two poles and one zero. Like Type I, there is a pole at 0Hz but a zero that you place at the lowest frequency at which the single-output filter pole appears. This cancels the phase shift caused by the pole and adds gain to stop the -20dB/decade gain rolloff caused by the 0Hz pole. The effect of this is to extend the useful bandwidth of the loop. A final high-frequency pole ensures that the gain turns down again before the overall loop phase shift reaches 360 degrees with some margin.

The Type III compensator is used for voltage-mode control where the double pole of the output filter introduces a steep -40dB/decade gain rolloff in the power stage transfer function with a rapid phase change of -180 degrees. The compensator has two zeros that are placed again to cancel the two output filter poles. The 0Hz pole and two high-frequency poles are placed to keep gain high and minimize phase delay to as high a frequency as possible. Given the number of variables possible, you can play around with different pole-zero placement schemes to optimize results under differing conditions.

Using these techniques, the loop can have useful gain and bandwidth up to about a tenth of the switching frequency. A higher amount would lead to switching noise and associated problems. Learn more about this topic by watching the video, "[Introduction to Control Algorithms in Switching Regulators](#)" hosted by Bob Mammano, the father of the first switch-mode power supply. This video is part of a [power system design seminar video series](#), where Mammano shares techniques for designing smaller, simpler, cooler power designs.

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