

# ACHIEVING DESIRED DYNAMIC PERFORMANCE IN HIGH-SPEED, HIGH-RESOLUTION ADCS WITH LEVEL TRANSLATORS/ISOLATORS IN THE SYSTEM

By: Kien Mach

*Abstract: Communicating with ADCs above 500ksp/s is tough. Adding another variable such as a level translator or isolator to the SPI communication requires more understanding of timing and modifying hardware and firmware. This application note discusses how to achieve the desired dynamic performance with level translators or isolators.*

## Introduction

The **MAX11905** is a 20-bit, fully differential SAR analog-to-digital converter (ADC) that samples at 1.6Mps. When designing a board with the MAX11905, one requirement is to test different ranges of  $V_{OVDD}$ , 1.5V to 3.6V. The **MAX11905EVKIT** uses a **MAX14935** isolator that is capable of 150Mps and can support 1.71V to 5.5V I/O translating on both ends. Integrating the isolator between the ADC and the master board is not as simple as connecting all the I/O signals. In this application note, we'll discuss how to achieve the desired dynamic performance.

## Design and Test (General Case)

In the general case, the design in **Figure 1** works at a low sampling rate, which means slow SPI SCLK under 1MHz. For this case, the master device is running at 75MHz SCLK to achieve 1.6Mps. The MAX14935 has a typical propagation delay of 37.7ns for  $t_{pLH}$  and 37.9ns for  $t_{pHL}$ . When the MAX11905 is ready to return data, the signal has gone through the isolator twice and is off by a typical propagation delay of 75.4ns to 75.8ns. When dealing with high speed and high resolution, every nanosecond starts to become critical.

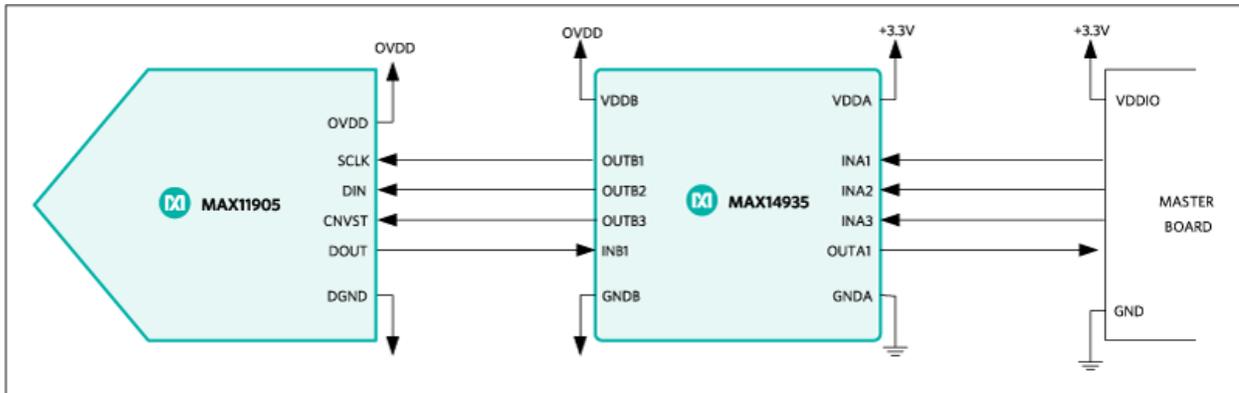


Figure 1. Circuit of digital communication of ADC with isolators (general case).

While testing the circuit of Figure 1, the data was not able to exceed  $\pm 262,143$  counts, and the positive and negative peaks clipped with a full-scale sine wave applied at the inputs of the MAX11905. **Figure 2** is the data capture using the MAX11905 EV kit software. The expected data should have been closer to  $\pm 524,287$  counts. Due to the delay of the isolator, the MSB of the data was missing and was only able to capture 19 bits of data instead of 20 bits. The missing bit affected the dynamic performance dramatically. The specified SNR of the MAX11905 is 98.1dB. **Figure 3** shows SNR was only 35.9dB. How is this issue resolved?

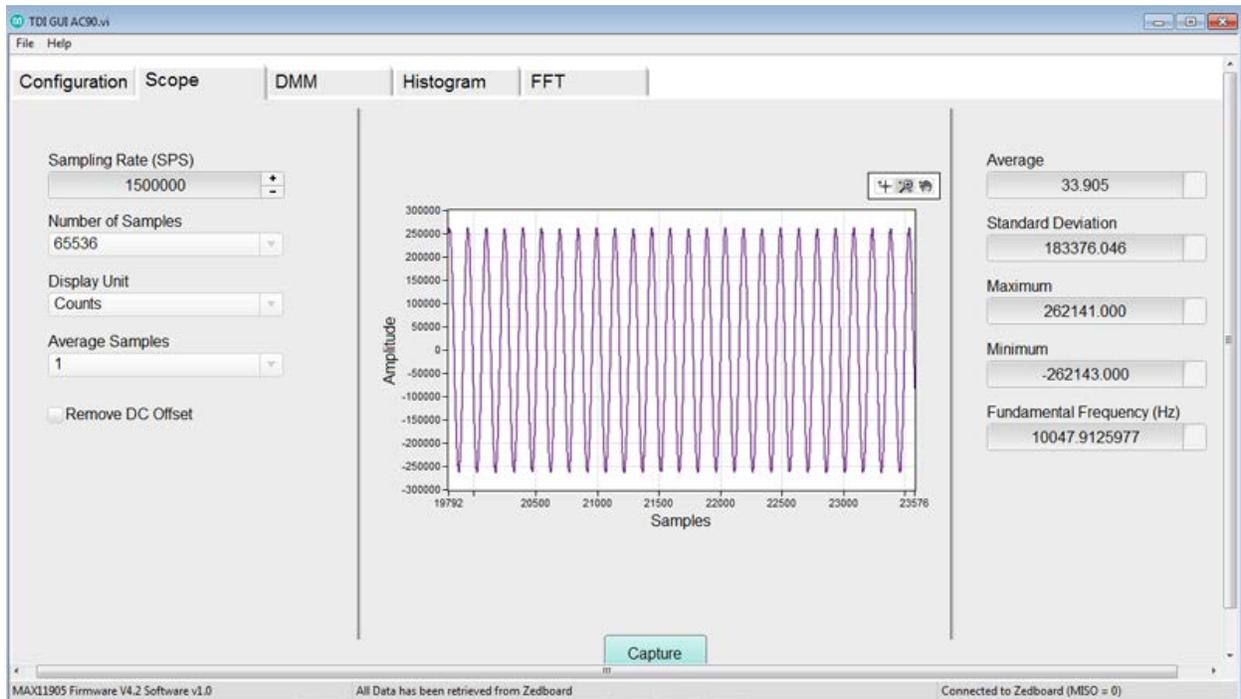


Figure 2. Data capture of general case.

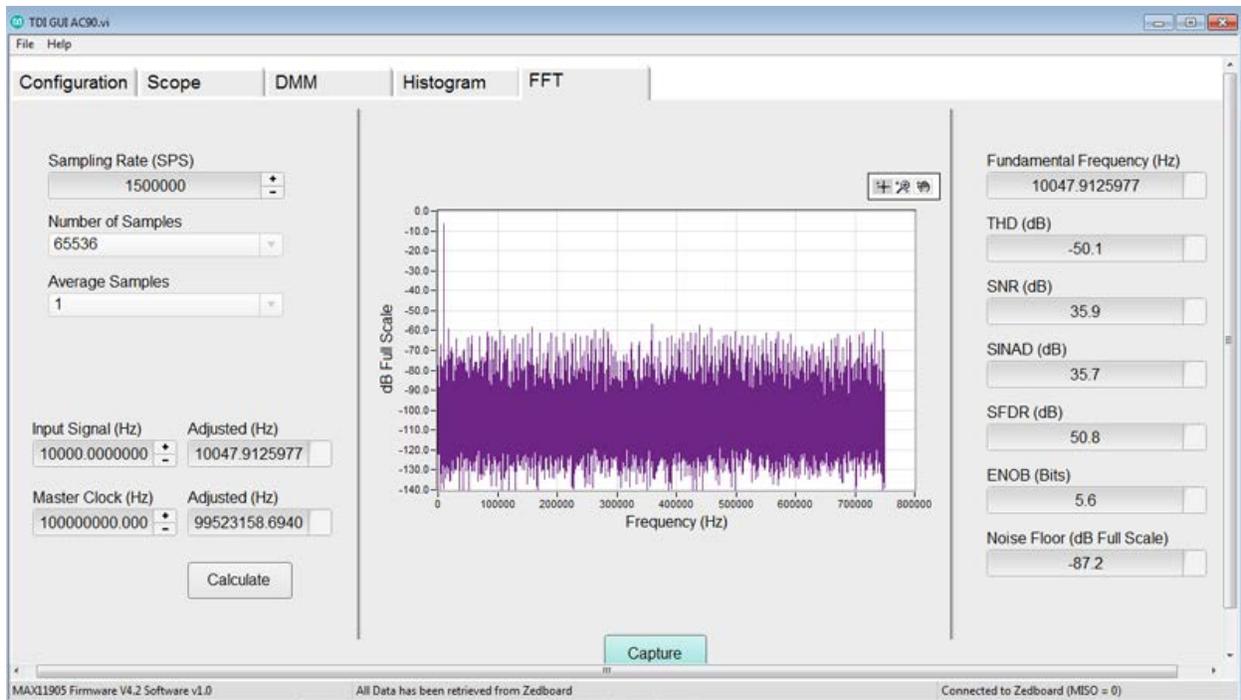


Figure 3. FFT of digital communication of ADC with isolators (general case).

## Design and Test (High-Speed Case)

For simplicity of comparison, **Figure 4** is called the high-speed case. Another isolator, **MAX14936** (same family of parts, but different numbers of I/O in different direction), is introduced to the system. Notice how there is a copy of the SCLK between the MAX11905 and the MAX14935, then it is routed back to the master device via MAX14936. With the copy of the SCLK, the delay is eliminated and DOUT data is clocked with the correct SCLK edges. Not only do we introduce new hardware, but the design also requires firmware adjustments to take in the return SCLK. The master device needs to use copy of the SCLK to store the data. One other note to keep in mind is to have the return SCLK and DOUT on the same isolator. It is not guaranteed that the MAX14935/6 propagation delays are the same from device to device.

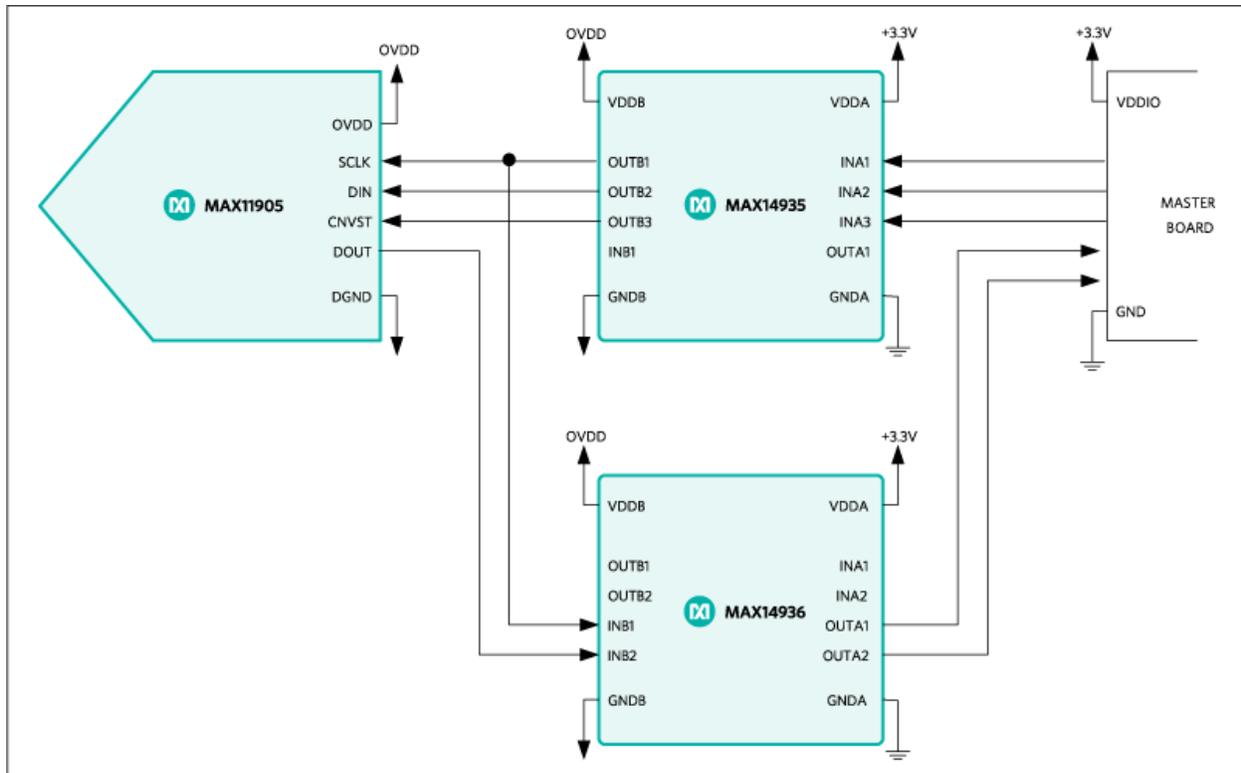


Figure 4. Circuit of digital communication of ADC with isolators (high-speed case).

**Figure 5** shows the performance with two isolators and a return SCLK. The dynamic performance is closer to what is expected of the MAX11905.

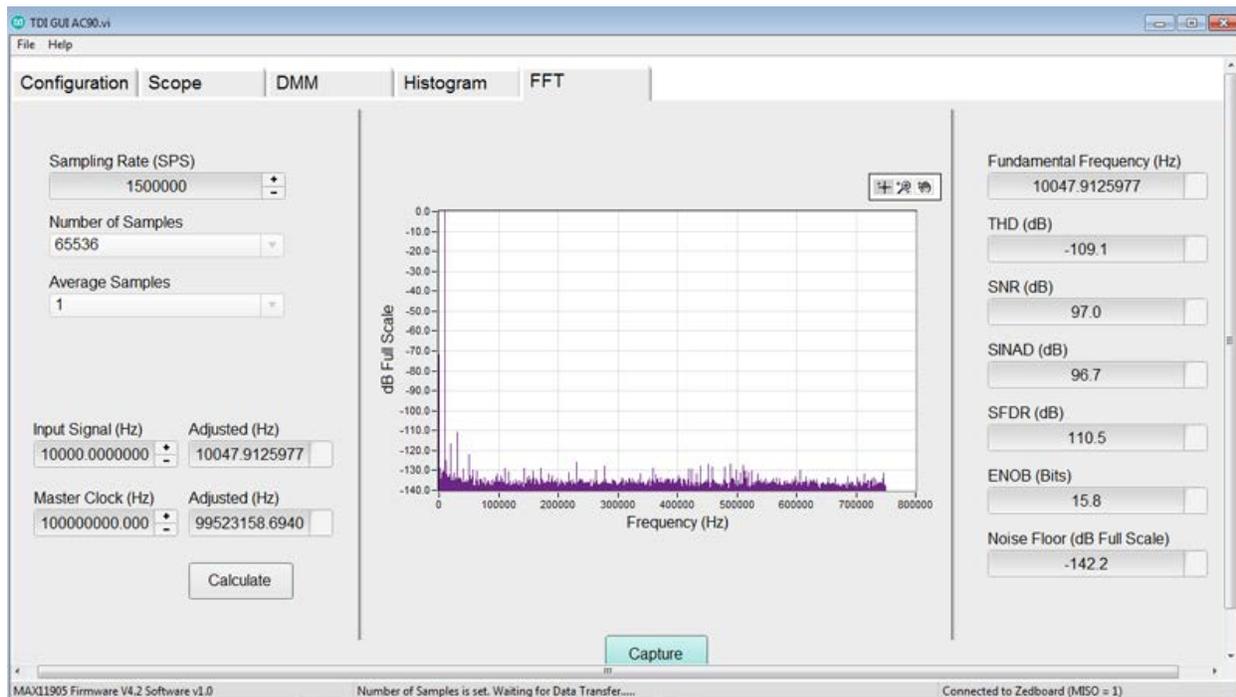


Figure 5. FFT of digital communication of ADC with isolators (high-speed case).

Table 1. Dynamic Performance

Parameter	General Case (dB)	High-Speed Case (dB)
THD	-50.1	-114.9
SNR	35.9	97.4
SINAD	35.7	97.4
SFDR	50.8	118.2
ENOB	5.6	15.9
Noise Floor	-87.2	-139.7

## Conclusion

When designing a high-speed, high-resolution ADC using a device such as the MAX11905 with isolators/level translators, always return a copy of the SCLK with DOUT to the master device. Apply this design to all high-speed, high-resolution ADCs and achieve the desired dynamic performance. Doing so saves time and money in creating new hardware and firmware.

## Related Parts

<a href="#">MAX11905</a>	20-Bit, 1.6Msps, Low-Power, Fully Differential SAR ADC	<a href="#">Free Samples</a>
<a href="#">MAX14935</a>	Four-Channel, 5kV <sub>RMS</sub> Digital Isolators	<a href="#">Free Samples</a>

**More Information**

For Technical Support: <https://www.maximintegrated.com/en/support>

For Samples: <https://www.maximintegrated.com/en/samples>

Other Questions and Comments: <https://www.maximintegrated.com/en/contact>

---

Application Note 6488: <https://www.maximintegrated.com/en/an6488>

APPLICATION NOTE 6488, AN6488, AN 6488, APP6488, Appnote6488, Appnote 6488

© 2014 Maxim Integrated Products, Inc.

The content on this webpage is protected by copyright laws of the United States and of foreign countries. For requests to copy this content, [contact us](#).

Additional Legal Notices: <https://www.maximintegrated.com/en/legal>