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APPLICATION NOTE 6323

OPTIMIZING YOUR POWER AMPLIFIER FOR PREDISTORTION WITH RF PA LINEARIZER (RFPAL)

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Abstract: This document provides guidelines in designing a power amplifier to achieve optimum performance with Maxim's Radio Frequency (RF) Power Amplifier (PA) Linearizer (RFPAL) or other types of predistortion.

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1. Introduction

This document provides guidelines for designing a power amplifier to achieve optimum performance with Maxim's radio frequency (RF) power amplifier (PA) linearizer (RFPAL) or other types of predistortion. Using RFPAL products (SC1894 and SC2200), an optimally-tuned PA can achieve up to 28dB of correction; thereby, allowing the amplifier to operate at the highest possible efficiency. Conversely, a PA which has not been optimized for operation with a linearizer could achieve little-to-no improvement in linearity and it could fail to meet the spectral requirements.

The majority of RF PAs deployed in wireless infrastructure applications use either a Class AB or Doherty architecture. Class AB PAs are commonly used in microwave backhaul applications or in very low antenna-output power applications and are dynamically biased between Class A and Class B. They are a compromise between linearity, output power, efficiency and cost. On the other hand, Doherty PAs are used to deliver high power at high efficiency using high-PAR signals, but they require the use of linearization technology to meet the spectral emissions mask requirements. RFPAL can be applied to

both types of amplifiers to achieve better efficiency and linearity results. The typical efficiency curves for Class AB and Doherty PAs, as a function of the output power, are shown in **Figure 1**.

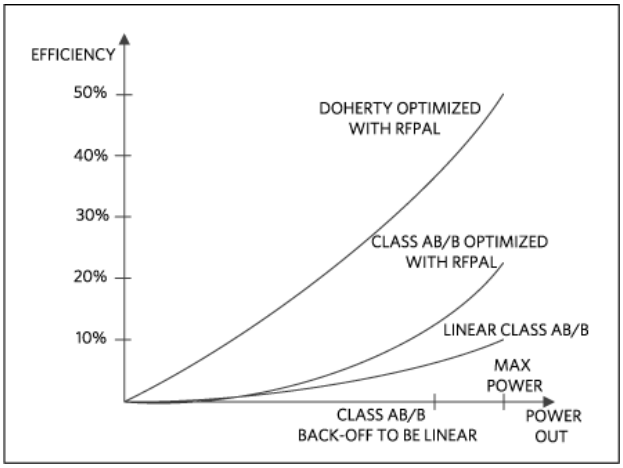

Figure 1. Ideal power-efficiency curves for Class AB/B and Doherty power amplifiers.

In Figure 1, we can see that to achieve reasonable linearity for Class AB PAs, the average power must be reduced so that the signal peaks are below the 1dB compression point. The efficiency now is very low, around 10%. This can be increased to around 24% with a class AB PA optimized for linearization, as we can now push the signal peaks into the nonlinear region of operation of the PA, close to saturation. The Doherty PA relies on a circuit technique to achieve high efficiency in the backoff region, where the signal spends most of its time. Typically, an LDMOS Doherty PA optimized for wireless infrastructure applications achieves up to 50% efficiency. But some form of linearization is essential to meet the specifications, as the Doherty PA is a nonlinear device.

A common approach to linearization in wireless infrastructure is digital predistortion (DPD). This is typically a closed loop system using a feedback path that taps into the PA output, down-converts and then digitizes the signal, which is then used by the linearizer. Therefore, a typical feedback path consists of blocks including a down-converting mixer, a variable gain amplifier and an ADC. As a discrete implementation, these components add additional cost and power consumption to the system. The RFPAL integrates the linearizer and all necessary feedback components into a single IC. This vastly simplifies (and speeds up) the system implementation and minimizes the additional board space.

2. Proper Transistor Line Up

RF PA transmitter systems typically require a significant amount of power gain that can only be achieved through the use of multiple gain stages. The final stage transistor(s) are selected to meet the system output power specification in the given PA architecture, and their behavior contributes to other critical requirements like linearity and efficiency.

The PA must be designed for a peak power output that is equal to or greater than the required average power of the transmitter, plus the peak-to-average ratio (PAR) of the signal. This is to ensure that the peaks of the signal are not clipped or distorted, with consequent loss of information. The average power requirement determines the distance or range of the transmitted signal: the cell coverage. The choice of final PA stage transistors depends on the PA architecture.

- For Class AB PAs, the peak or saturated power PSAT of the transistor determines the peak power of the PA.
- For Doherty PAs, there are several variables, including how many Doherty branches are included, whether the design is symmetric, using identically-sized transistors, or asymmetric, using higher power transistors for the peaking amplifier(s), input power splitting ratio, to name but a few. Generally, the peak power of a Doherty PA is the sum of the PSATs of the transistors, and the average power is determined by power capability of the main amplifier transistor.

Typically, the final PA in the transmitter line-up has a power gain of around 15dB. The rest of the required gain is made up using a cascade of several driver and predriver stages. These amplifier stages must be designed to operate in their linear range; it is assumed that virtually all of the transmitter distortion is produced in the final stage PA. The driver amplifier must be sized so that it is capable of delivering the input required by the PA at peak

power, with some margin. This is to ensure that the driver operates below its 1dB compression point at all times, and delivers linear output. The predriver stages must be sized in a similar way, though this is usually not a problem as the power levels required are quite modest. In **Figure 2**, we show an example lineup for a nominally 10W average power transmitter that can be used for 3G or 4G signals with a PAR of up to 8dB.

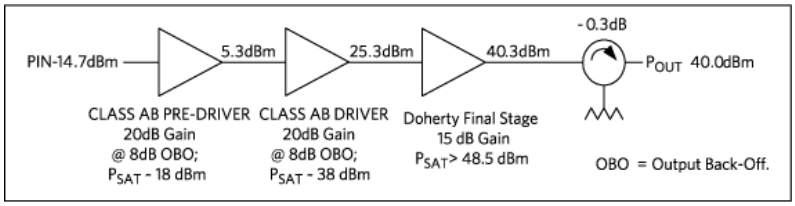

Figure 2. Example 10W PA lineup.

The selection of the driver and predriver devices is especially important for low-power transmitters, such as small cell designs in which the average power output is below about 5W. In this case, the power consumption of the driver stages has a great impact on the overall system efficiency. The driver device might not have to meet the stringent linearity demands of the full PA if we include the driver in the RFPAL linearizer loop. Nevertheless, this approach takes predistortion resources away from linearizing the final stage. This can result in a lower overall linearity, but higher system efficiency. In this low-power transmitter case, the driver should be chosen so that its linearity, measured by its ACLR performance, for example, is about 0dB to 3dB better than ACLR of the corrected final stage. An approximate rule of thumb is to choose the driver with a saturated power, P_{SAT}, about 3dB higher than the peak input power required by the final stage.

In the case of medium power PAs, the driver-stage devices are typically optimized to be just linear enough not to degrade the overall ACLR performance significantly. This 'better linearity' results in lower efficiency, but frees up linearizer resources to correct the final stage. In the medium power transmitter case, the driver linearity or ACLR should be ~5dB better than the corrected final stage.

In high power PAs, as used in macro base-stations, the driver and predriver transistors are selected such that neither the driver nor the predriver degrade the overall linearity performance. The efficiency of the predriver and driver are low, but this represents a very small reduction in the overall high-power transmitter efficiency. Furthermore, the priority in these systems is to achieve the highest possible final-stage efficiency, often at wide-signal bandwidth. In the high-power transmitter case, the driver linearity should be 10dB better than the corrected final stage.

3. Desired PA Characteristics for Correction using RFPAL

Maxim's RF predistortion algorithm is based on a Volterra series approximation, which is commonly used in the field of PA linearization. The Volterra series is an infinite series, so in practice, we truncate the series to give the best compromise between accuracy of the approximation and cost of the calculation. Maxim has chosen a Volterra approximation comprising of four delay taps, each of which is an odd-order ninth-degree polynomial. This approach provides a good compromise between complexity and effectiveness, ensuring that we can cancel IM distortion products up to the ninth order. This is shown in more detail in **Figure 3** and **Figure 4**.

This simplified Volterra model assumes that the PA has flat and symmetrical intermodulation products in the desired frequency of operation range, well-matched AM-AM and AM-PM characteristic across the supported signal bandwidth, well-behaved AM-AM and AM-PM ripple and variation, as well as limited memory effects. Details of all these requirements are discussed in the following sections.

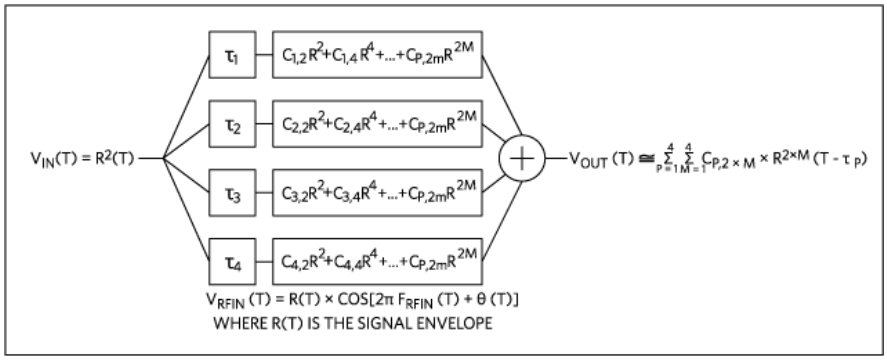

Figure 3. Volterra Series equation.

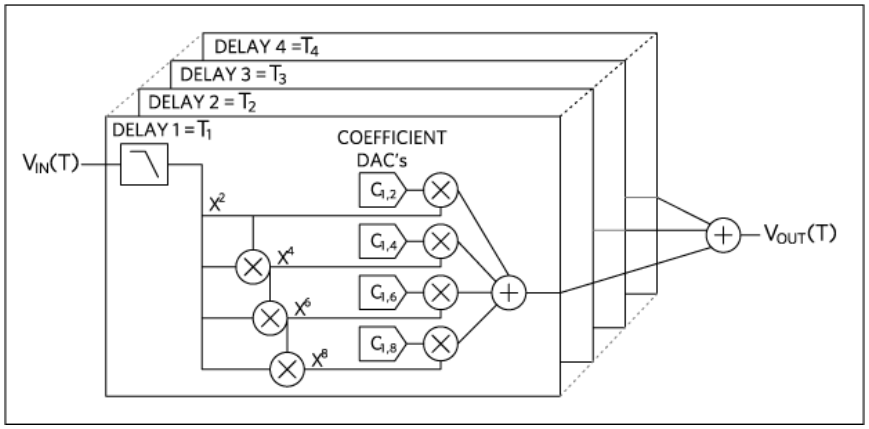

Figure 4. Volterra series block diagram.

3.1 PA AM-to-AM Response

AM-AM Response with gain ripple ² 2dB (unlinearized) across the entire operation range for best linearization performance.

The AM-to-AM response of the amplifier, namely the output power versus the input power, is one of the key characteristics used to determine the linearity and correctability of a given PA. A linear PA produces a straight AM-to-AM line response; for each 1dB increase in input power, the output power of the PA increases by exactly 1dB; being linear, the PA produces no distortion. A PA operated in deep backoff, far from compression, behaves in this way. But, this is not typically how we operate the PA in wireless infrastructure applications because the efficiency would be very low. The RF PAs used in cellular base stations are operated in compression, often close to saturation at the peaks of the signal, in order to maximize the efficiency. Under these operating conditions, the PAs are quite nonlinear, and some means of linearization is essential for the transmitter to meet specific spectral emission requirements while maintaining high-efficiency operation. Class AB amplifiers typically have a monotonic gain response with the gain decreasing as the output power approaches the saturation point, which is gain compression. Advanced PA architectures such as Doherty, generally have more complicated AM-to-AM responses. Doherty PAs often exhibit a gain expansion at the power level where the peaking amplifier is becoming engaged. **Figure 5** illustrates this Doherty gain expansion phenomenon at approximately 49dBm (RMS) P_{OUT}. To maximize the benefits of using RFPAL, this gain expansion must be minimized.

Figure 5.1 shows an example of an acceptable AM-to-AM response. For a well-designed amplifier, the AM-AM gain variation for the unlinearized PA should not exceed 2dB across the entire operation range, including the compression region. The gain in Figure 5.1 has a gain variation of about 1.4dB. RFPAL linearizes this PA to have a straight (linear) AM-to-AM curve as shown in **Figure 5.2**. In contrast, the PA in **Figure 5.3** has a gain ripple larger than 3dB, which limits the effectiveness of the RFPAL in linearizing this PA, as seen in **Figure 5.4**. These two different AM-to-AM curves were actually measured on the same PA with different bias. Because of this difference in the AM-to-AM response, the adjacent channel leakage ratio (ACLR) for a four-carrier WCDMA signal is 4dBc better on the properly designed PA in Figure 5.1 versus the poorly designed PA in Figure 5.3.

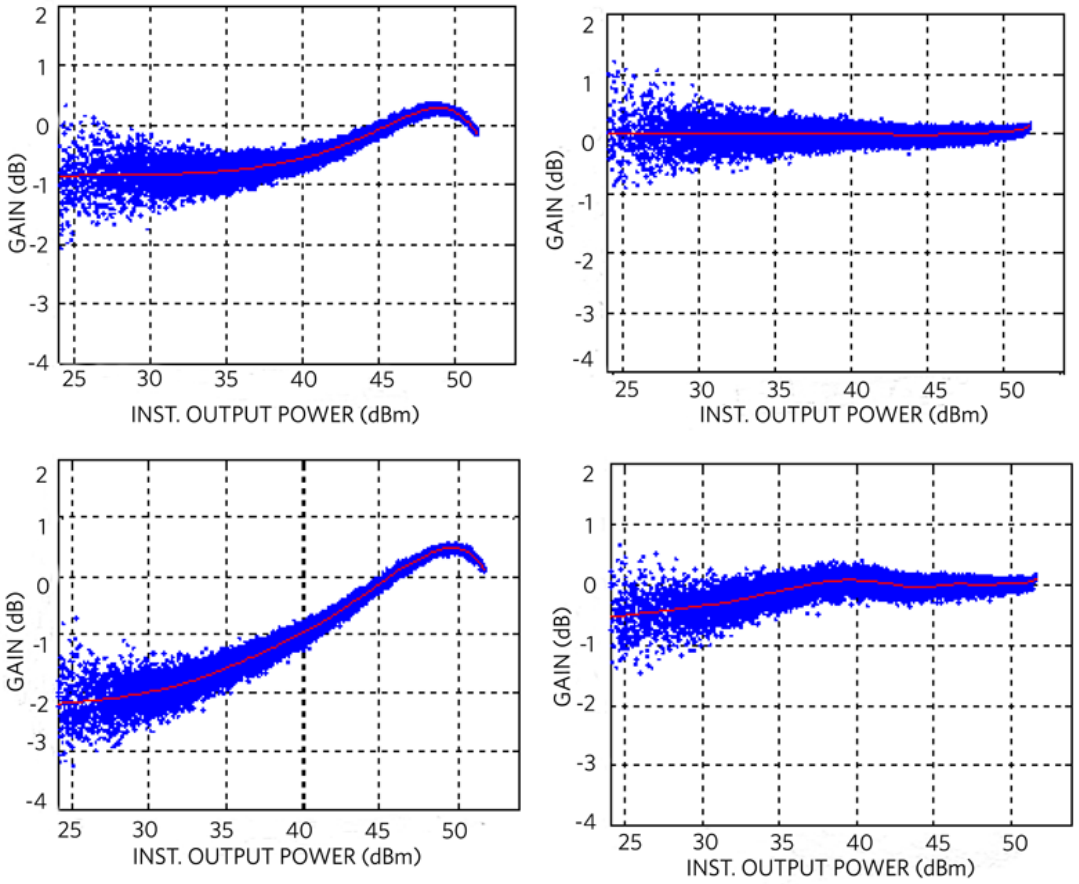

Figure 5.1. Uncorrected AM-to-AM for a well-designed PA.	*Figure 5.2. Corrected AM-to-AM for a well-designed PA.*
Figure 5.3. Uncorrected AM-to-AM for a poorly-designed PA.	*Figure 5.4. Corrected AM-to-AM for a poorly-designed PA.*

Figure 5. PA AM-AM Responses

The SC1894 does not include first order correction terms to provide equalization, or gain flatness correction over frequency. Therefore the PA should be designed to have a flat gain response over frequency with no more than 1dB variation across the target frequency band. Greater variation of up to 1.5dB can be tolerated, provided the phase variation (AM-to-PM; see below) is reduced to less than 10°. An uneven gain over frequency and (unlinearized) AM-AM gain variation greater than 2dB can significantly degrade the overall linearization performance.

Recommend improving PA gain flatness for wideband performance

3.2 PA AM-to-PM Response

The second key element for a correctible RF amplifier design using RFPAL is the phase response, or AM-to-PM response. The phase of the PA begins to rotate as the PA output power approaches P_{SAT}. The amount of phase rotation and the monotonicity of the phase change are both important to the linearization result.

The overall phase rotation should not exceed 15° if the gain variation is less than 1dB. If the gain variation is greater than 1dB, then the AM-to-PM should be less than10o for good linearization using RFPAL.

Additionally, the linearization performance is improved dramatically if the AM-to-PM curve is smooth and monotonic with no inflection points, as shown in **Figure 6.1**.

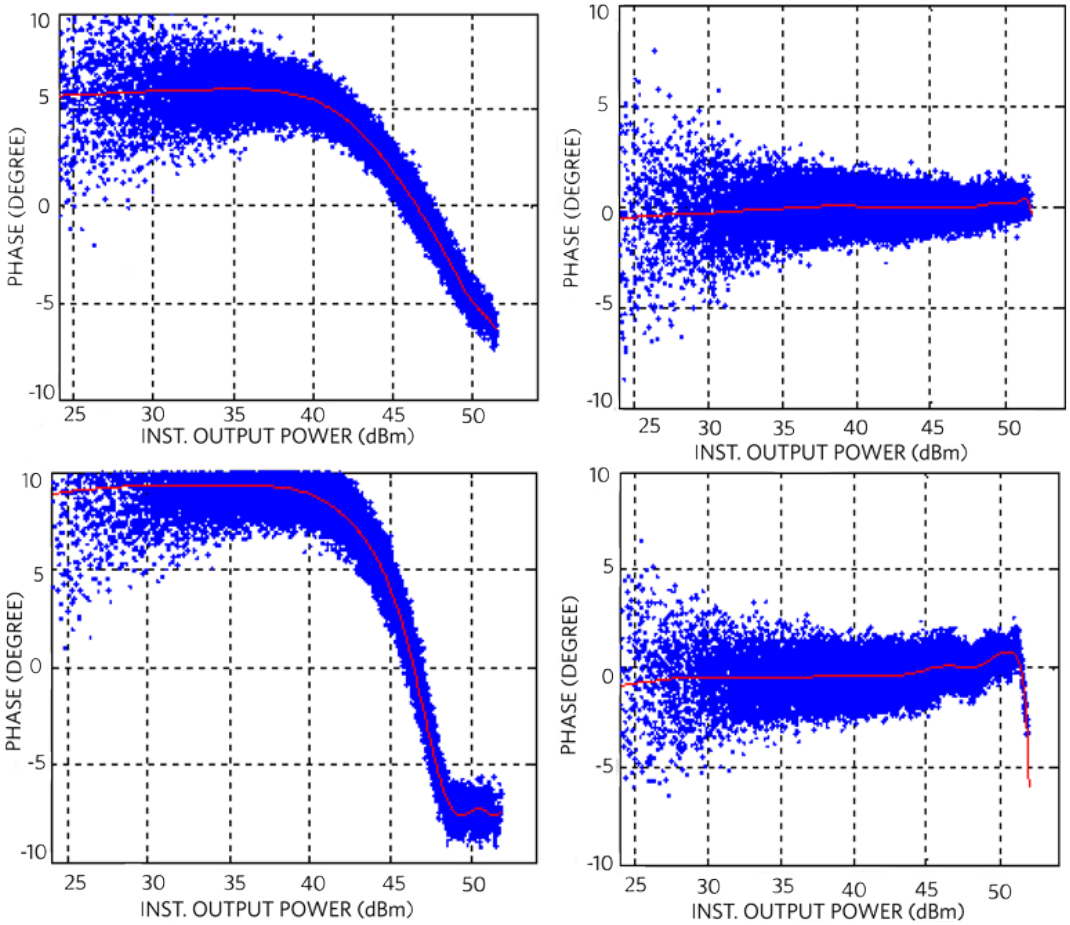

Figure 6.1. Uncorrected AM-to-PM for a well-designed PA.	*Figure 6.2. Corrected AM-to-PM for a well-designed PA.*
Figure 6.3. Uncorrected AM-to-PM for a poorly-designed PA.	*Figure 6.4. Corrected AM-to-PM for a poorly-designed PA.*

Figure 6. PA AM-PM plots.

A class AB LDMOS amplifier typically has a simple AM-to-PM curve (Figure 6.1), whereas Doherty type amplifiers can have both positive and negative slope characteristics in a single phase plot, illustrated in **Figure 6.3**. This multiple change of phase direction makes linearization more difficult. The recommendation is to shift the high power-phase change, phase at 49dBm (RMS) in Figure 6.3, to a power level higher than the peak (instantaneous) P_{OUT} operation range.

The AM-to-PM response of the amplifier should exhibit similar characteristics over the entire frequency range of the application: smooth, monotonic curves with a similar total phase change. Consistent AM-to-PM performance over frequency helps ensure consistent performance with any linearization schemes, including RFPAL.

3.3 PA Memory Effects

The so-called memory effects in a PA are really a manifestation of energy storage in the PA.

Keep the PA's memory effect under 5ns for best performance with RFPAL.

'Short-term' memory effects are associated with the matching networks of the PA, and the transistor's input and output capacitances and transit-time behavior. The matching networks in a PA are usually designed to be lossless impedance transformers, and the energy storage is in the reactive components of the match. These networks provide the conjugate matching at the PA input and the power matching at the PA output providing the appropriate match to 50Ω (usually) for the capacitive input and output admittances of the transistor. These matching networks are designed to function at the RF carrier frequency of the signal, and are not too important from a predistortion perspective, provided they produce a flat-frequency response and linear phase in the band of interest.

'Long-term' memory effects are on a timescale that can be associated with the envelope or information rate of the signal, and any variations in the PA performance or behavior on this timescale leads to distortion of the signal. These are the memory effects that are of primary concern in predistortion. The main sources of long-term memory effects are:

- **Thermal effects:** The amplitude of the information signal changes with time in response to the data itself and the number of users (the traffic load). This means that the energy input to the transistor varies with time, and the transistor heats up and cools down as a result. The rates of heating and cooling are dependent on the semiconductor material of the transistor, and are different from the rate of change of the signal energy. As a result, the instantaneous gain of the transistor, and PA, are changing with time, giving rise to complex gain behavior that is dependent not only on the signal value at a given instant, but also on the recent history of the signal. Thermal memory effects can be more pronounced in TDD operation, in which the PA signal is switched on and off continuously, resulting in bursts of heat energy into the transistor.
- **Charge-trapping effects:** The capture and later emission of charge, electrons in the transistor channel, causes changes in the current flow through the device that are dependent again not only on the instantaneous voltage in the device, but also on the history of the voltage signal. All semiconductor materials and interfaces are potential sources of traps, but silicon LDMOS transistors are relatively trap-free whereas power FETs made from compound semiconductors such as gallium arsenide (GaAs) and gallium nitride (GaN), which is becoming popular for wide-bandwidth PAs, are much more susceptible to trapping effects.
- **Bias and supply circuitry:** The PCB traces and decoupling or bypass capacitors found on the DC bias and supply circuits on the PA pallet contribute inductive and capacitive energy storage elements that contribute to memory effects. The large time constants associated with these bias- or supply-line filters makes them important contributors to long-term memory. An important measure of the bias circuit long-term memory effect is the **video bandwidth** described below.

The RFPAL architecture has four delay taps including a 300ns term. The 300ns delay compensates for strong thermal effects and is limited to IM3 only. The other taps can account for memory effect correction of up to 5ns.

3.4 Video Bandwidth (VBW)

Memory effects are created when VBW < IMD BW making predistortion more difficult.

Recommend VBW>3-5x signal BW for best performance with RFPAL.

The video bandwidth (VBW) of an RF power amplifier is usually expressed as the frequency range over which the PA shows a symmetrical and constant intermodulation (IM) product. This is usually measured by a two-tone test where the frequency spacing between the two tones is increased and the power levels of the higher as well as the upper- and lower-third orders IM products are monitored as a function of the tone separation. The total PA output power is kept constant during the tone separation sweep to remove any effect due to PA gain variation over the frequency band. **Figure 7** shows a VBW measurement for an LDMOS Doherty PA.

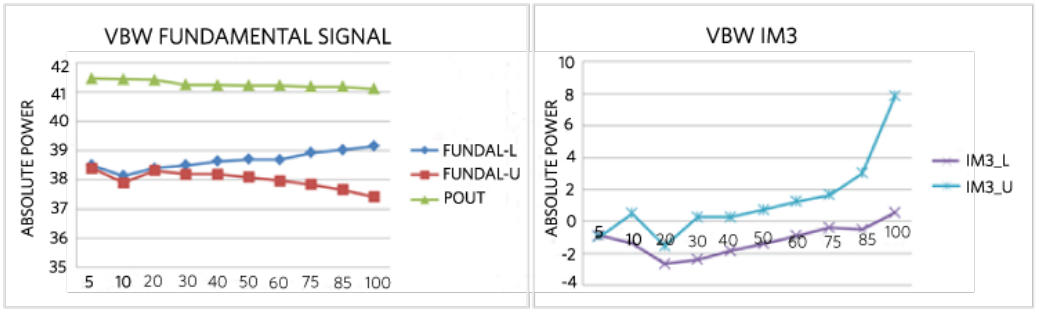

Figure 7. Example VBW measurements on LDMOS Doherty PA.

On the left is the total power and the power in each of the fundamental tones as the tone separation is increased. The total power is kept approximately constant while the individual tone amplitudes differ as a result of the broadband frequency response. On the right are the upper- and lower-third order IM tone powers. We reach about 90MHz tone separation before the two IM products begin to diverge by about 3dB. This yields a VBW of 3 × 90MHz 270MHz, which is the total frequency separation of the two IM tones in this case. We can also evaluate the VBW using higher-order IM tones. The fundamental tone separation at which the IM products diverge is less, but the total IM tone separation should be much the same:

$3 \times \Delta IM3 \approx 5 \times \Delta IM5$, where the deltas are the fundamental tone separations in each case.

The RFPAL requires that the VBW is greater than three times the signal bandwidth, and making the VBW four to five times the signal bandwidth enables the RFPAL to address higher-order intermodulation products more effectively for better correction performance. For example, for a PA designed to accommodate two contiguous 20MHz LTE signals for 40MHz signal bandwidth, the VBW needs to be at least 120MHz for the RFPAL to be able to correct for third-order IM asymmetries. If the signal is now the two-20MHz carriers placed at each end of Band 2, for instance, the total signal bandwidth is 60MHz, and the VBW requirement is increased to 180MHz to enable correction of the third-order products.

One of the main factors that impact VBW are the bias feeds. Refer to section 4.3 for more details.

4. Some Tips for Optimizing your PA for RFPAL

Running RFPAL during adaptation during this tuning step provides real-time feedback on the success of this optimization step.

When changing PA configurations (supply voltage, bias application, impedance matches, etc.), it is strongly recommended that RFPAL be reset before reoptimizing the PA performance.

4.1 Initial ACLR Consideration

The SC1894 RFPAL can provide typically between 15dB to 28dB of ACLR correction depending on the signal PAR, PA type, and signal bandwidth. Refer to PA results with RFPAL for more details. As an approximation, it is reasonable to assume 15dB of correction for an optimized Class AB PA and 20dB of correction for an optimized aggressively biased, high-efficiency Doherty PA.

For the RFPAL to be able to provide optimal correction, the PA should be designed so that the uncorrected ACLR of the PA is no worse than the target ACLR + 15dB for class AB PA and ACLR + 20dB for Doherty PA. For instance, if the ACLR target for a small cell using WCDMA waveforms is -50dBc with a high-efficiency Doherty PA, the initial uncorrected ACLR should be no worse than -50dBc + 20dBc -30dBc.

4.2 Analyze AM-AM and AM-PM result with RFPAL in the loop

As shown in section 3, characterizing the amplitude and phase response of a PA is important for optimizing the system performance. The amplitude and phase response of the PA **with** RFPAL enabled should also be measured. Doing so provides valuable information on which parameter is not being sufficiently corrected; thereby, degrading the ACLR performance whether it is primarily the amplitude, phase, or memory effect. If all three parameters are satisfactory, but the PA is still not achieving the target specifications, then the cause is likely due to insufficient VBW.

A big advantage of RFPAL is that it allows the PA and linearizer to operate together and enables the tuning and optimization of the PA's matching circuitry, gate and drain bias, and Doherty circuitry under active conditions.

4.3 Signal and Video Bandwidths

RF power transistors generally have fairly low load and source characteristic impedances for optimal power output and efficiency performance. The input and output matching networks are designed to transform these low impedances to 50Ω. The matching networks are often designed for lowest Q, to maximize the RF-signal bandwidth.

The PA must also be designed for maximum, or at least optimal VBW. While the VBW is measured at RF, it is determined by lower-frequency concerns. The asymmetry in the odd-order IM products is a result of the modulation of the PA behavior by even-order IM products, which are found close to DC. The DC connections to the PA are ideally short circuits, but must maintain this low impedance over a specific bandwidth in order to short out any even-order IM signals created at the transistor's connections. If this low-frequency impedance is not negligible, then the even-order IM products generate a voltage signal that modulates the bias, which in turn modulates the complex gain of the PA, for instance, a nonlinear memory effect. Maintaining low RF impedance for the DC connections over a wide frequency range is a goal of PA bias line design. The use of decoupling capacitors placed close to the transistor connections can improve this parameter, and hence increase the VBW. Some RF power transistor manufacturers have addressed this issue by package design and in-package circuitry.

4.4 Drain Voltage and Quiescent Current (I_{DSQ})

Setting the quiescent current of the power transistor to the proper level is also one of the key steps in the process of optimizing the PA performance and also its performance with RFPAL. With the supply voltage applied to the amplifier pallet (i.e., 5V, 28V, or 48V), the gate voltage is adjusted such that the quiescent current (I_{DSQ}) is raised to the target value. For Doherty amplifiers, the quiescent current of the main amplifier is generally adjusted as for a standard Class-AB amplifier, whereas the gate voltage of the peaking amplifier is below the level of the gate-to-source threshold voltage (V_{GSTH}), placing this device in Class C. Adjusting the gate bias of the peaking transistor affects the linearity and efficiency of the overall Doherty PA.

5. GaN PA Design Considerations for Linearization with RFPAL

5.1 Introduction

GaN technology brings the advantage of large bandwidth at the expense of gain expansion and increased distortion in large backoff (12dB to 15dB away from max power). We refer to the distortion in large backoff as "small signal distortion."

Whereas LDMOS PAs typically have very little nonlinearity at high backoff (> 15dB from P_{MAX}), to the extent that RFPAL output could be disabled, GaN PAs can have significant distortion at such high backoff, possibly more than at higher power levels. Furthermore, for LDMOS PAs, the gain of the PA in backoff is independent of output power level, at least to a first approximation, but it is common to see the gain of a GaN PA increase > 3dB at 10dB backoff, for example.

The Volterra series correction signal is generated by the correction block (CORR) of the SC1894. A simplified block diagram is shown in **Figure 8**. The elements affected by GaN PA behavior are shown in red.

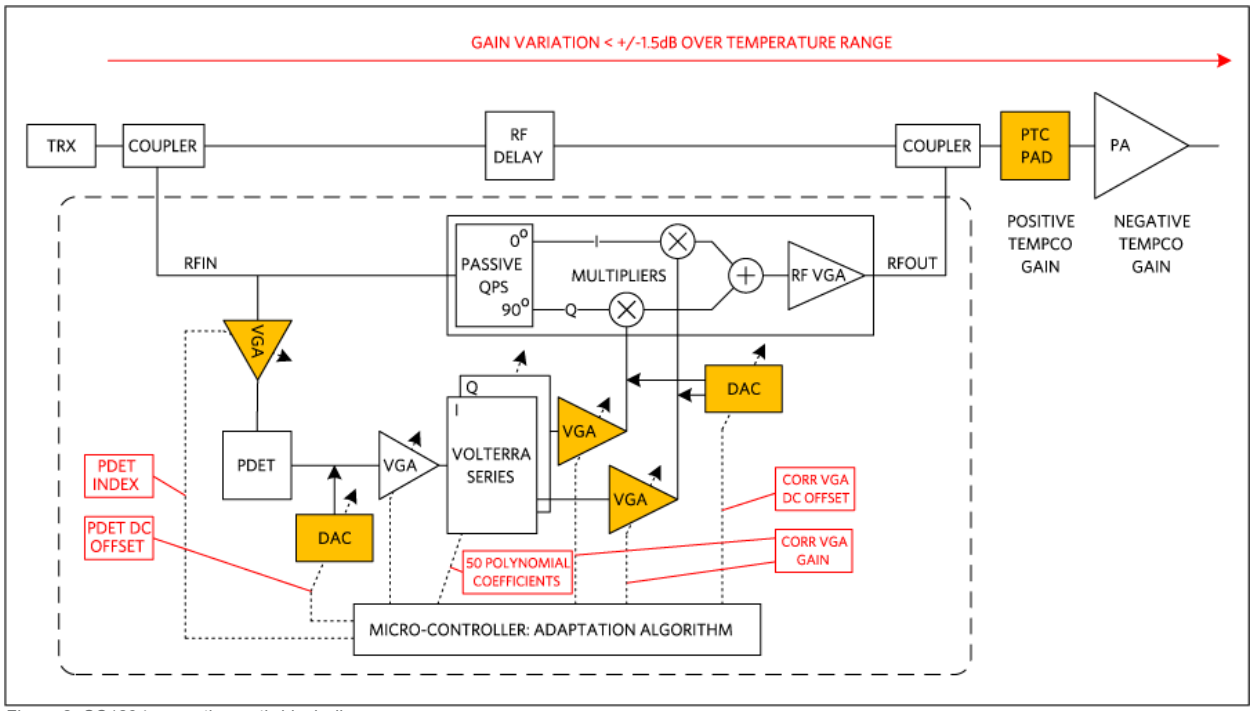

Figure 8. SC1894 correction path block diagram.

To help with GaN PA performance, a GaN PA mode was introduced in SC1894 firmware. Like for any linearization technology, the GaN PA must meet certain criteria for best linearized performance:

- Sufficient linearization bandwidth (> 3-5x signal BW)
- Well-behaved AM-AM and AM-PM response (monotonic, no kinks and flat at low power)
- Low-memory effects

5.2 RFIN Dynamic Range

When linearizing a GaN PA, the RFIN dynamic range is critical.

The RFIN power at P_{MAX} must be selected carefully:

- When the PA operates at maximum power, the RFIN level must be as high as possible (within the RFPAL data sheet limits).
- Since the PDET index and CORR VGA gains are fixed over the RFIN range, the correction power decreases in backoff. The higher the RFIN power at P_{MAX}, the higher it is in backoff, which is good for small signal-distortion linearization

The PA gain variation over temperature is also a very critical parameter that needs to be taken into account:

- The PA gain must vary as little as possible over temperature and batch to batch (ideally < ±1.5dB over the whole temperature range).
- Positive temp coefficient (PTC) pads can be used to compensate the (NTC) PA gain (see Figure 8).
- Although the FW compensates for the PA gain using the PDET-gain compensation. Large variation reduces the overall RFIN dynamic range.

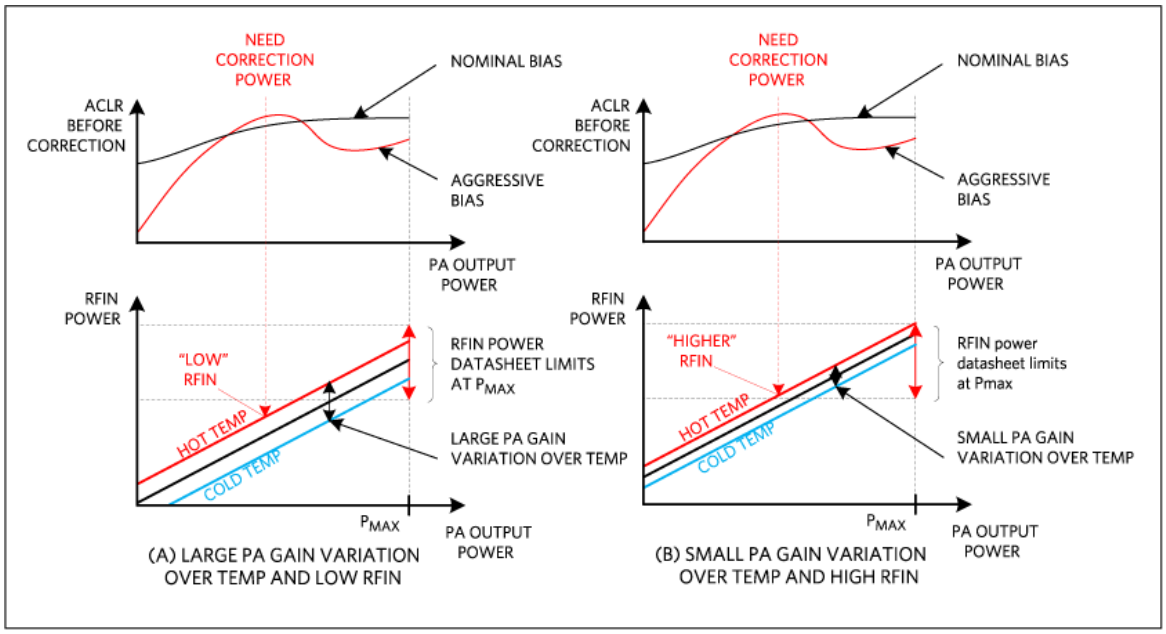

Figure 9. RFIN-range and PA-gain variation.

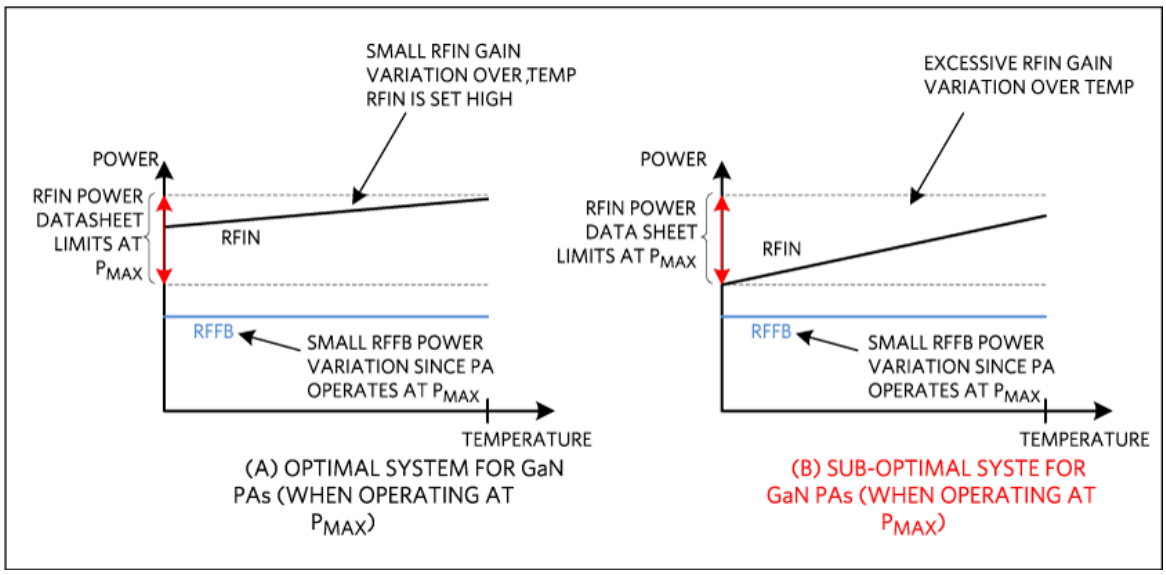

Figure 10. RFIN-range and PA-gain temperature variation.

6. Conclusion

1. Avoid overly aggressive bias that yields excessive small signal distortion.
2. For optimal RFIN dynamic range:
    1. Keep transceiver-to-PA output gain as constant as possible over temperature (target ±1.5dB over temperature range).
    2. Keep RFIN as high as possible within the RFPAL data sheet limits across all conditions.
3. To meet traditional techniques for linearizability:
    1. Allow VBW > 3-5x signal BW.
    2. Keep AM-AM response with gain ripple ² 2dB (unlinearized) across the entire operation range for best linearization performance.

3. The overall AM-to-PM phase rotation should not exceed 15° if the gain variation is less than 1dB. If the gain variation is greater than 1dB, then the AM-to-PM phase rotation should be less than 10° for good linearization using RFPAL.
4. It is recommended to improve PA gain flatness for wideband performance.
5. Keep the PA's memory effect under 5ns.

Related Parts	
SC1894	225MHz to 3800MHz RF Power Amplifier Linearizer (RFPAL)
SC2200	Dual RF Power Amplifier Linearizer (RFPAL)

More Information
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APPLICATION NOTE 6323, AN6323, AN 6323, APP6323, Appnote6323, Appnote 6323