PHASE-SHEDDING APPLICATION NOTE

1.0 INTRODUCTION

The purpose of the phase-shedding application is to allow for efficiency optimization of the voltage regulator across the variety of loads. This minimizes average energy consumption by optimizing the powertrain for specific load power states. Phase-shedding is achieved by disabling a desired number of phases in the system, and is initiated by a user defined signal. Maxim supports two different schemes with its Generation 4, 5 and 5.5 technology:

- Dynamic Phase-Shedding
- Static Phase-Shedding.

The main difference is that the dynamic approach allows for changing the number of active phases at any point of time, while static phase-shedding occurs only at startup. Detailed differences and implementation will be explained in this application note.

2.0 BASIC CONTROL ARCHITECTURE

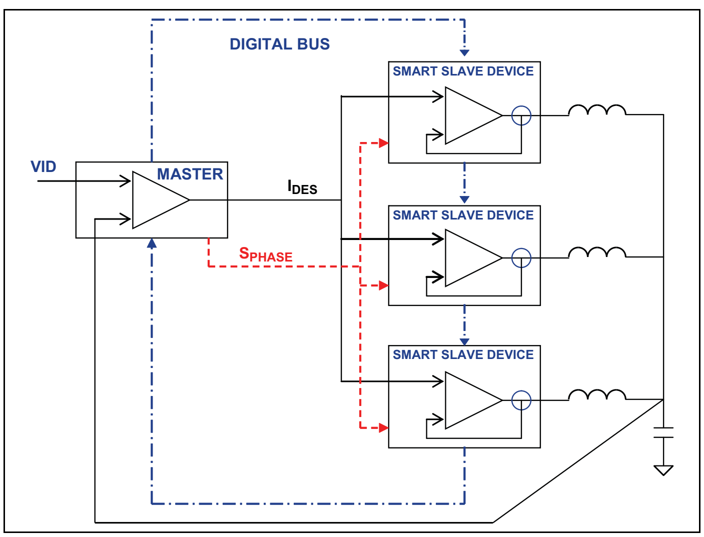

Figure 1: Basic Control Architecture

Desired output current (I_{DES}) is a differential signal communicated to the slaves by an Ides bus lines (differential pair consisting of I_{DES}_N and I_{DES}_P). The slaves respond to the Ides signal by producing a DC current proportional to the differential Ides voltage, with zero volts commanding zero amps and 1.6V corresponding to the full scale current of the slave (programmable by a selection resistor on the master). The slaves use their own internal control and current sense to switch the power FETs in order to control their inductor currents at the correct DC level, phase and frequency.

A proprietary communication bus (daisy-chain digital bus, DBI/DBO) sends out the configuration settings from the master to the slaves during the initial power-up sequence. It is also used to report slave status information back to the master during operation.

The system clock signal (S_{PHASE}) is broadcast from the master to each of the slaves.

3.0 PROGRAMMABLE DROOP

To achieve the correct system load line, the proper gain must be chosen through resistor settings on the VT11xxM master. System gain relates total system current to output voltage droop where the system gain (in current per droop voltage) is described by Equation 1 (more details can be found in the appropriate Maxim master data sheets).

Equation 1

$$\frac{I_{SLAVE}}{V_{DROOP}} = \frac{R2}{R1} \bullet \frac{I_{MAX}}{1.6} \bullet Gain$$

where,

I_{SLAVE} = *current per slave*
V_{DROOP} = *system droop*
I_{MAX} = *max current per slave*
Gain = *internal gain specified by one of the* R_{SEL} *resistors*

R1 and R2 are external resistors connected around the error amplifier as shown in Figure 2.

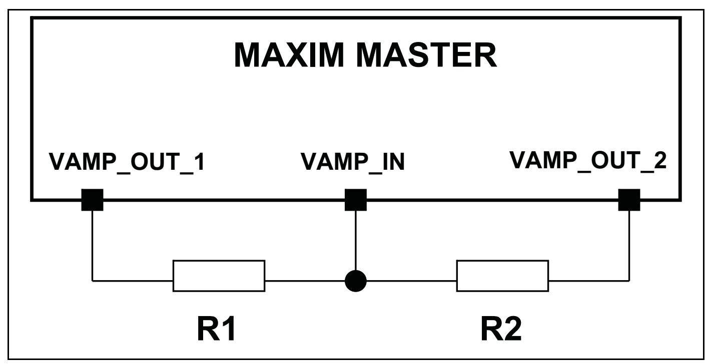

Figure 2: Master Diagram

When using phase-shedding, a desired number of phases are being disabled. As system droop is calculated for N phases, it is necessary to compensate for change in the phase count in order to maintain the same droop when changing the number of active phases. External resistors R1 and R2 are defining a portion of the total system gain and are very convenient to use in this case. Their ratio can be adjusted easily at the same time of phases being dropped when phase-shedding is initiated, which in effect keeps the total system gain constant.

For example, if we have an N-phase system that's set up such that when the PSIB signal is active we disable N-1 phases (leaving only one phase active), we should change as follows:

$$\frac{R2}{R1} \text{ should be changed to } N\left(\frac{R2}{R1}\right)$$

4.0 DYNAMIC PHASE-SHEDDING IMPLEMENTATION

The basic idea of dynamic phase-shedding application is presented in Figure 3. I_{DES}_N and I_{DES}_P lines both have a common mode level of 1.6V, which is detected by the slaves. If any of these lines is shorted to ground, the slave will register a low common mode and will stop regulating. When the common mode level of I_{DES} lines is back to normal, the slave will start switching again. This feature is used to achieve dynamic phase shedding on Maxim systems. Smart slave device(s) that will always remain on are called primary smart slaves, while the ones that can be disabled during Phase-Shedding mode are called secondary smart slave devices.

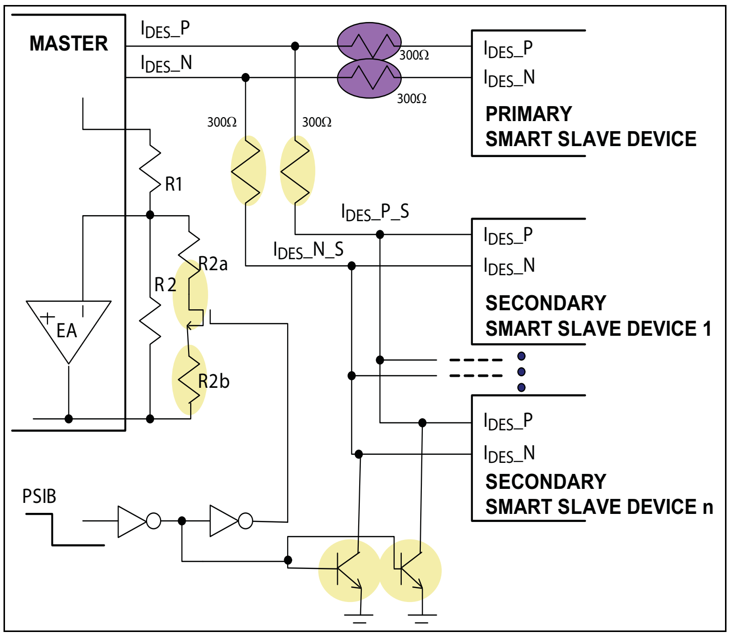

Figure 3: Dynamic Phase-Shedding Application

Secondary smart slave devices are getting I_{DES} command through the I_{DES}_N_S and I_{DES}_P_S lines that are isolated from the main I_{DES}_N and I_{DES}_P lines using 300Ω resistors. When dynamic phase-shedding is initiated, I_{DES}_N_S and/or I_{DES}_P_S lines are shorted to ground, which will disable the Secondary Smart Slave devices.

In order to preserve the total system gain when dynamic Phase-Shedding mode is active, the equivalent value of R2 (error amp feedback resistor) is appropriately adjusted at the same time.

Typical application schematic is shown in Figure 4.

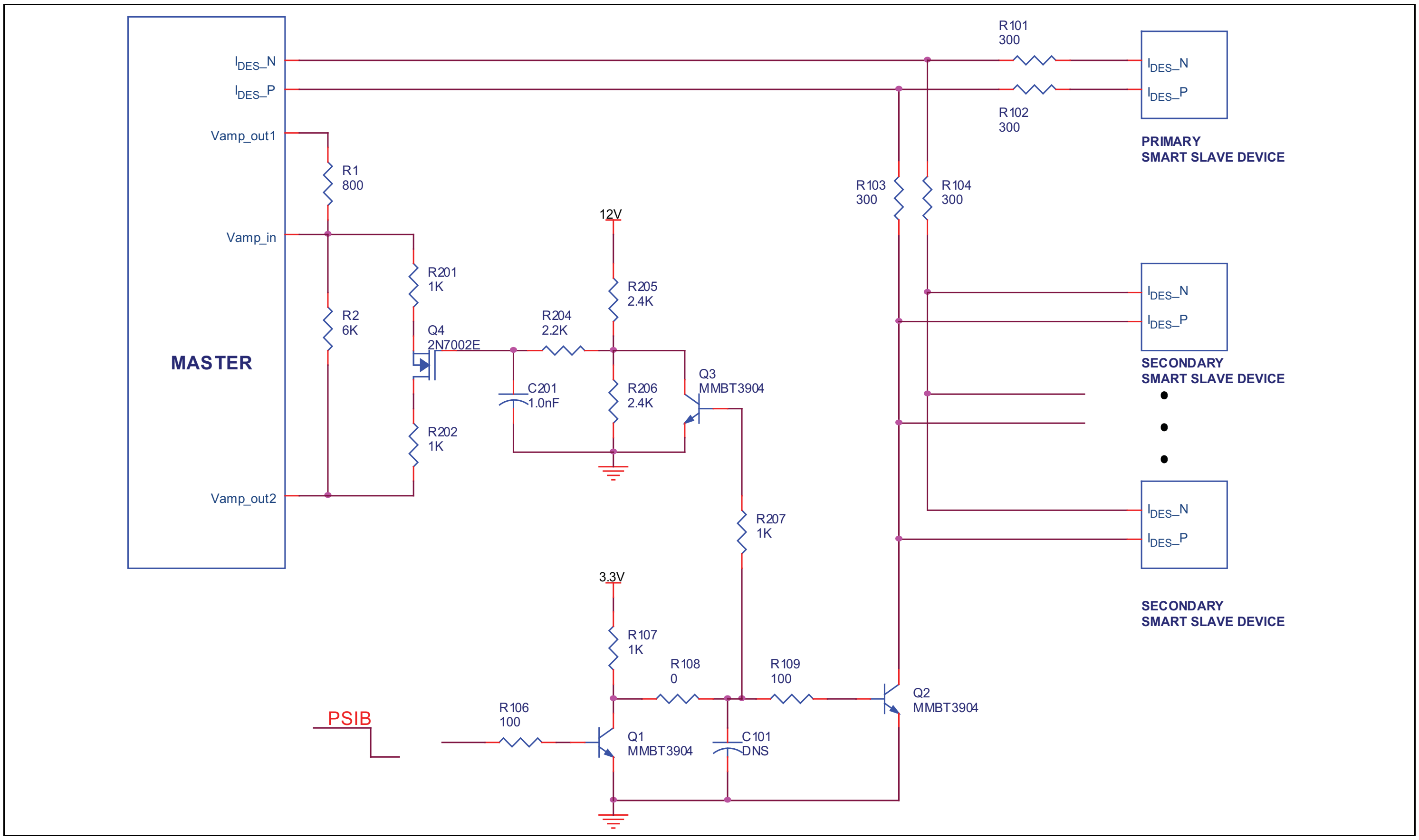

Figure 4: Typical Application Schematic

- In the presented schematic, it is assumed that the Phase-Shedding Initiation signal (PSIB) is active-low.
- It is possible to adjust this schematic to a specific user's needs, as necessary.
- Scope shots of typical dynamic phase-shedding entry and exit are presented in Figure 5 through Figure 8.

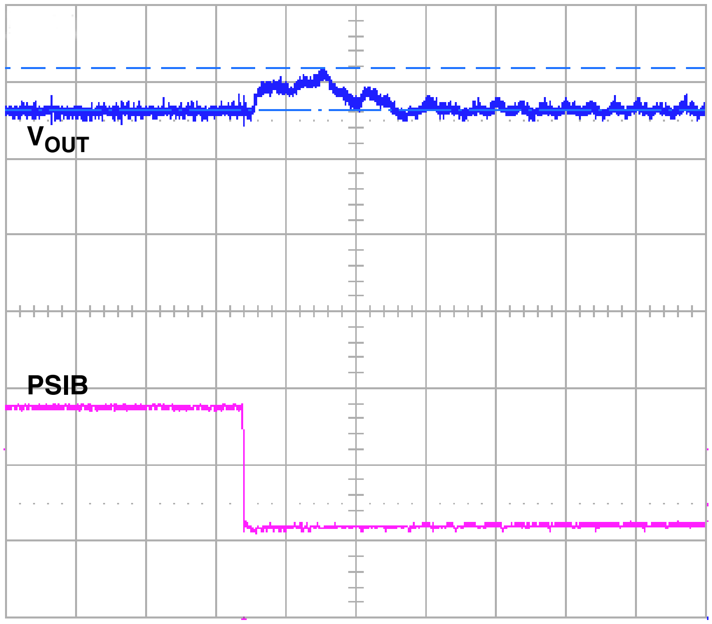

Figure 5: Entry to PSI Mode at 0A

V_{OUT} (20mV/div)
PSIB (2V/div)
Time Scale: 5µs/div

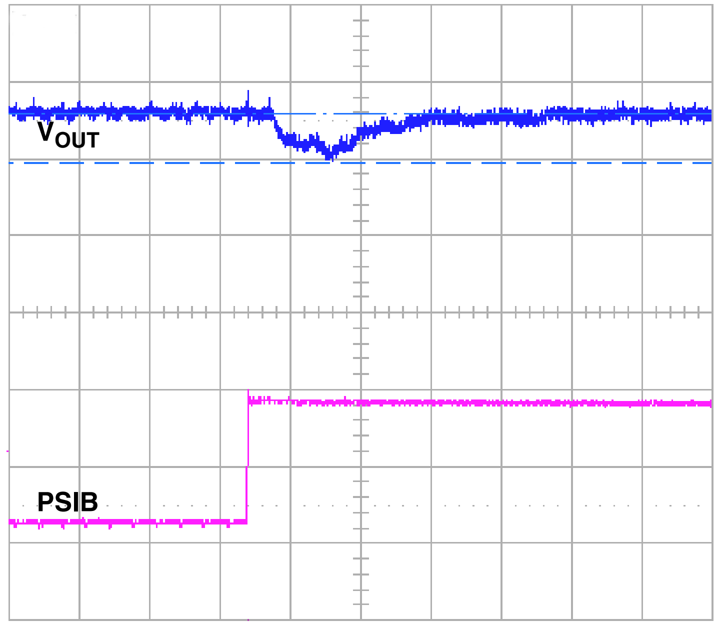

Figure 7: Exit From PSI Mode at 0A

V_{OUT} (20mV/div)
PSIB (2V/div)
Time Scale: 5µs/div

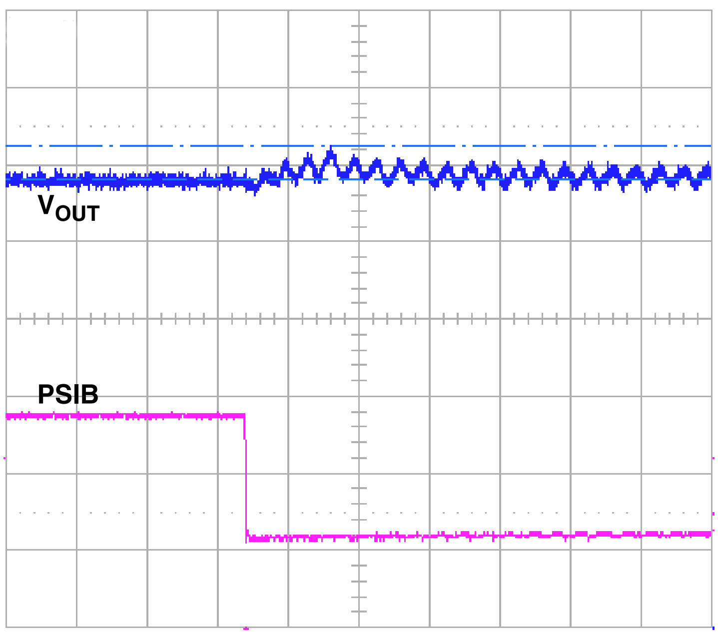

Figure 6: Entry to PSI Mode at 20A

V_{OUT} (20mV/div)
PSIB (2V/div)
Time Scale: 5µs/div

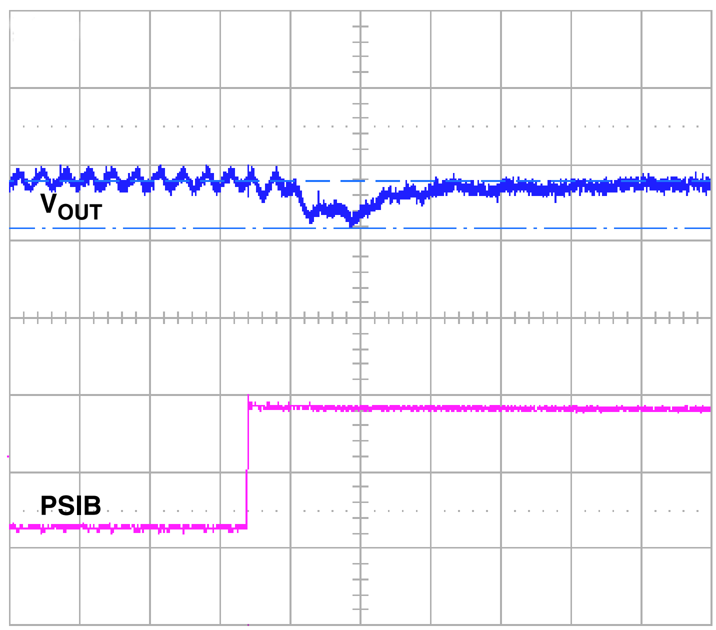

Figure 8: Exit From PSI Mode at 20A

V_{OUT} (20mV/div)
PSIB (2V/div)
Time Scale: 5µs/div

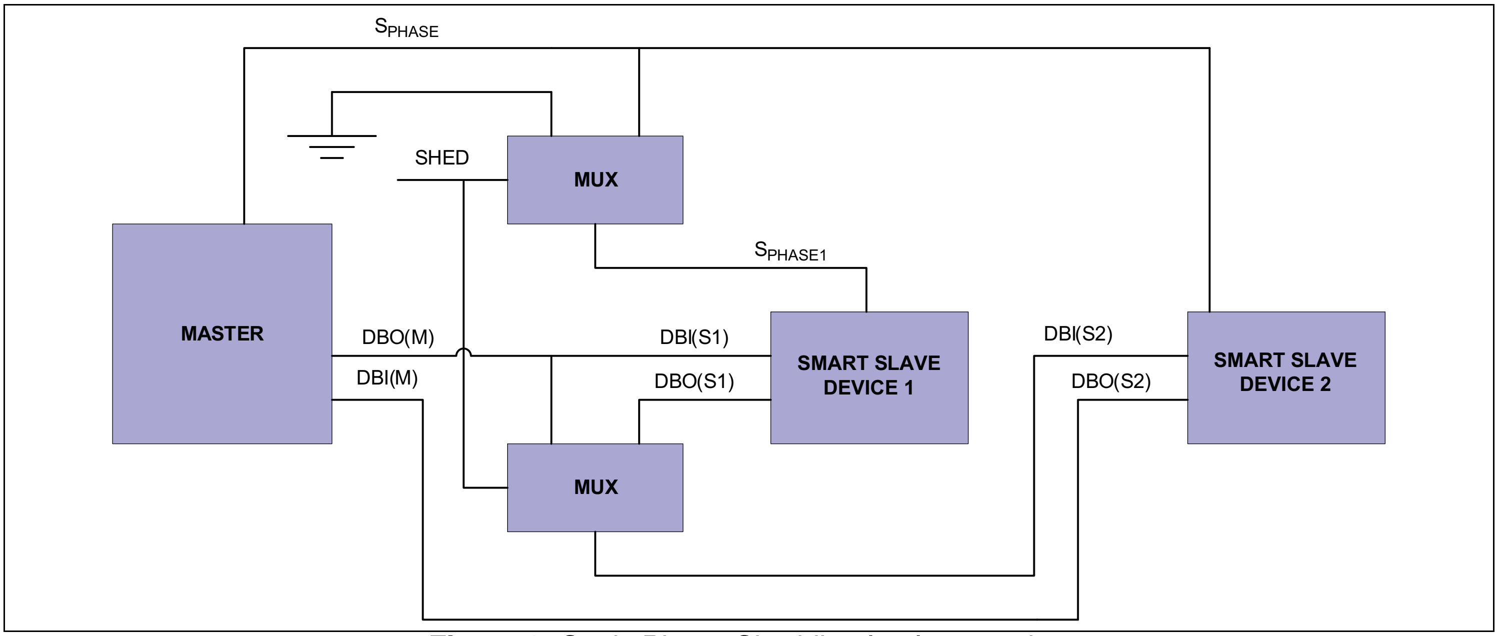

Figure 9: Static Phase-Shedding Implementation

5.0 STATIC PHASE-SHEDDING

If there is a need to have one board and one bill of materials that can support different system requirements (different sizes of memory cards being loaded, for example), including the number of phases that are being used, and still have optimized solution for each set of requirements, Maxim suggests a static phase-shedding approach.

The static phase-shedding approach assumes that all of the changes (phase disabling, gain and any other needed adjustment) will occur at the startup. No additional changes are required during the normal operation of the system.

Smart Slave devices that are being disabled have to be isolated from the digital daisy-chain bus. Each smart slave device is required to have two additional multiplexers. One of them is forwarding appropriate digital bus signal to the next slave in daisy chain, and the other is forwarding S_{PHASE} signal from the master or shorting the S_{PHASE} input of the slave to ground; hence, disabling the slave).

Based on Figure 9, here is an example of how the circuit works:

- In the normal mode of operation, the digital bus MUX is forwarding the DBO(S1) signal to the smart slave device 2, and the S_{PHASE} MUX is forwarding S_{PHASE} signal from the master to the Smart Slave Device 1. In this way, both slaves are enabled.
- When SHED signal is low (the appropriate level to initiate the static phase-shedding) digital bus MUX is forwarding DBO(M) signal to the Smart Slave Device 2 (isolating Smart Slave Device 1 from the digital bus), and S_{PHASE} MUX is shorting S_{PHASE} input of the Smart Slave Device 1 to GND (which will disable Smart Slave Device 1). In this way, only the Smart Slave Device 2 will be working in the system, and being recognized and configured by the Master.

A typical application schematic is shown in Figure 10.

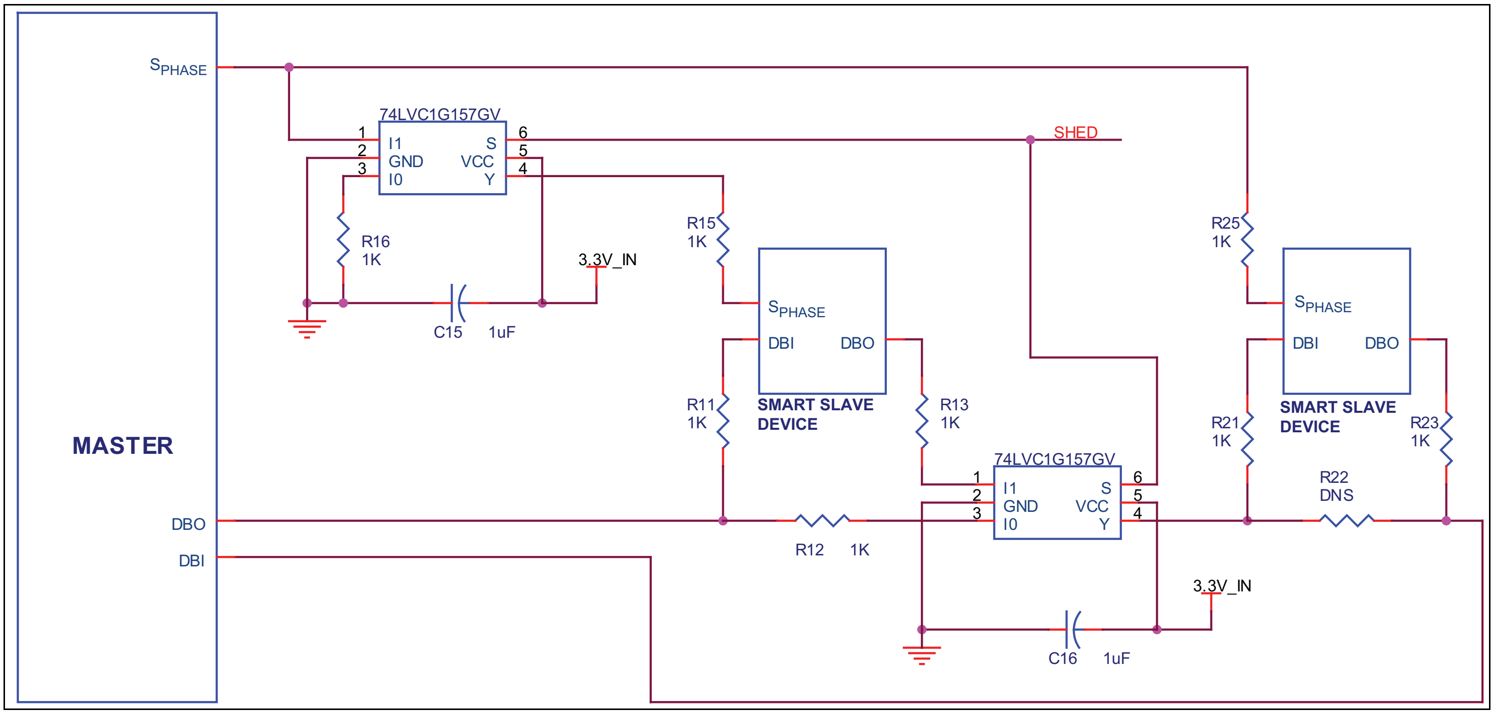

Figure 10: Static Phase-Shedding Typical Application

Gain adjustment and any other needed optimization through R_SEL resistors is achieved by the same circuitry as for gain adjustment in dynamic phase-shedding. This will be initiated by SHED signal provided by the user. The assumption is that this signal will also be active-low.

If static phase-shedding initializing signal (SHED) is not present at the startup, a separate simple circuitry is needed to temporarily recycle the master in order to properly configure the system. An example of that circuitry is given in Figure 10.

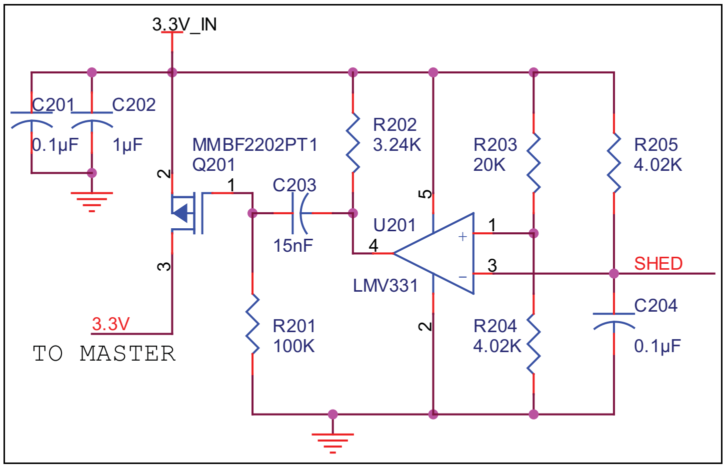

Figure 11: Phase-Shedding Circuitry

The circuitry in Figure 11 can be described as follows: during the normal mode of operation, the SHED signal is high and the output of U201 is low. This means that voltage across C203 is zero, the gate of the Q201 is at zero level and Q201 is on (supplying voltage to the master). When the SHED signal changes from high to low, the output of the U201 will go high (to 3.3V) and, since it's not possible to instantly change the voltage across the capacitor (C203), the voltage at the gate of Q201 will briefly go to the 3.3V level, turning Q201 off. C203 will charge up through R201 and R202 and the gate of Q201 will go back to zero, turning the FET on again. In this way, the master bias voltage is recycled, allowing for proper reconfiguration.