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APPLICATION NOTE 6014

HOW TO MEASURE CAPACITY VERSUS BIAS VOLTAGE ON MLCCS

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Abstract: The application note explains how to always check the capacitor's datasheet to see how the capacitance varies with the bias voltage. Using the presented circuit, a dual power supply, and a voltmeter, it is quite simple to measure the DC bias characteristic of a high-capacity MLCC.

Introduction

High-capacity, multilayer ceramic capacitors (MLCC) have a property often not well understood by electronic designers: the capacitance of these devices varies with applied DC voltage. This phenomenon is present in all high-dielectric constant, or Class II capacitors (B/X5R R/X7R, and F/Y5V characteristic). However, the amount of variation can differ considerably among different MLCC types. A good application note on this topic was written by Mark Fortunato.[1]

The conclusion of this application note is that you should always check the capacitor's datasheet to see how the capacitance varies with the bias voltage. But what if the data sheet does not include this information? How can you determine how much capacitance is lost under the conditions in your application?

Theory for Characterizing Capacitance versus Bias Voltage

A circuit to measure the DC bias characteristic is shown in **Figure 1**.

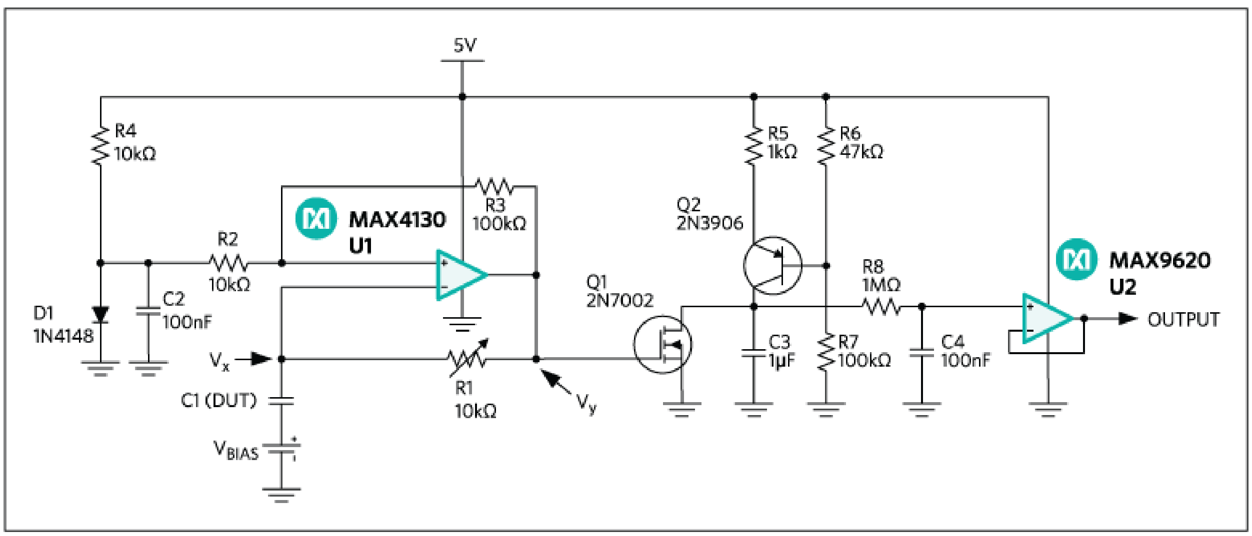

Figure 1. Circuit to characterize capacitance versus bias voltage.

This circuit is built around op amp, U1 (MAX4130). The op amp acts as a comparator with feedback resistors R2 and R3 adding hysteresis. D1 sets a threshold above GND so that no negative supply voltage is needed. C1 and R1 form a feedback network to the negative input, which makes the circuit operate as an RC oscillator. Capacitor C1, the device under test (DUT), serves as the C in this RC oscillator; potentiometer R1 is the R.

The voltage waveforms of the op amp output pin, V_y, and the junction between R and C, V_x, are shown in **Figure 2**. When the output of the op amp is at 5V, capacitor C1 is charged by R1 until it reaches the upper threshold; thus, forces the output to 0V. Now the capacitor is discharged until V_x reaches the lower threshold, thus forcing the output back to 5V. This process repeats, resulting in a stable oscillation.

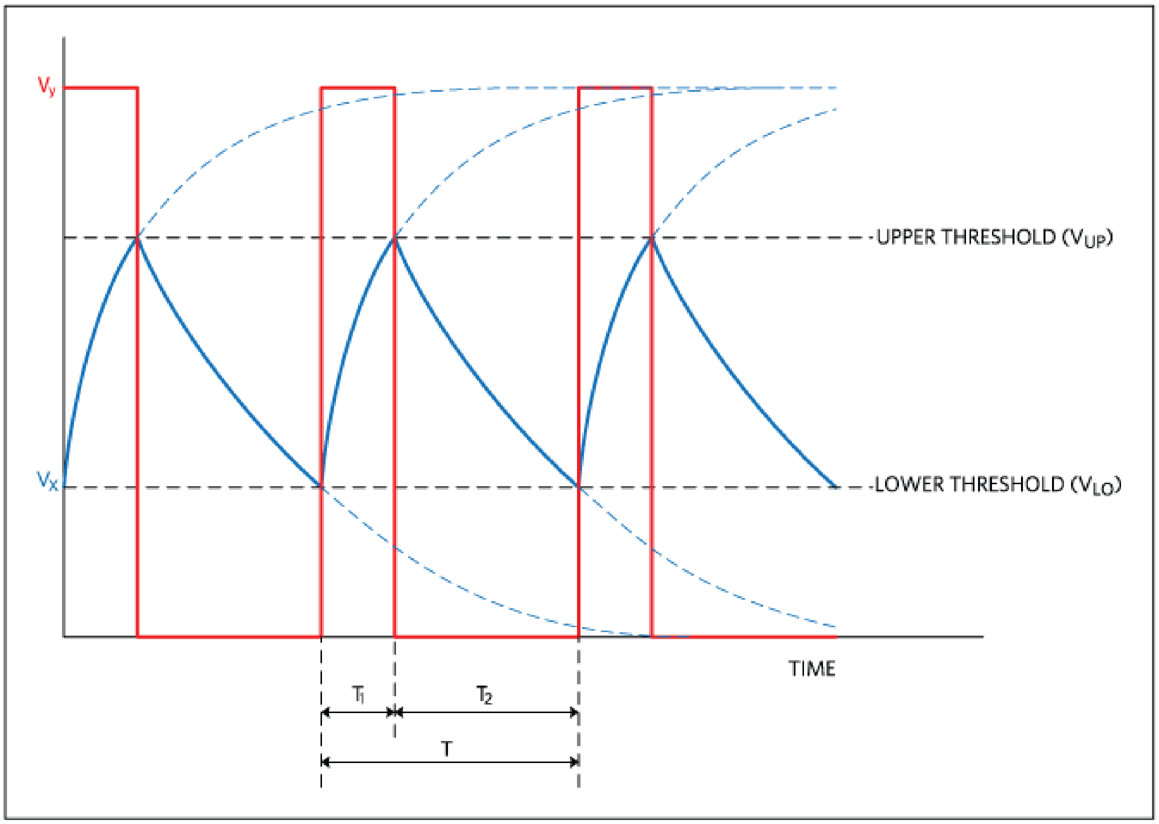

Figure 2. Oscillation voltages V_x and V_y.

The oscillation period depends on the values of R, C, and the upper and lower thresholds V_{UP} and V_{LO}:

$$T_1 = RC \ln\left(\frac{5V-V_{LO}}{5V-V_{UP}}\right) = \alpha RC$$

$$T_2 = RC \ln\left(\frac{V_{UP}}{V_{LO}}\right) = \beta RC$$

$$T_1 = \frac{\alpha}{\beta} T_2$$

$$T = T_1 + T_2 = \left(1+\frac{\alpha}{\beta}\right)T_2$$

Since 5V, V_{UP} , and V_{LO} are constant, then T_1 and T_2 are proportional to RC. This is often referred to as the RC time constant.

The threshold of the comparator is a function of V_y, R2, R3, and the forward voltage of D1 (V_{DIODE}):

$$V_{THRESHOLD} = V_{DIODE} \frac{R3}{R2 + R3} + V_y \frac{R2}{R2 + R3}$$

where V_{UP} is the threshold for V_y = 5V, and V_{LO} is the threshold for V_y = 0V. With the given values these thresholds yield to approximately 0.55V for V_{LO} , and 1.00V for V_{UP} .

The circuit around Q1 and Q2 converts the cycle time into a proportional voltage. This works as follows. MOSFET Q1 is controlled by the output of U1. During T_1, Q1 is on, clamping the voltage on C3 to GND. During T_2 , Q1 is off, allowing the constant current source (Q2, R5, R6, and R7) to linearly charge C3.[1] As T_2 is increased, the voltage on C3 becomes higher. **Figure 3** shows the voltage on C3 over three cycles.

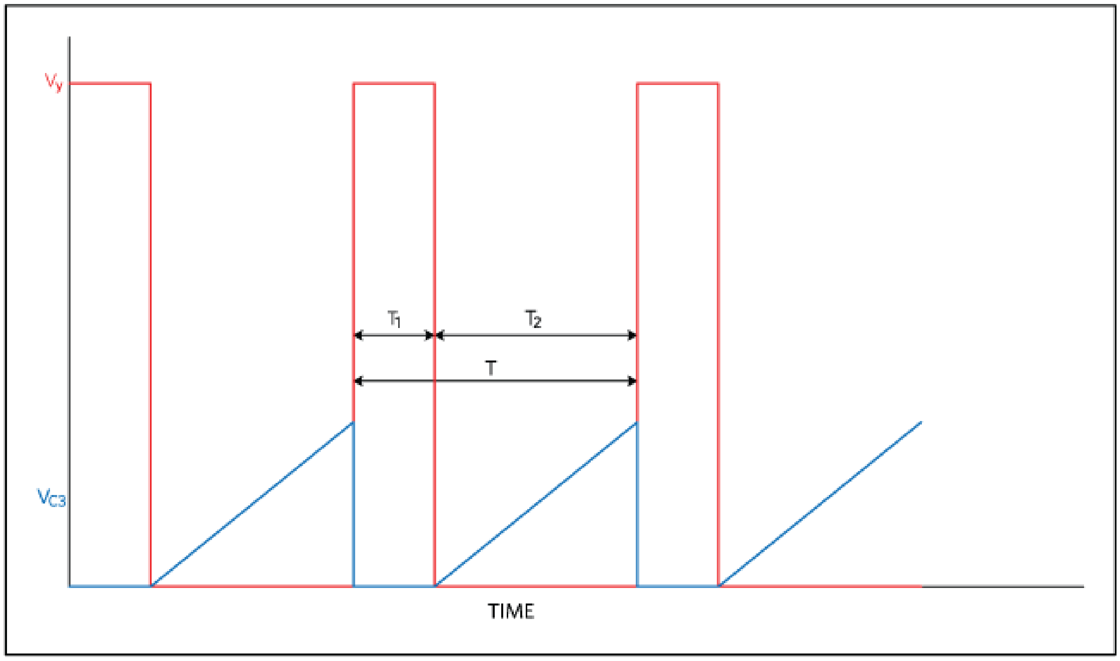

Figure 3. C3 is clamped to GND during T_1 and linearly charged during T_2 .

The average voltage on C3 (V_{C3}) is equal to:

$$\overline{V_{C3}} = \frac{1}{T}\int_0^{T_2} \frac{I}{C_3}\, t\,dt = \frac{I}{2TC_3}\,[t^2]_0^{T_2} = \frac{IT_2^2}{2TC_3} = \frac{IT_2^2}{2C_3\left(1+\frac{\alpha}{\beta}\right)T_2} = \frac{I}{2C_3\left(1+\frac{\alpha}{\beta}\right)}\,T_2$$

Since I, C3, α , and β are all constant, the average voltage on C3 is proportional to T_2 and, therefore, also to C1.

Lowpass filter R8/C4 filters the signal while low-offset op amp U2 (MAX9620) buffers the output so that it can be measured with any voltmeter.

Before measurements can be made, this circuit requires a simple calibration. First the DUT is installed in the circuit, and V_{BIAS} is set to 0.78V (the average of V_{LO} and V_{UP}) so the actual average (DC) voltage across the DUT is 0V. The output voltage will vary when potentiometer R1 is varied. Adjust R1 until the output voltage reads 1.00V. Under these conditions, the peak voltage on C3 is around 2.35V. The bias voltage can be modified and the output voltage will show the resultant percentage change in the capacitance. For example, if the output voltage is 0.80V, the capacitance at that particular bias voltage is 80% of the capacitance at 0V bias.

Lab Tests Confirm the Theory

The Figure 1 circuit was built on a small PCB. The first measurement was done using a random 10µF capacitor. **Figure 4** and **Figure 5** show the signals under 0V and 5V bias conditions, respectively.

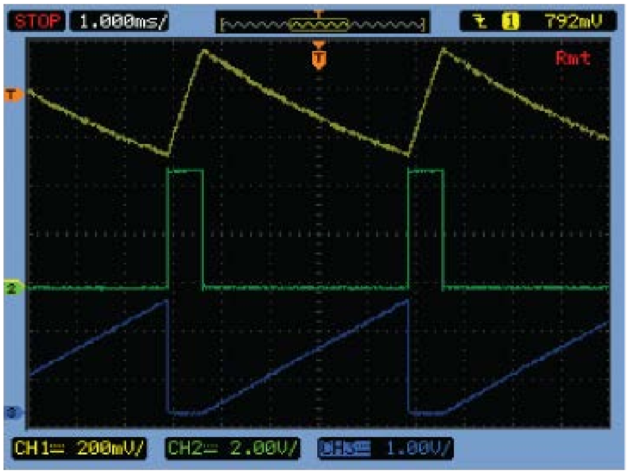

Figure 4. Measurement with V_{BIAS} = 0V; Ch1 = V_x ; Ch2= V_y Ch3 = V_{C3} . R1 was adjusted so the voltmeter showed 1.000V.

To prevent saturation of Q2, the voltage peak on the collector (= V_{C3}) should stay below the emitter voltage minus the emitter-collector saturation voltage, which yields to approximately 4V.

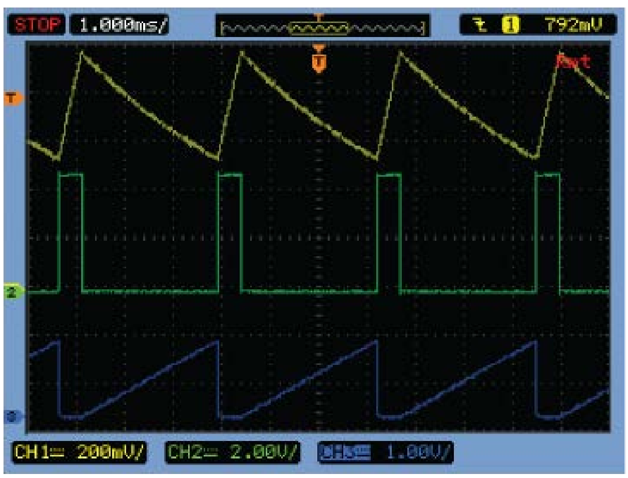

Figure 5. Measurement with V_{BIAS}= 5V. The oscillation period has clearly decreased due to the reduced capacitance. Ch1 = V_x; Ch2 = V_y; Ch3 = V_{C3}. The voltmeter reads 0.671V.

At 0V bias, potentiometer R1 was adjusted so the voltmeter showed 1.000V. At 5V bias, the voltmeter showed 0.671V, indicating that 67.1% of the capacitance remained. With an accurate counter, the total period, T, was also measured. T was 4933µs at 0V bias and 3278µs at 5V, indicating that 66.5% (= 3278µs/4933µs) of the capacitance remained. These values match very well, demonstrating that the circuit design can accurately measure the capacitance drop as a function of the bias voltage.

A second measurement was performed, now using a known 2.2µF/16V capacitor taken from a sample kit supplied by Murata (part number = GRM188R61C225KE15). In this measurement the values were recorded over the entire operating 0 to 16V range. The relative capacitance was determined by measuring both the output voltage of the circuit and the actual oscillation period. Additionally, data was collected from the Murata® Simsurfing tool, which can provide the DC bias characteristic for this particular part based on measurements performed by Murata. **Figure 6** shows all the results. Both graphs with our measurement data show almost identical results, which proves that the time-to-voltage circuit performs well over a larger dynamic range. There is some difference between the data from the Simsurfing tool and our measurements, but the shapes of the curves are similar.

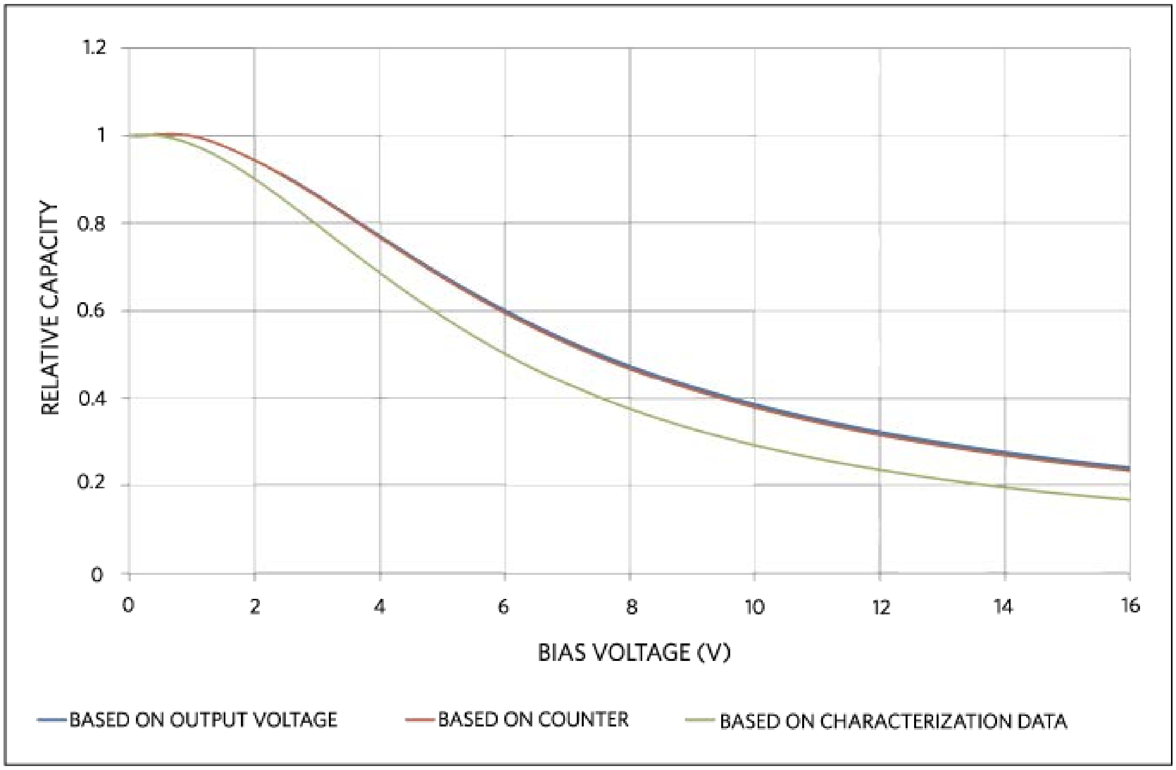

Figure 6. Relative capacity as a function of bias voltage for a 2.2µF/16V MLCC. The values are normalized to the capacitance at 0V bias. The blue curve is based on measuring the output voltage of the circuit; the red curve is based on the measurement of the oscillation period; the green curve is based on characterization data supplied by the Murata Simsurfing tool.

Conclusion

Using the presented circuit, a dual power supply, and a voltmeter it is quite simple to measure the DC bias characteristic of a high-capacity MLCC. A quick bench test will reveal how much the capacitance decreases as a result of the applied bias voltage.

Reference

1. Fortunato, Mark, "Temperature and Voltage Variation of Ceramic Capacitors," EDN, December 4, 2012, http://www.techonline.com/electrical-engineers/education-training/tech-papers/4410874/Temperature-and-Voltage-Variation-of-Ceramic-Capacitors. Also found as Maxim Integrated application note 5527, "Temperature and Voltage Variation of Ceramic Capacitors, or Why Your 4.7µF Capacitor Becomes a 0.33µF Capacitor," by Mark Fortunato.

Footnotes

1. This will only be linear when using a capacitor with constant capacitance up to 5V bias voltage (MKS, MKT, etc).
2. To prevent saturation of Q2, the voltage peak on the collector (= V_{C3}) should stay below the emitter voltage minus the emitter-collector saturation voltage, which yields to approximately 4V.

Related Parts		
MAX4130	Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply Rail-to-Rail I/O Op Amps	Free Samples
MAX9620	High-Efficiency, 1.5MHz Op Amps with RRIO	Free Samples

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