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APPLICATION NOTE 5980

# SETTING UP UART COMMUNICATION WITH THE MAX78615+LMU AND THE MAXREFDES14# ISOLATED ENERGY MEASUREMENT SUBSYSTEM

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*Abstract: The MAXREFDES14# provides a compact solution for isolated energy measurement featuring the MAX78615+LMU. This reference design is configured for SPI communication by default. This application note describes how to configure the MAX78615+LMU for UART communication and gives some example transactions for that interface.*

## Configuring the Serial Interface

All of Maxim Integrated's energy measurement devices provide support for three different serial interfaces, which allow for maximum flexibility when interfacing with different host processors and applications. However, only one serial interface can be active at a time. During power-up, the Maxim Integrated energy measurement device will poll the state of its hardware interface pins to determine which serial protocol will be active. To change the communication mode after the part is already on, the user must perform a power cycle to the device with the new configuration logic applied to the interface pins. The MAX78615+LMU features two interface pins: MP0/IFC1 on pin 16 and IFC0 on pin 2. **Table 1** shows which serial interface corresponds with the logic state of these pins upon power-up.

**Table 1. Serial Interface Selection Logic**

Interface Mode	IFC1	IFC0
SPI	X	0
UART	0	1
I <sup>2</sup> C	1	1

The **MAXREFDES14# system board** is shown in **Figure 1**. The design features 10k pull-down resistors on both IFC0 and IFC1, which select the SPI mode by default. To enable UART communication instead of SPI, R10 in the schematic should be pulled up to  $V_{CC}$  instead of pulled down to GND. Since MP0 can be used as a “multipurpose” pin after the interface is selected, a pull-down is recommended instead of connecting the pin directly to GND. With these connections, the **MAX78615+LMU** will be configured for UART mode during power-up. The default settings for the UART interface are 38,400 baud, 8 data bits, no parity, and one stop bit.

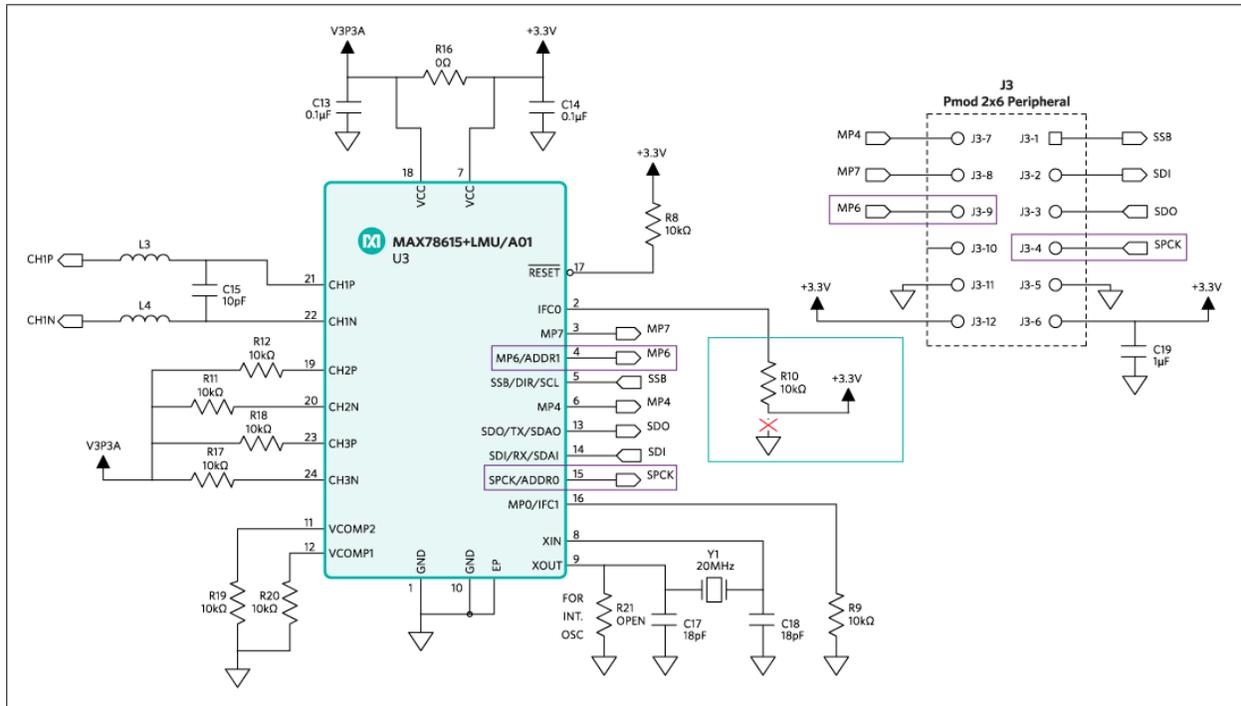


Figure 1. MAXREFDES14# schematic—nonisolated side.

## Setting the SSI ID

The protocol used for communicating via UART is the Simple Serial Interface, or SSI. One major difference between the SPI and UART interfaces is that, whereas an SPI master selects a device through a hardware chip-select (SSB on the MAX78615+LMU), the UART interface establishes communication by using the defined SSI ID of each device. The MAX78615+LMU can have an SSI ID from 1 to 255, and the SSI ID is chosen in two steps. The DEVADDR[5:0] register bits in the MAX78615+LMU are used to define the upper 6 bits of the SSI ID. The lowest 2 bits of the SSI ID are set by the hardware pins MP6/ADDR1 and SPCK/ADDR0 pins. The state of these pins is sampled upon power-up in the same way the MP0/IFC1 and IFC0 pins are sampled to determine the serial interface. The MAX78615+LMU SSI ID is equal to the total device address + 1. Thus, if DEVADDR[5:0] = 000000 and ADDR1 = ADDR0 = 0, the SSI ID will be 1. Since 255 is the maximum allowable SSI ID, a total device address of ‘FF’ is unsupported. The MAX78615+LMU has a default DEVADDR = 0.

## Establishing Communication

Once the MAX78615+LMU is powered in UART mode and the SSI ID is set, data can be sent over the

UART interface. Pulling down ADDR1 and ADDR0 will configure the MAX78615+LMU with an SSI ID of 1. The following packet can be sent to select the device:

**Table 2. SSI Select Target Packet**

Byte No.	Data	Description
1	0xAA	Header Byte
2	0x04	Byte Count
3	0xC1	Select SSI ID Target '1'
4	0x91	Checksum

The checksum was calculated by adding the three previous bytes and taking the two's complement of the lowest byte of the sum. If configured properly, the MAX78615+LMU will respond with the single-byte response 0xAD, which is an acknowledgement without data. **Figure 2** shows a logic analyzer capture of the transaction.



*Figure 2. SSI select target logic waveform.*

### Changing the SSI ID

The SSI ID can be configured both in firmware and in hardware. The DEVADDR register can be written through any of the serial interfaces—SPI, I<sup>2</sup>C, or UART. To write the contents of a register via UART, the “Set Read/Write Address” command should be issued, followed by two address bytes sent LSB first that represent the register byte address. The “Write 3 Bytes” command is next, followed by three data bytes that are sent LSB first. Only the lowest byte of DEVADDR is used to determine the SSI ID; the upper two bytes are unused. The following packet can be sent to set DEVADDR register to 1. The MAX78615+LMU should respond with a ‘0xAD’—acknowledge without data.

Table 3. SSI DEVADDR Write Packet Example

Byte No.	Data	Description
1	0xAA	Header Byte
2	0x0A	Byte Count
3	0xA3	Set Read/Write Address [15:0]
4	0x69	DEVADDR register address [7:0]
5	0x00	DEVADDR register address [15:8]
6	0xD3	Write 3 Bytes Command
7	0x01	Data Byte Low
8	0x00	Data Byte Mid
9	0x00	Data Byte High
10	0x6C	Checksum

Initially, the new contents of the DEVADDR register will not be saved to flash. To store the device address in the on-chip flash memory, the flash access command must specifically be called. Failure to do so will result in the device loading the previously stored values to the registers upon the next power cycle. The COMMAND register, located at word address 0, can be used to initiate calibration, perform software reset, or store register data to flash memory. To access the flash storage, write 0xACC2 to the upper bytes of the COMMAND register. The following packet can be sent to store register contents to flash:

Table 4. SSI Flash Access Command Packet Example

Byte No.	Data	Description
1	0xAA	Header Byte
2	0x0A	Byte Count
3	0xA3	Set Read/Write Address [15:0]
4	0x00	COMMAND register address [7:0]
5	0x00	COMMAND register address [15:8]
6	0xD3	Write 3 Bytes Command
7	0x00	Data Byte Low
8	0xC2	Data Byte Mid
9	0xAC	Data Byte High
10	0x68	Checksum

Once this step is performed, the register contents will be loaded with the new flash contents on the next power-up.

## Distinguishing between DEVADDR, the Device Address, and the SSI ID

Due to the implementation and naming convention used, some clarification should be made between DEVADDR, the device address, and the SSI ID. DEVADDR is the name of the register that stores user programmable data to set the device address. The actual device address, however, is a combination of the lower six bits of DEVADDR and the state of the ADDR1 and ADDR0 pins on device power-up or reset. The DEVADDR[5:0] bits correspond to the upper six bits of the device address, and ADDR1 is assigned to bit 1 and ADDR0 is assigned to bit 0. Once the device address is set, the SSI ID is simply the device address + 1. In the above example, if DEVADDR[5:0] = 1 and ADDR1 = ADDR0 = 0, the new device address after power up or reset will be 4, which will make the SSI ID a value of 5 in the above example.

### Summary

The MAX78615+LMU featured on the MAXREFDES14# Isolated Energy Measurement Subsystem

Reference Design contains support for SPI, I<sup>2</sup>C, and UART interfaces. The reference design has the SPI interface configured by default. By changing the logic state of the hardware pins upon power-up, the UART interface on the MAX78615+LMU can be enabled. Once active, the SSI protocol is implemented to communicate via UART. Multiple devices can be connected in parallel by setting unique addresses through hardware and firmware. For a full description of the SSI protocol with example code, see the Maxim Integrated application note 5947, “[Using the Simple Serial Interface for Embedded Measurement Devices: 78M6610+LMU, 78M6610+PSU, and MAX78630+PPM](#)” and the data sheet for each specific device.

#### Related Parts

<a href="#">MAX78615+LMU</a>	Isolated Energy Measurement Processor for Load Monitoring Units	<a href="#">Free Samples</a>
<a href="#">MAX78700</a>	Multichannel, Isolated, Precision ADC	<a href="#">Free Samples</a>
<a href="#">MAXREFDES14</a>	Sonoma (MAXREFDES14#): Isolated Energy Measurement Subsystem Reference Design	

#### More Information

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