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APPLICATION NOTE 5963

SMT ASSEMBLY AND PCB DESIGN GUIDELINES FOR MAXIM'S FLIP-CHIP EXPOSED DIE QFN (NO LEADS) PACKAGES

By: Phil Eisenberg

Abstract: This document provides a checklist of the critical items to observe during PCB design and layout for systems using Maxim's flip-chip exposed die QFN packages. The objective is to ensure that projects operate successfully at initial power-up.

Introduction

The QFN or Quad Flat package No leads is an industry standard in plastic molded packages.

QFN packages have the following advantages:

- Small footprint per I/O resulting in significant PCB space savings.
- Superior electrical and thermal performance compared to leaded plastic packages.
- Utilizes standard surface mount assembly technology.
- Proven Board-Level Reliability (BLR) per IPC-9701 standards.

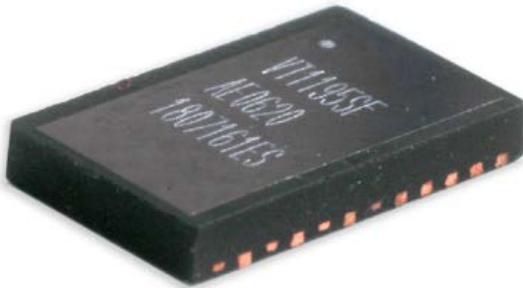


Figure 1a. QFN Isometric Top View.

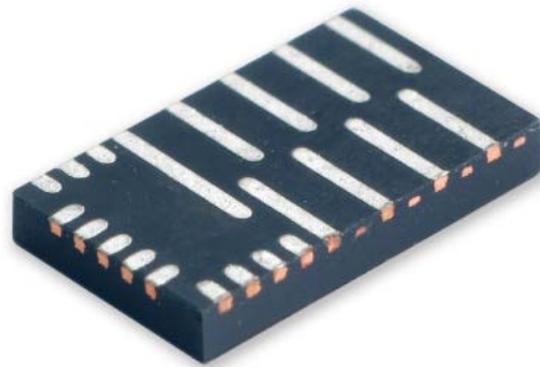


Figure 1b. QFN Isometric Bottom View.

Table 1. Key Attributes for Maxim QFN Packages

Typical Lead Pitch	Control 0.5mm/Power 1.0mm
Package Total Height	0.95mm
Lead Coplanarity	Leadless
Moisture Sensitivity Classification	MSL 1 2 Depending on Package Size

QFN Transportation Media

The QFN is shipped in standard polycarbonate conductive carrier tape with pressure-sensitive adhesive cover tape.

The tape and reel is sealed inside an ESD bag. A flat cardboard box is used to store the sealed bag with the appropriate label.

PCB Pad Design

A well-designed and manufactured printed circuit board (PCB) is required for optimum manufacturing yields and product performance.

Two types of land patterns are used for surface-mount devices:

- a. Solder Mask-Defined (SMD) pads have solder mask openings that are smaller than metal pads.
- b. Non-Solder Mask-Defined (NSMD) pads have metal pads that are smaller than the solder mask openings.

Maxim Integrated recommends the use of SMD pads for all integrated power devices to achieve optimum performance. SMD pads allow for greater copper trace width, which yields lower electrical and thermal resistance. QFN products that do not include integrated power devices (i.e., controllers) can use NSMD pad design.

There should NOT be any mixture of SMD and NSMD pads within the same QFN footprint.

Keeping with good Design For Manufacture (DFM), Maxim Integrated recommends the inclusion of fiducial marks in proximity to the QFN package to facilitate component placement.

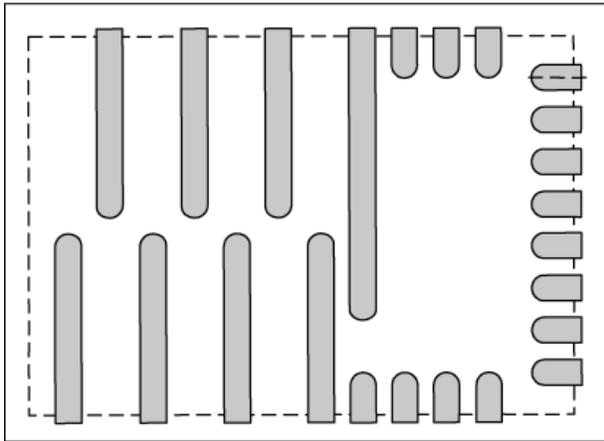


Figure 2. Example of Land Pattern.

PCB Fabrication and Control

Another important consideration in the PCB fabrication process should be the control of the solder mask opening size on the SMD pads.

- Solder mask openings shall be positioned over copper features without exposing FR4 material or copper edge.
- Some reduction in the copper width may be required if the final copper thickness is to be greater than or equal to 2oz.

Failure to comply with this recommendation may result in insufficient solder at the joint, leading to open connections or compromised solder joint reliability.

PCB Finish

Selection of an appropriate PCB pad surface finish is critical to ensuring optimum manufacturing of the final board assembly. Table 2 compares several popular surface finishes and summarizes Maxim Integrated's experience with each.

Stencil Design

The stencil thickness and pattern geometry determine the precise volume of solder paste deposited onto the device land pattern. Stencil alignment accuracy and consistent solder volume transfer is critical for uniform solder reflow. Stencils are usually made of stainless steel.

To enhance solder paste release, the walls of the apertures should be as smooth as possible. In addition, rounded corners and a trapezoidal cross-section enhance the release of solder paste from the aperture.

Maxim Integrated recommends the following:

- 5mil stencil thickness—Stencil aperture opening of 1 mil/side smaller than the pad size.
- 4mil stencil thickness—Stencil aperture opening should be 1:1 to PCB pad sizes.
- QFN stencil aperture must meet the industry-standard area ratio of > 0.66 .
- Stencil aperture tolerances must be tightly controlled, specifically for 0.5mm and 0.4mm pitch packages, as these tolerances can effectively reduce aperture size.
- Stencil fabrication—Laser-cut with electropolish. This provides a better release than the regular laser-cut stencil.

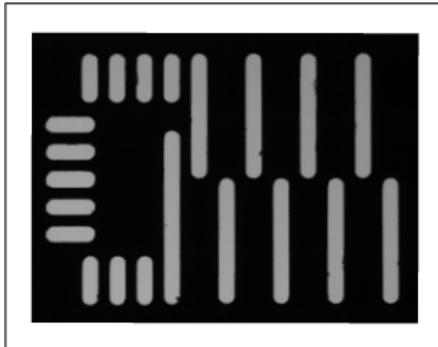


Figure 3. Stencil Sample.

Stencil design for E-type land pattern:

Pads are broken into multiple stencil apertures to reduce the paste volume (Figure 4) if it has an E-type package land pattern (shown in Figure 5).

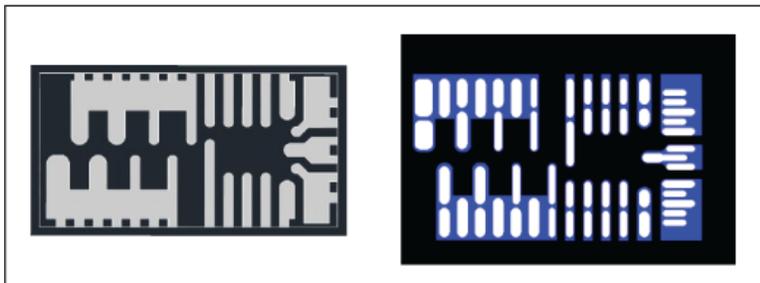


Figure 4. Example of E-type Package Outline (Left) and Stencil Apertures Design (Right). Blue color indicates solder mask openings. White color indicated stencil apertures.

Solder Paste

A low-residue, no-clean solder paste is commonly used in mounting QFNs. Water-soluble flux materials are not recommended as there is minimal stand-off (distance of package to PCB) and it will, therefore, be very difficult to clean flux trapped underneath the package.

A Type 3 (or finer) solder paste is recommended for 0.5mm pitch printing.

Maxim Integrated's recommended solder pastes are as follows:

- a. Eutectic – Indium SMQ-92J.
- b. Lead-free – Indium NC-SMQ230, Senju GRN360, Kester EM907 or Alpha OM338SAC305 solder alloy is highly recommended.

Solder Paste Printing

An automatic or manual stencil/screen printer can be used to distribute the solder paste onto the PCB lands.

A Design of Experiment (DOE) should always be used to establish optimum printing parameters. Most assemblers find that the following parameter ranges serve as good starting points:

- Print head speed: 1-2 inches/s
- Squeegee pressure: 0.75–1.5 pound per inch of squee-gee
- Under-stencil wiping: Every 3 boards
- Temperature: 23°C to 28°C
- Humidity: 30% to 60% RH

A stainless steel squeegee should be used.

Multiple printing of solder paste should be avoided for fine pitch devices as it may cause smearing of the solder paste.

QFN Placement

Conventional placement systems can be employed using either the QFN outline or the position of the leads as a placement guide.

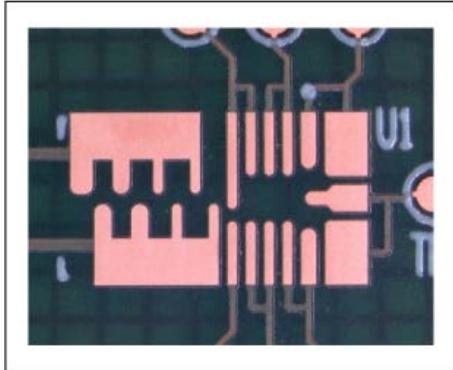


Figure 5. PCB Example of E-type package.

Table 2. Surface Finish Options

Finish Name	Description	Recommendation	Comments
Copper OSP	Organic Solderability Preservative (OSP)	Acceptable	
Silver Immersion	Thin-layer silver electroless plated	Acceptable	Silver immersion thickness must be controlled to 0.150 - 0.625µm to minimize micro voids at the solder joint.
Gold Immersion	Thin-layer gold electroless plated	Acceptable	
HASL	Hot air solder leveled	Acceptable	Vendor's process must be controlled to provide solder coverage of small solder mask openings.

Table 3. Eutectic Solder Reflow Temperature Profile Guidelines

Reflow Profile	Description of Characteristics	Process Windows
Preheat	Initial heating of component solder balls	2°C to 2.5°C/s
Thermal Soak	Solder paste dries out and flux activates	150°C to 170°C 95 to 100 sec
Reflow	Time above 183°C Peak reflow temperature	55 to 60 seconds 220°C
Cooling	Cooling rate	Max -4°C/s

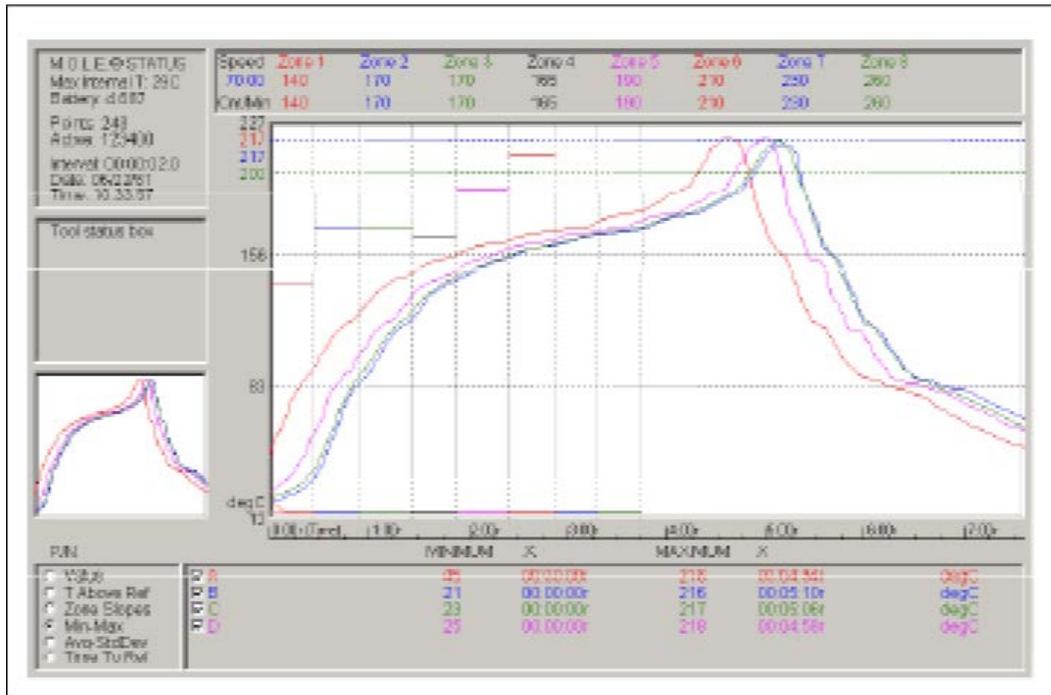


Figure 6. Eutectic Solder Reflow Temperature Profile.

Table 4. Temperature Profile Guideline

Reflow Profile	Description of Characteristics	Process Windows
Preheat	Initial heating of component leads	2.0°C to 2.5°C
Thermal Soak	Solder paste dries out and flux activates	150°C to 190°C, 80s to 85s
Reflow	Time above 217°C/Peak reflow temperature	70s to 75s/237°C
Cooling	Cooling rate	Max - 4.95°C/s

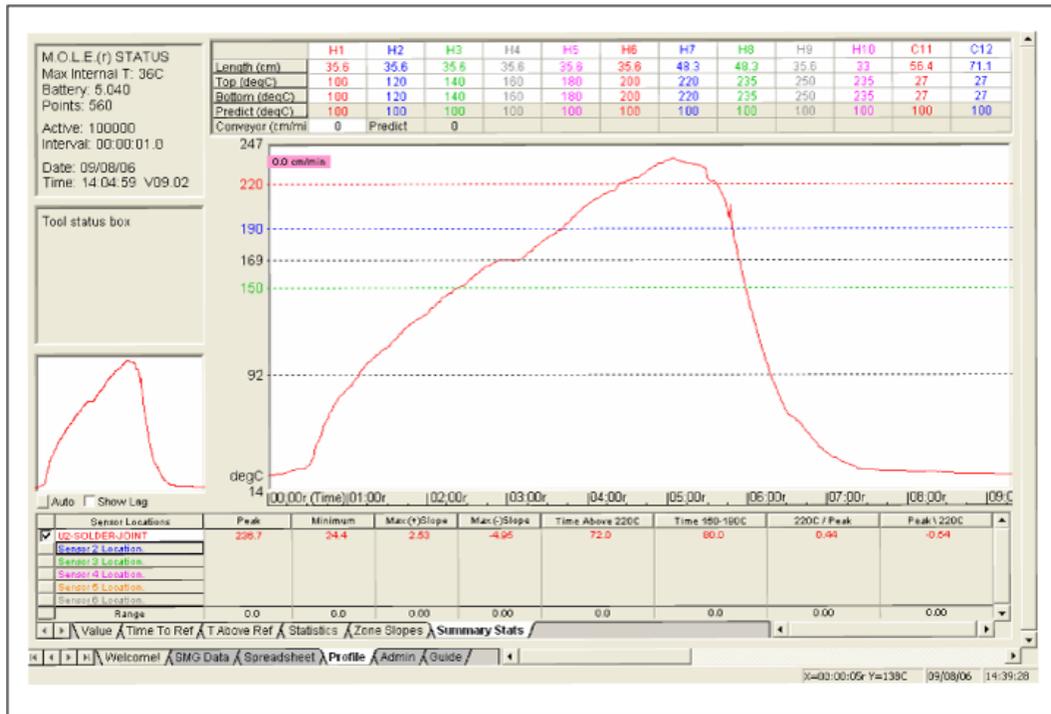


Figure 7. Lead-Free Solder Reflow Temperature Profile.

Solder Reflow Process

Maxim QFNs are compatible with all industry-standard solder reflow processes. There are no special requirements for reflowing QFNs. As with all surface-mount devices, it is important that profiles be checked on all new board designs. Additionally, if there are tall components mixed on the board, the profile must be checked at different locations on the board. Component temperatures may vary due to surrounding components, locations of parts on the PCB, and package densities.

The reflow profile guidelines are based on the temperature at the actual lead to PCB land pad solder joint location. The actual temperature of the solder joint is often different than the temperature settings in the reflow system. It is important that reflow-specific profiles be done using thermocouples at the actual solder joint locations and characterized using the reflow guidelines outlined in Table 3 and Figure 6 for eutectic solder, and Table 4 and Figure 7 for lead-free solder.

Solder Joint Inspection

Post-reflow inspection of QFNs on PCBs is typically accomplished by using transmission-type X-ray equipment. X-ray can be used for reflow process monitoring and as a failure analysis tool.

A 2-D X-ray system with Oblique View at Highest Magnification (OVHM) is highly recommended as it can detect solder bridges, opens, and voids. Solder joint visual inspection—as in any leaded package technology, the leads are either punch or saw singulated by design and, therefore, the edges of the leads will have bare copper exposed. Lack of solder wetting in this area is not considered a criteria for visual inspection/rejection.

Related Parts

[VT1697SB](#)

Smart Slave IC with Integrated Current and Temperature Sensors

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More Information

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