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APPLICATION NOTE 5554

ASIC Fixes for Noisy Analog “Oops”

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Abstract: Noise is a common problem in mixed-signal ASICs, degrading performance and jeopardizing the completion of products. This application note gives hints and tips for adding external circuits that make many of these ASICs operational for prototyping or shippable as final products. Ways to optimize the ASIC by correcting noise in analog circuits, making adjustments, calibrating gain and offset, and cleaning power sources are discussed. The payoff is quicker time to market and even the prevention of an extra ASIC manufacturing spin.

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Introduction

Good application-specific integrated circuits (ASICs) enjoy > 90% first silicon success. You might wonder why we want to talk about ways to “fix” this? After all, the ASIC almost works and there is no time to spin it and still meet the market window. Sound familiar? Unfortunately, Murphy’s Law[1] that says, “anything that can go wrong, will go wrong at the worst possible time,” applies here. No matter how we simulate, build field-programmable gate arrays (FPGAs), and prototype, there will be surprises. Small things will need improvement. And then, just when you think that you are getting close, Sales say they cannot sell the device without another “little” feature. Of course, the deadline for introduction cannot be extended. This drama is hardly unfamiliar and it can be the ASIC designer’s nightmare.

Digital circuits are relatively easy to fix because they tend to be black and white, on or off. But what happens when there is an analog issue on the ASIC? This can be daunting. Analog issues include things that *almost* work correctly. It is just a little noisy; it needs a little more gain; it needs a minor adjustment to calibrate it, bring it into range, or compensate for another component’s tolerance. If optimizing ASICs were so straightforward, many of us would drink less coffee and sleep better.

We see analog design mistakes on an ASIC all the time. We pick up a board and over in the corner is a piece of “oops logic,” a design feature that seemed right at the time but is clearly not working now. This article discusses ways to fix the “oops.” We present hints and tips to add external circuits to make many of these ASICs operational for prototyping or, in many cases, shippable products. We show how to correct noise in analog circuits, make adjustments, calibrate gain and offset, and clean power sources. The

payoff is everyone's goal: quicker time to market and even avoiding an extra ASIC manufacturing spin.

Optimizing the Analog to Reduce Noise

Noise is a common problem in a mixed-signal ASIC, primarily because digital-logic switching noise gets into sensitive analog circuits. **Figure 1** illustrates the best-case layout where each block has its own power and ground pin. Nonetheless, the digital circuits are switching current with fast edges that crosstalk and bounce the grounds and power pins.

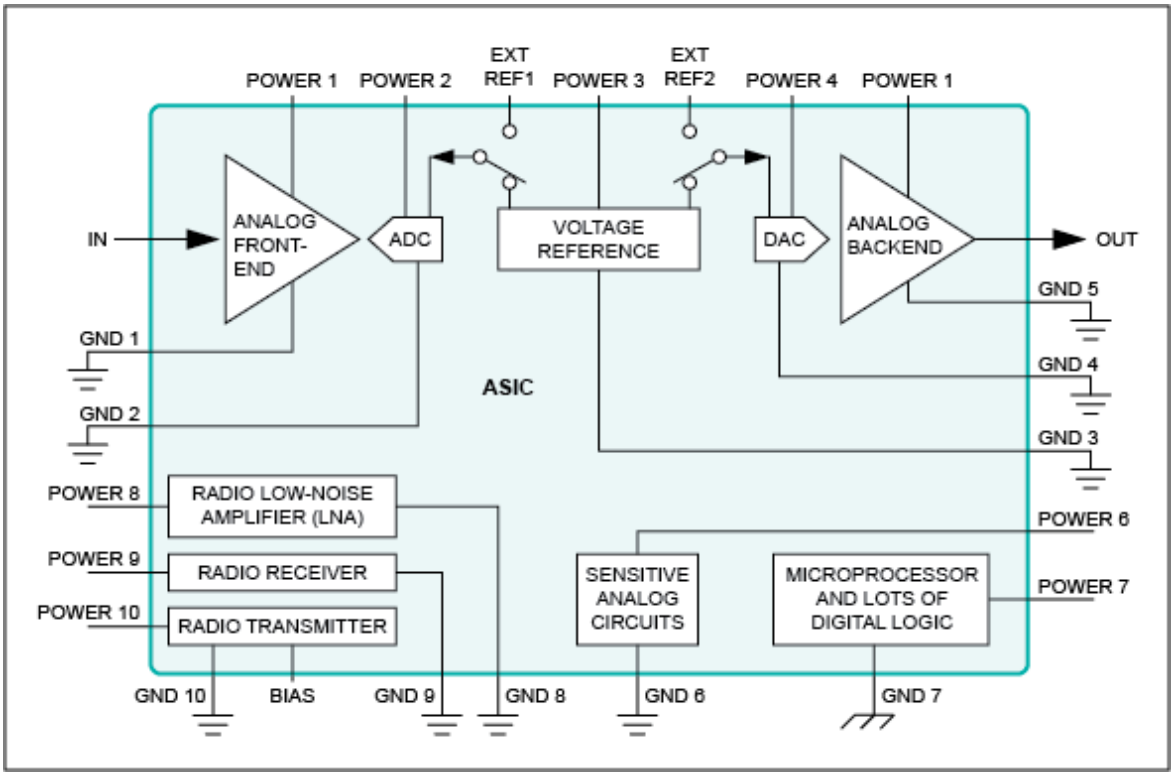

Figure 1. An ASIC block diagram shows the best-case layout where each block has its own power and ground.

This layout would be ideal if there were two dies (one analog and one digital) in the same package, built much like a hybrid. That configuration would allow two truly separate grounds because the circuits would not share a common silicon substrate. Alas, in the real world this ASIC is one die, but it is still important to have as many separate power and ground pins as possible. This gives us the most flexibility when we are troubleshooting and fixing issues.

Now let's look at ways to optimize some of the blocks in this circuit.

Switching Noise in the Microprocessor and Digital Logic

We start our examination of the Figure 1 circuit with the lower right corner, the microprocessor and the other digital logic, which are both sources of switching noise. The inexperienced designer might say, "but the clock is only 1MHz." This is true, but the edge of a perfect square wave has odd harmonics extending

to infinity. In practice, the most energy is in the first five to seven harmonics. Also in a clocked system, the clock makes the edges coincide except for propagation delays. Finally, a CMOS output draws current during the switching time. **Figure 2** shows the current used in two ways: one, to charge the capacitance of the next stage; and two, to partially power both transistors during the switching time. See this data in **Figure 3**. It is a small current, but it adds up when there are literally millions of transistors switching.

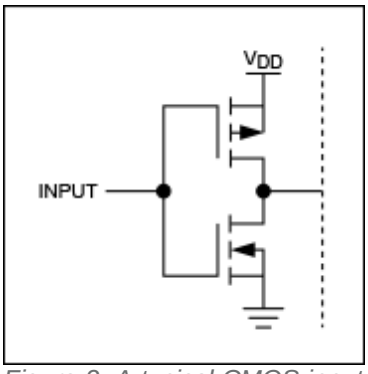

Figure 2. A typical CMOS input or output circuit uses current to charge the capacitance of the next stage and to partially power both transistors during the switching time.

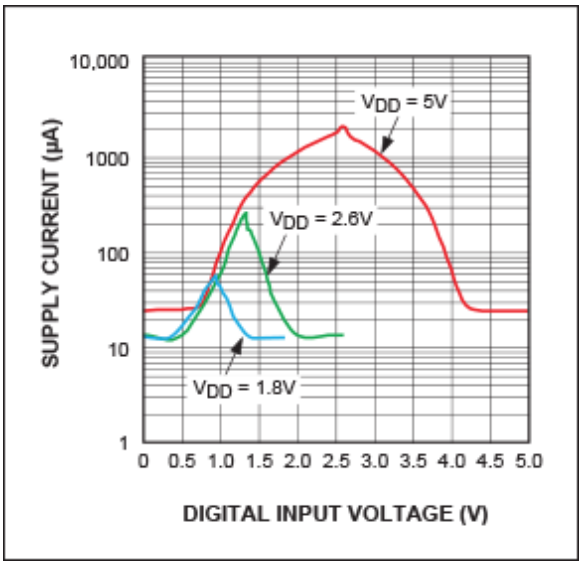

Figure 3. Voltage on a CMOS input pin versus power-supply current. Data are for the MAX5391 digital potentiometer.

Where does this get us? Some designers discriminate between power and ground domains with the terms “analog” and “digital”. We prefer the terms “clean” and “dirty,” respectively, as it helps with the thought process. Inside the ASIC, the ground can bounce, thereby introducing digital ground noise into the analog circuits. Consequently, these two ground domains need to connect at one system star point to keep their noise separated.[2] The power-supply decoupling capacitors need to be chosen with the capacitor’s self-resonance in mind.[3] The thresholds in digital logic remove noise, whereas analog circuits have no thresholds.[4]

Improving SNR to the ADC

Turn now to the analog front end (AFE) that feeds the ADC. This is comprised of a multiplexer, amplifiers, and filters. If the ADC signal is noisy, we look at the signal-to-noise ratio (SNR) of the input signal to determine what we can improve. There are several straightforward questions to ask. Is the full range of the ADC utilized? Can we add gain or offset with an amplifier and digital potentiometers to center and optimize the signal range? If the input signal is too noisy, can we clean up the source's power supply, even going to a low-noise reference to power it? Is there out-of-band (OOB) radio frequency interference (RFI) or electromagnetic interference (EMI)? Can we shield the circuit, add twisted wires, use a differential input amplifier, or add a lowpass filter to common mode out the noise?[5,6] The short answer to these questions is, yes. One or more of these actions can be taken before the ASIC input.

Another common issue is the source of the signal into the AFE. Let's say that a sensor is not available or needs to be replaced with another manufacturer's part. The situation becomes even more complex because that replacement part might have different output qualities; it might need impedance transformation, gain, or offset with an external amplifier to continue comparable operation. The AFE itself might be too noisy, so can we do a better job of decoupling the power possibly with a series inductor, resistor, or ferrite bead? The low-noise voltage reference can also work here as a power-supply replacement.

Moving to the right on Figure 1, we see a voltage reference that could feed both the ADC and DAC. There is also a switch option to feed the ADC with an external lower noise voltage reference. This simple change could improve the ADC's SNR. If you use a voltage reference that is adjustable or trimmable, you can adjust the full-scale amplitude of the ADC or DAC.

DAC Output Noise

Look now at the top right blocks of Figure 1 where we find the DAC followed with an analog backend made of amplifiers and filters. There is a quick way to evaluate the noise at the DAC and output conditioning: set the DAC to output three DC voltages at 10%, 50%, and 90% of its range. We choose 10%, 50%, and 90% to avoid clipping or compression and to stay in the linear signal area. The typical DAC reference input is connected to full scale and the zero scale to ground. Therefore, to understand the source of the noise, change the DAC DC value. (A spectrum analyzer is very helpful here.) The noise from the reference or power supplies is more pronounced near full scale; any ground noise prevails near zero scale. Switching between the internal and external voltage references reveals differences in that noise source. Also, be careful about interactions between the ADC and the DAC through the common voltage reference. Stepping the DAC with a clean DC on the ADC shows crosstalk through the reference path.

It might be necessary to add an external amplifier for filtering, and digital potentiometers for gain and offset adjustments and impedance conversion.

Powering the Radio Without Adding Noise

There are three radio blocks at the lower left of the ASIC. Radios are interesting because the transmitter can block or desensitize the receiver. The digital switching noise can do the same thing. This is a good place for a real-world example of what can go wrong, a very disruptive "oops" in a design.

Some years ago a company provided an upgraded cell phone that also allowed email access. The old

phone worked at my home with good SNR; the new phone required more signal to work. The design flaw became obvious: the extra digital circuits for the email function were so noisy that the phone receiver could not operate as intended. We had to install a cell phone repeater on the roof that repeated the signal in my home office to make the new phone work.

Now back to our main discussion. What does my story mean for our discussion of ASICs? Cell phones are duplex devices. That is, they simultaneously transmit and receive on different radio frequencies. A specialized filter called a duplexer allows duplex communication; it keeps the receiver from being confused by the higher power transmit frequency. However, it is possible for signals to leak around the duplexer and cause issues. By definition, the digital switching noise is not effectively removed by the duplexer. The radio receiver signal comes through an LNA. As in most systems, the first amplifier sets the SNR because the following amplifiers see a higher signal. Therefore, they do not contribute as much to the overall SNR.

The most sensitive power supply is the one feeding the LNA. Replacing this supply with a low-noise voltage reference can work wonders to improve receiver performance. The radio transmitter might also use an external MOS transistor to augment the power needed. This transmitter might need calibration to meet the maximum power output standards of the U.S. Federal Communications Commission (FCC) or the radio regulatory agencies in other countries. For example, if the component tolerances in the transmitter allowed the power to vary ±10%, the tolerances would need to be reset so the radio output could be between 80% and 100%. To be legal, the output power can never be above 100%; a lower power means that the range of the radio would be reduced. A simple calibration of power out in final test guarantees the maximum radio range and performance. Calibration allows compensation for those tolerances, and a simple digital potentiometer connected to the power amplifier bias pin ensures full power radio output.[7]

Look now to the last block of Figure 1, the “sensitive analog circuits.” We do not know what they are here! So, we guess: a MEMs accelerometer, a touch screen, an LCD display, a microphone input, an audio output, a light sensor, a face sensor, a dew or humidity sensor, a temperature sensor, and so it goes. We live in an analog world and we need to sense it, convert it to digital, process it, and then convert it to analog to control our analog world. At the very least, this example needs to add a digital potentiometer for calibration of LCD contrast, if the manufacturer has a voltage tolerance greater than expected or if it is necessary to use two manufacturers’ products to meet the delivery numbers. Calibrating the LCD bias with a digital potentiometer in the factory allows the existing ASIC to function without time-consuming rework.

Conclusion

How many other ASIC issues can we solve with simple fixes that do not require another complete layout pass? We will never know until we see them and try. Engineers know that Murphy and his “law” are always lurking in the shadows of the design lab. That is why every smart ASIC designer needs an experienced analog engineer to anticipate problems and to fix analog noise issues (the “oops”) that disrupt the product time to market.

References

1. For a discussion of the meaning and history of Murphy’s Law, you can start with the Wikipedia entry: http://en.wikipedia.org/wiki/Murphy%27s_law.

2. Application note 4605, “Avoid Design Misinterpretations that Put System Operation in Jeopardy.”
3. Tutorial 4992, “Reduce the Chances of Human Error: Part 1, Power and Ground.”
4. Application note 4345, “Well Grounded, Digital Is Analog.”
5. Tutorial 5065, “Radio Susceptibility - Cure with Antibiotic, Vaccine, or the Laws of Physics?”
6. Application note 4644, “Use a Twist and Other Popular Wires to Reduce EMI/RFI.”
7. For a list of design calculators, calibration parts, DACs, digital potentiometers, and references optimized for calibration applications, go to www.maximintegrated.com/cal.

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