



Maxim > Design Support > Technical Documents > Application Notes > Automotive > APP 5053
Maxim > Design Support > Technical Documents > Application Notes > High-Speed Interconnect > APP 5053
Maxim > Design Support > Technical Documents > Application Notes > Video Circuits > APP 5053

Keywords: high speed interconnect, GMSL, BER, eye diagram, pre-emphasis, equalization, serializer, deserializer, serdes, PRBS

APPLICATION NOTE 5053

Using 2.5Gbps SerDes with Built-In Bit-Error Rate Test Circuitry Makes Measuring Link Quality Easy

By: Craig Sakamoto
Wai Phyo
Jun 06, 2011

Abstract: Any application that involves sending information at high data rates over long distances requires tests to ensure good link quality. Thus, this applies to the MAX9259/MAX9260 gigabit multimedia serial link (GMSL) serializer/deserializer (SerDes), a chipset that sends audio/video data at payload rates of up to 2.5Gbps over a single twisted-pair cable up to 15m in length. This application note describes how to use the built-in bit-error rate (BER) tester and how to analyze eye diagrams to measure link quality with the MAX9259/MAX9260 evaluation (EV) kits. It also assists in proper jumper settings, measurement steps, and interpretation of results.

Introduction

Any application that involves sending information at high data rates over long distances requires tests to ensure good link quality, and the [MAX9259/MAX9260](#) gigabit multimedia serial link (GMSL) serializer/deserializer (SerDes) are no exception. This chipset sends audio/video data at payload rates of up to 2.5Gbps over a single twisted-pair cable up to 15m in length. One of the most straightforward tests of link quality is the bit-error rate (BER) test. Here, the transmitter sends a known data pattern across the serial link and the receiver checks the incoming data for any bit errors. A second test, the eye diagram, gives a graphical presentation of the link quality.

Both of these tests require a suitable pattern to be generated and transmitted over the serial link. While various test patterns are available, one of the common choices is to use is a long pseudorandom bit sequence (PRBS).

The MAX9259/MAX9260 chipset features an internal PRBS generator and BER checker to simplify testing, requiring only a parallel clock and a UART port to program the devices. The MAX9259 sends a $2^{30} - 1$ (in 32-bit mode) or a $2^{22} - 1$ (in 24-bit mode) PRBS data pattern across the serial link. The MAX9260 checks the received data and records the number of bit errors. This application note describes how to set up the MAX9259/MAX9260 evaluation (EV) kits for the internal PRBS test with bit-error analysis. It also compares test results for the default and optimized preemphasis/equalizer settings using a 15m cable.

Note that data sheets for the chipset and the EV kits, as well as the latest software, can be obtained through Maxim's website.

Required Equipment

- MAX9259 and MAX9260 EV kits
- Agilent® 33250A arbitrary waveform generator or similar device for clock generation
- USB cable
- Shielded twisted-pair cable with Rosenberger connectors

(Optional to analyze the eye diagram)

- Agilent DSO81004B or similar high-bandwidth digital oscilloscope
- Tektronix® P6248 differential probes or similar probes

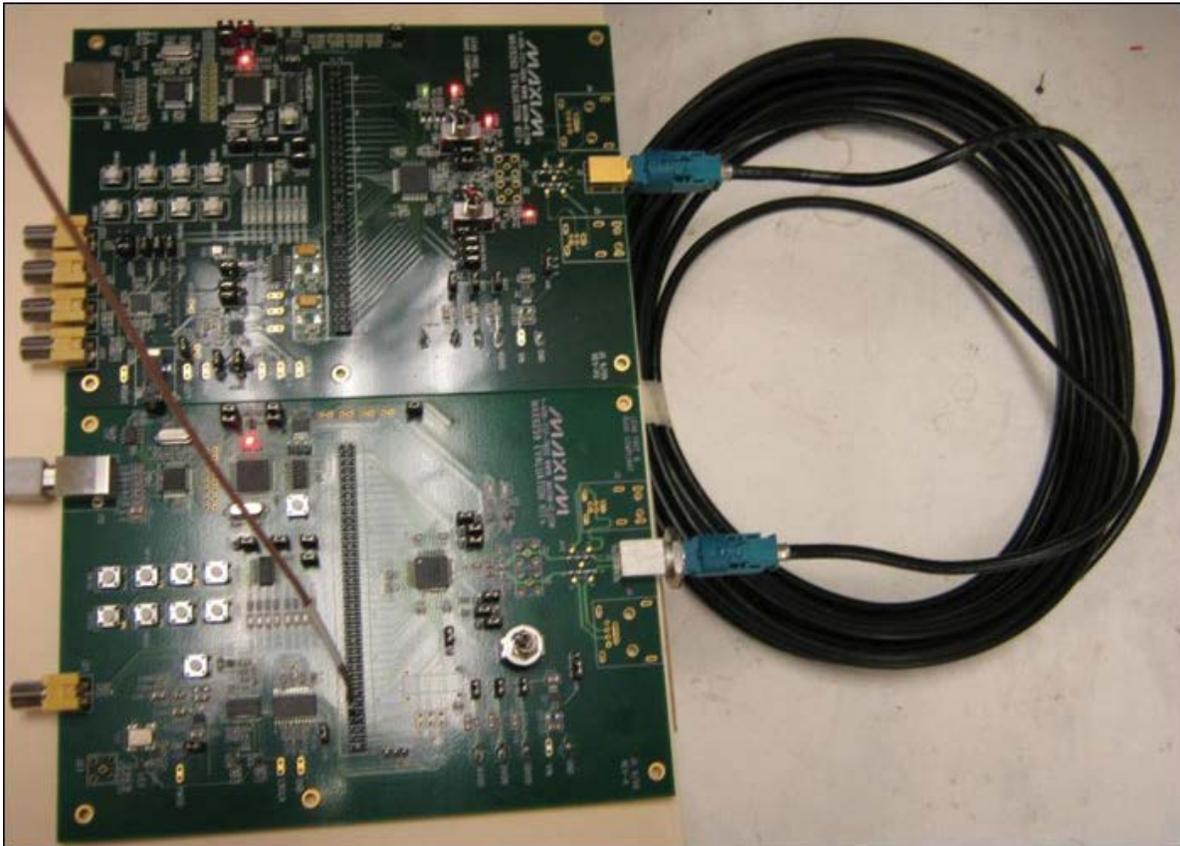


Figure 1. MAX9259/MAX9260 EV kits with 15m STP cable bench setup.

Built-In BER Test

Generally, getting a PRBS output from a serializer would require inputting data on all inputs to be serialized. For the MAX9259, this would require inputting data on the video, audio, and UART inputs. This can easily become very complicated due to the large differences in bit rates of the three interfaces. The MAX9259 includes an internal PRBS generator, which can be controlled through a single UART command. Set PRBSEN = 1 on the MAX9259 to turn on the PRBS generator. The serial data rate will be 30x PCLK (24-bit mode) or 40x PCLK (32-bit mode) based on the bus-width selection (BWS).

Table 1 below shows the results of BER test performed with different PCLK frequencies, a 15m STP cable with Rosenberger connector, 1.1dB or 10.5dB preemphasis, and a 9.4dB equalization level.

Table 1. 15m, 32-Bit BER vs. PCLK Frequency for 1.1dB or 10.5dB Preemphasis and 9.4dB Equalization Settings		
Input PCLK Frequency (MHz)	Errors at 1.1dB Preemphasis	Errors at 10.5dB Preemphasis
12.5	0	0
15	0	0
20	0	0
25	0	0
30	0	0
35	0	0

40	0	0
45	0	0
50	23	0
55	78	0
60	106	0
65	255	0

Activating the PRBS Mode

To begin the testing procedure, follow these guidelines to power up the EV kits and start the software.

1. Verify that the EV kit boards, software, and drivers are properly installed and operating by running through the *Quick Start* procedures as discussed in the [MAX9259EVKIT/MAX9260EVKIT](#) data sheets.
2. Verify that all the jumpers are set in the following positions, as shown in **Table 2**.

Jumper	Signal	Shunt Position	Description
JU1	CDS	2-3	CDS = low; ECU attached to MAX9259; connect USB to MAX9259 EV kit
SW1	MS	2-3 (toggle switch down)	MS = low; half-duplex base mode; required when writing to device registers or when using an external I ² C peripheral
JU2	BWS	1-2	BWS = high for 32-bit bus mode
JU3	ES	2-3	ES = low
JU4	DRS	2-3	DRS = low for parallel input data rates of 12.5MHz to 78MHz (32-bit bus mode)
JU5	SSEN	2-3	SSEN = low
JU6	PWDN	1-2	PWDN = high
JU7	AUTOS	2-3	AUTOS = low
JU8	H1 odd pins	2-3	2-3 H1 odd-numbered pins connect to GND
JU9	BUS power	1-2	J1 pin 1, J4 pin 1, and J5 pin 1 connect to VIN
JU10	BUS power	1-2	J1 pin 1, J4 pin 1, and J5 pin 1 connect to USB 5V
JU21	AVDD	1-2	AVDD power from 1.8V LDO U2, powered by VIN
JU22	DVDD	1-2	DVDD power from 1.8V LDO U2, powered by VIN
JU23	IOVDD	1-2	1-2 IOVDD power from 1.8V LDO U2, powered by VIN

3. Connect the STP cable from MAX9259 EV kit connector J1 to MAX9260 EV kit connector J1.
4. Connect the parallel data source or arbitrary waveform generator output to header H1-62, PCLK_IN. Set the parallel data source frequency between 12.5MHz to 78MHz and enable the output.
5. Connect the USB cable from the PC to the MAX9259 EV kit.

6. Verify that MAX9259 EV kit LED120 lights up, indicating that the microcontroller is powered and enabled.
7. Verify that MAX9260 EV kit LED120 lights up, indicating that the microcontroller is powered and enabled.
8. Verify that MAX9260 EV kit LED2 lights up, indicating that the link has been successfully established. If LED2 is off or LED1 is on, double-check that the PCLK_IN signal is clocking data.
9. Start the MAX9259/MAX9260 EV kit program by opening its icon in the **Start | Programs** menu. The EV kit software configuration window appears as shown in **Figure 2**.
10. Press the **Connect** button and the configuration window disappears.

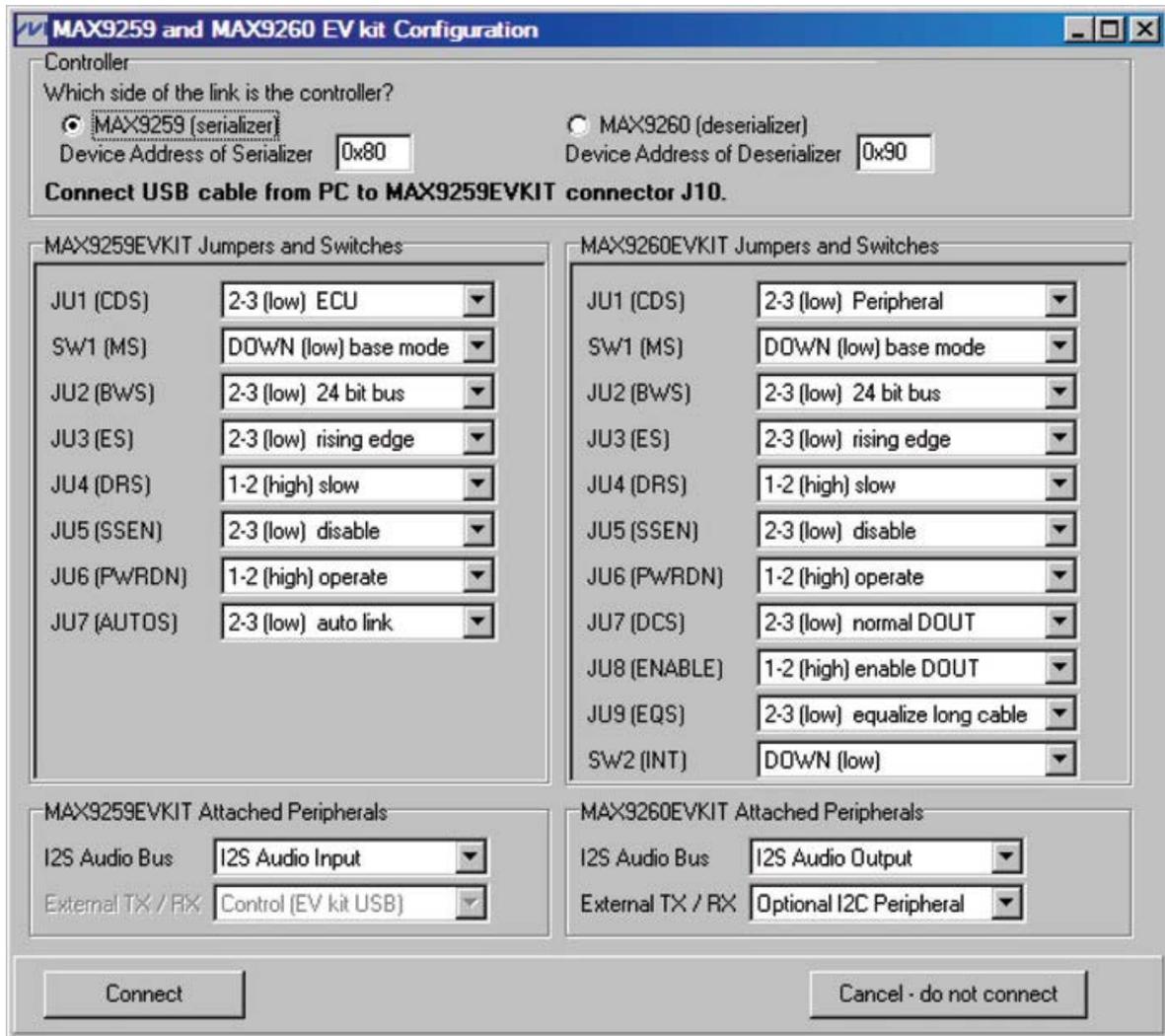


Figure 2. MAX9259/60 EV kits software configuration window.

11. The **Read All** button reads the entire MAX9259 and MAX9260 device registers. The **Write All** button writes all MAX9259 and MAX9260 device registers with the values shown **Figure 3** and **Figure 4**.

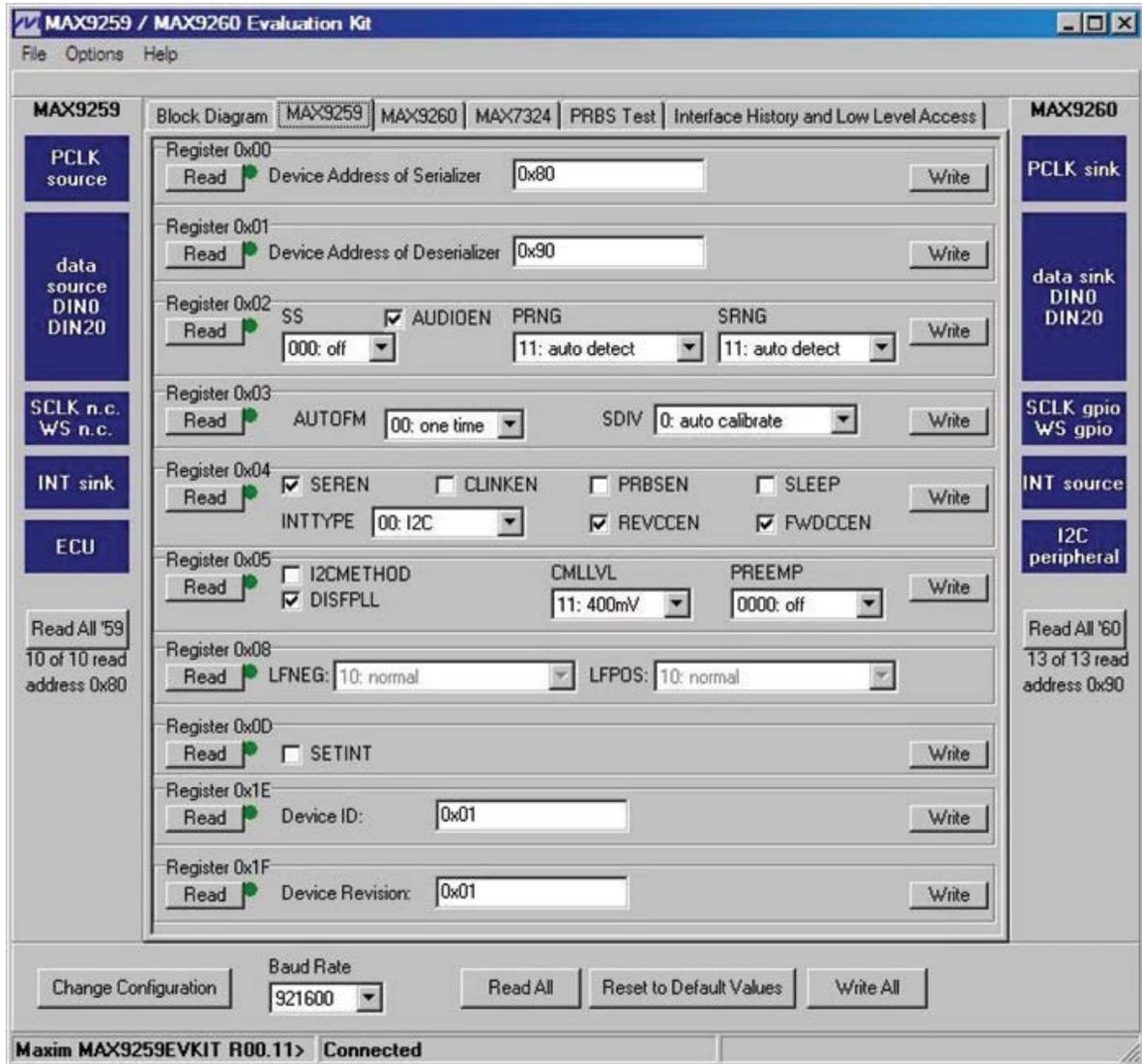


Figure 3. MAX9259/MAX9260 EV kits software main window (MAX9259 tab).

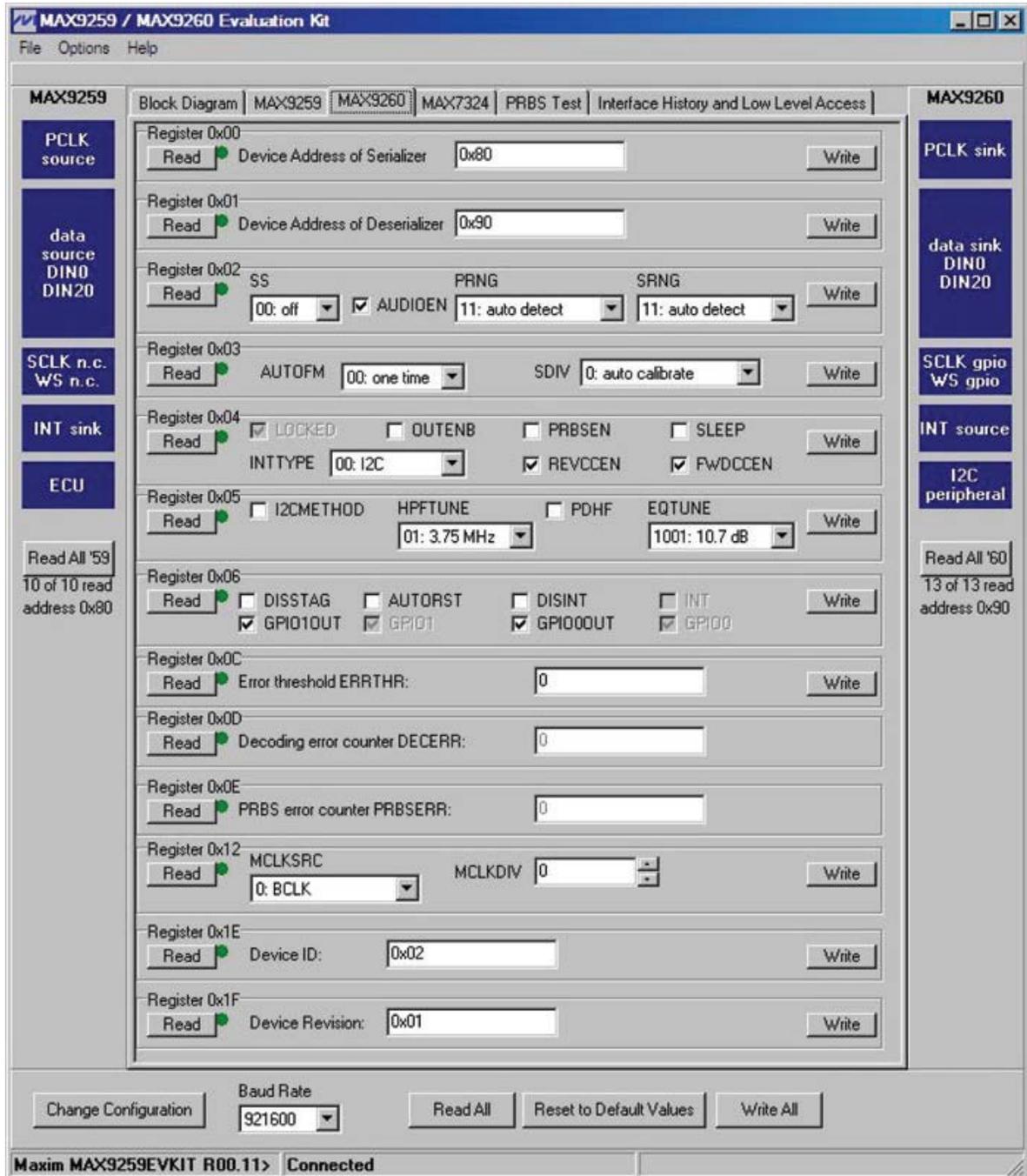


Figure 4. MAX9259/MAX9260 EV kits software main window (MAX9260 tab).

12. From the MAX9260 tab sheet (Figure 4), read the 8-bit error count register (0x0E) to clear the errors before the PRBS test.
13. Set PRBSEN = 1 (0x04 D5) first in the MAX9259 and then the MAX9260 to start the PRBS test.
14. Run the PRBS self test for the desired test time, and then set PRBSEN = 0 (0x04 D5), first in the MAX9260 tab and then the MAX9259 tab to exit the PRBS self test.
15. Read 8-bit error count register (0x0E) in the MAX9260 tab once. The total number of bit errors will report in the

window in "PRBS error counter PRBSERR." The error counter register is an 8-bit register, so the maximum number of errors that can be recorded is 255.

Eye Diagram

The BER test is a straightforward method to measure the link quality. Another approach to evaluate the system performance is analyzing the eye diagram opening. This provides a graphical presentation of the link quality, as well as insight into the nature of channel imperfections. **Figure 5** and **Figure 6** are eye diagrams of a serial link captured with a high-bandwidth digital oscilloscope (in infinite persistence mode) at the deserializer side of a 15m STP cable. The preemphasis settings of 1.1dB (Figure 5) and 10.5dB (Figure 6) were selected to provide the visible differences in the eye diagrams. The user can determine impedance mismatches, reflections, timing variation, and even frequency attenuation issues from the analysis of eye diagrams.

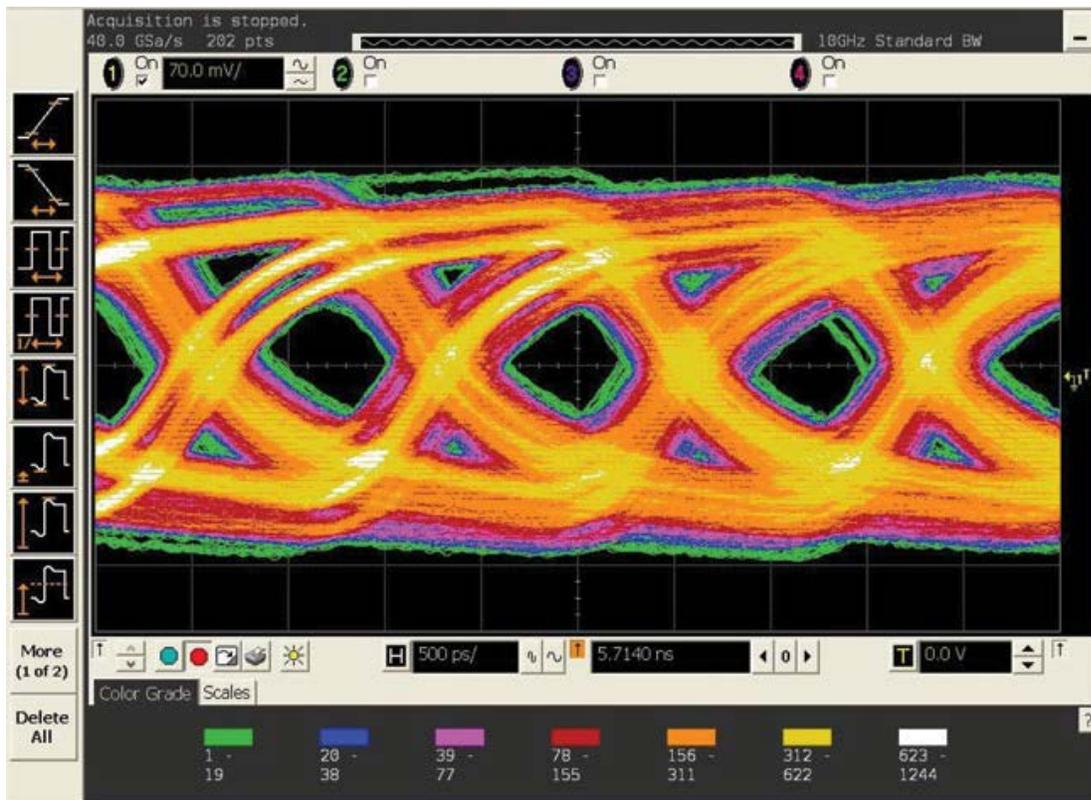


Figure 5. PRBS mode—eye diagram (15m cable with 1.1dB preemphasis setting).

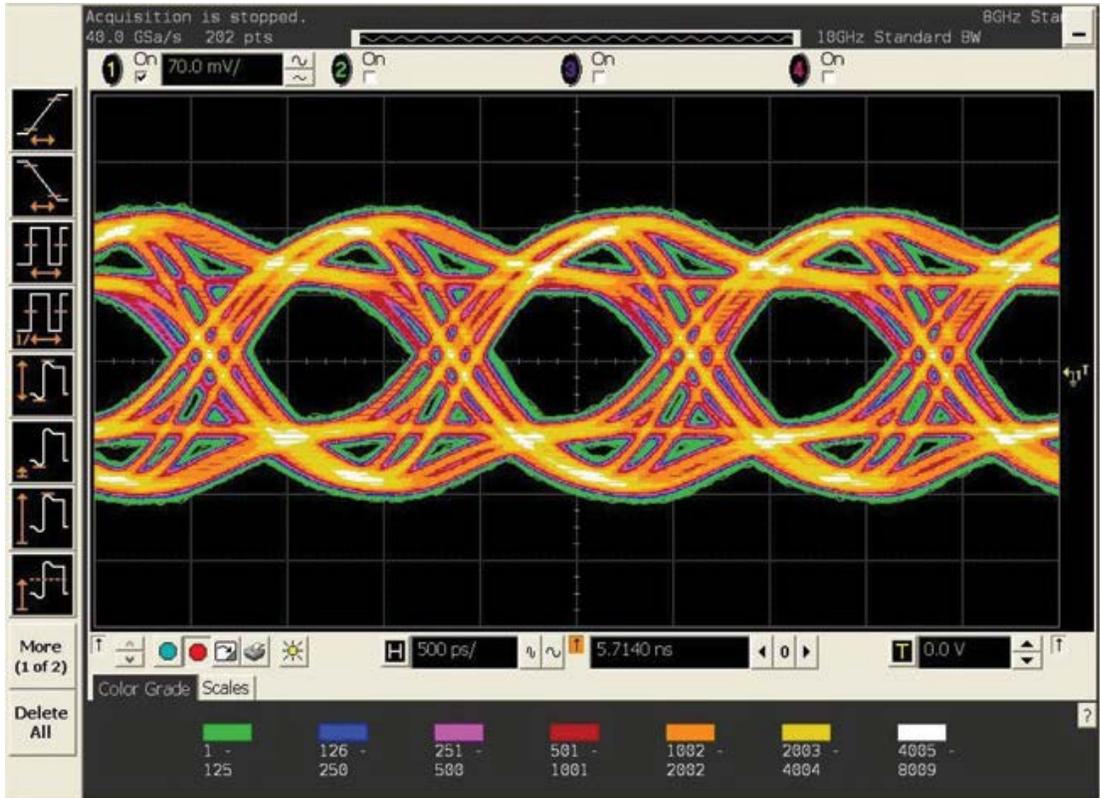


Figure 6. PRBS mode—eye diagram (15m cable with 10.5dB preemphasis setting).

Agilent is a registered trademark and registered service mark of Agilent Technologies, Inc.
 Tektronix is a registered trademark and registered service mark of Tektronix, Inc.

Related Parts		
MAX9259	Gigabit Multimedia Serial Link with Spread Spectrum and Full-Duplex Control Channel	Free Samples
MAX9259EVKIT	Evaluation Kit for the MAX9259	
MAX9260	Gigabit Multimedia Serial Link with Spread Spectrum and Full-Duplex Control Channel	Free Samples
MAX9260EVKIT	Evaluation Kit for the MAX9260	
MAX9263	HDCP Gigabit Multimedia Serial Link Serializer/Deserializer	Free Samples
MAX9264	HDCP Gigabit Multimedia Serial Link Serializer/Deserializer	Free Samples
MAX9265	HDCP Gigabit Multimedia Serial Link Serializer with LVDS System Interface	Free Samples
MAX9266	HDCP Gigabit Multimedia Serial Link Deserializer with LVDS System Interface	Free Samples
MAX9268	Gigabit Multimedia Serial Link Deserializer with LVDS System Interface	

More Information

For Technical Support: <http://www.maximintegrated.com/support>

For Samples: <http://www.maximintegrated.com/samples>

Other Questions and Comments: <http://www.maximintegrated.com/contact>

Application Note 5053: <http://www.maximintegrated.com/an5053>

APPLICATION NOTE 5053, AN5053, AN 5053, APP5053, Appnote5053, Appnote 5053

Copyright © by Maxim Integrated Products

Additional Legal Notices: <http://www.maximintegrated.com/legal>