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Keywords: clock, synchronization, clock synchronization, stratum, SEC, EEC, SSU, 1Hz, 1PPS, PPS, pulse per second, GPS, IEEE1588, 1588, DPLL, digital PLL, hitless switching, holdover, DS31400, DS31404, DS31406, DS31407, DS31408, DS31415

## APPLICATION NOTE 4976

# Using DS314xx Clock Synchronization ICs with 1Hz Input Clocks

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Mar 25, 2011

*Abstract: This application note describes how Maxim's DS314xx clock-synchronization ICs can be field upgraded to accept and lock to 1Hz input clock signals. It also describes the need for a 1Hz clock monitoring function and for system software support in a few situations. With these elements in place, a system built using DS314xx devices can have standards-compliant clock-synchronization behavior with any mix of 1Hz and higher speed input clocks.*

## Introduction

Maxim's DS314xx family of clock-synchronization ICs are powerful, flexible solutions for synchronized timing in telecommunication systems. These devices were originally designed to lock to input clock frequencies from 2kHz to 750MHz, a frequency range that meets the needs of most telecom systems. Occasionally, however, a telecom system must synchronize with a 1Hz or 1PPS (one pulse per second) input clock signal. Such a timing signal may come from a GPS receiver or an IEEE® 1588 slave function, for example.

Maxim has responded to this need by developing a 1Hz initialization script for the DS314xx family. This script provides an in-system software upgrade. After configuration with this script, a DPLL in a DS314xx device can directly lock to a 1Hz signal and can perform hitless switching among 1Hz clocks and higher frequency clocks. Maxim has verified in the lab that a system using a [DS31400](#) upgraded by this script can comply with the clock-synchronization requirements in ITU-T G.813 options 1 and 2, ITU-T G.8262 options 1 and 2, Telcordia GR-1244-CORE stratum 3, and the synchronization requirements of Telcordia GR-253-CORE. Compliance reports are available on request.

This application note covers the following topics:

- DS314xx device setup requirements for operation with 1Hz input clocks
- Redefinition of a few DS314xx register fields when locked to a 1Hz input clock
- The need for external monitoring of the 1Hz input clocks
- Support needed from system software for standards compliance

This application note assumes that the reader is knowledgeable about clock synchronization in telecom

systems and at least one of Maxim's DS314xx clock-synchronization ICs.

## Setup Requirements

### Oscillator

There are no special requirements for 1Hz inputs. Use the same TCXO or OCXO used in applications without 1Hz input clocks. Maxim's compliance testing was done with a TCXO.

### 1Hz Initialization Script Required

DPLL behavior must be modified to work with 1Hz input clocks. The write sequence listed in initialization file `DS314xx_1Hz.mfg` must be performed to configure a DPLL to work with 1Hz input clocks. This script can be downloaded from the [DS31400 web page](#) (Technical Documents tab, under the heading Software/Models). This script can be used with any DS314xx device.

### Input Clock Lock Frequency

Set `ICCR1.LKFREQ=0xE` for 1Hz inputs.

The 1Hz initialization script assigns the previously unused 0xE decode to be 1Hz.

### Disable Input Clock Monitors for 1Hz Inputs

The DS314xx input clock monitor logic was not designed for 1Hz input clocks. Therefore, the following must be disabled for each 1Hz input clock:

- Frequency monitoring hard limits (`ICCR2.HARDEN=0`)
- Gross frequency monitoring (`ICCR2.FREN=0`)
- Activity monitoring using the leaky bucket accumulator (`ICLBS=0`).

Input clocks with kHz and MHz frequencies can be monitored normally by the DS314xx devices.

### DPLL Settings

The following settings are *required* for a DPLL that is expected to meet ITU-T G.813 SEC, ITU-T G.8262 EEC, or Telcordia GR-1244 stratum 3 clock-synchronization requirements:

- `DPLLCR6.AUTOBW=0`
- `DPLLCR6.LIMINT=1` (reset default value)
- `DPLLCR1.UFSW=1`
- `DPLLCR4.LBW=00111` (set bandwidth to 0.06Hz or lower)
- `DPLLCR6.PBOEN=1` (reset default value)
- `DPLLCR5.FLEN=0`

In addition, the following settings are recommended:

- `HRDLIM[15:0]=421Eh`, which gives  $\pm 9.5$ ppm DPLL frequency limit
- `DPLLCR5.FLLOL=1` (reset default), causes DPLL loss-of-lock when `HRDLIM` is reached
- `DPLLCR2.HOMODE=10`, `MINIHO=10`, which specify use of the 5.8min holdover average

The `DS314xx_1Hz.mfg` initialization script configures DPLL1 in the DS314xx ICs for both required and recommended settings listed above.

# Redefinition of Register Fields When Locked to a 1Hz Input Clock

## PHASE Field

When the DPLL is locked to a 1Hz input clock, the PHASE field is redefined to have units of nanoseconds with a 1ns resolution. When the DPLL is locked to a kHz or MHz input clock, the PHASE register behaves as described in the data sheet.

## FINE LIM and COARSE LIM Fields

When the DPLL is locked to a 1Hz input clock, the FINE LIM field has no meaning and must be ignored. The COARSE LIM field specifies the DPLL's phase limit. In addition, COARSE LIM is redefined so that the DPLL's phase limit is  $2^{\text{COARSE LIM}} \times 32\text{ns}$ . When the value in the PHASE field exceeds this phase limit, the PALARM status bit is set in either PLL1SR or PLL2SR. The DPLL state machine then immediately transitions to the loss-of-lock state. When the DPLL is locked to a kHz or MHz input clock, the FINE LIM and COARSE LIM fields behave as described in the data sheet.

# External Monitoring Required for 1Hz Signals

## External Monitoring

The DS314xx input clock-monitoring logic cannot monitor 1Hz input clocks. In addition, a DS314xx DPLL cannot invalidate a 1Hz input clock for lack of activity (i.e., lack of clock edges) or frequency offset. If activity and/or frequency monitoring are required for 1Hz input clocks, this monitoring must be done outside the DS314xx device.

For 1Hz signals that come from systems or subsystems like GPS receivers or IEEE 1588 slaves, the source of the 1Hz signal may already do the required monitoring. In that case, system software can receive clock status information from the source, and can validate and invalidate the 1Hz clock using the appropriate VALCR bit.

If the source of the 1Hz signal does not do the required monitoring, then a monitoring circuit can be built in FPGA logic. A high-speed clock signal (e.g., 50MHz or 100MHz) from the DS314xx device can be routed to the FPGA. Logic in the FPGA can count the number of high-speed clock cycles in each cycle of the 1Hz clock. With a 100MHz clock signal, frequency can be measured in this way with 0.01ppm resolution. If measured frequency is found to be too high or too low, the FPGA's monitor logic can indicate that the frequency is out of spec. System software can then respond by invalidating the 1Hz clock using the appropriate VALCR bit in the DS314xx device.

When the VALCR bit is cleared for the 1Hz clock, the DPLL automatically locks to the next highest priority, valid, input clock or goes to the holdover state if there are no other clocks available. The other inputs can be any mix of 1Hz or higher speed clocks.

## What a DS314xx DPLL Can and Cannot Do When a 1Hz Input Clock Has Defects

When the DPLL is locked to a 1Hz input clock that stops toggling (such as from a cable disconnection), the DPLL cannot quickly recognize that the signal is not toggling. This is because the DPLL receives only one phase update per second when the signal is present. The DPLL does leave the Locked state within a few seconds and may then change states among Prelocked/Prelocked2, Locked and Loss-of-Lock without going to holdover.

System software should react when the DPLL leaves the Locked state (which can cause an interrupt request on the DS314xx INTREQ pin, if enabled) by assuming that the 1Hz input is bad and then clearing the VALCR bit. This allows the DPLL to switch to the next valid input or go to holdover if there

are no other input clocks available.

If the system software does not invalidate the bad 1Hz clock and the DPLL is still trying to lock to the 1Hz signal when it is restored, DPLL pull-in may be very slow. Specifically, the DPLL frequency may move all the way to the positive or negative limit set by the HRDLIM field before it eventually pulls in and locks to the 1Hz input clock. This pull-in process can take tens or hundreds of seconds. If system software detects that DPLL frequency is too far from nominal, it can intervene by clearing and then setting the input clock's VALCR bit. This allows the DPLL to use its phase build-out routine to pull-in and lock in just a few seconds.

## Extra Steps Required for Holdover Entry and Exit

When configured for 1Hz operation, a DS314xx DPLL cannot leave the holdover state until it receives a "new selected reference" signal from the DS314xx input clock block. To ensure that this signal is generated with 1Hz clocks, system software must do the following:

- An invalid 1Hz input clock must be marked invalid. This is done by clearing the appropriate VALCR bit or by setting the priority of the input clock to 0.
- A valid 1Hz input clock must be marked valid. This is done by setting the appropriate VALCR bit and setting the priority of the input clock to a nonzero value.

If the state of a DPLL is *forced* to holdover, the system software must do a few extra steps using the DPLLCR2.STATE field. If the validity of the input clocks does not change when the STATE field is changed back to automatic state transitions, then the "new selected reference" signal is not generated and the DPLL does not leave the holdover state. To avoid this situation, system software should do the following procedure after changing the DPLL STATE field back to automatic:

1. If DPLLCR1.REVERT=0, then set it to 1.
2. Clear and then set the VALCR bit for the highest priority, valid, input clock.
3. Set the REVERT bit back to its original value.

The above procedure causes the input clock block to generate the "new selected reference" signal, which allows the DPLL to leave the holdover state and lock to the highest priority valid input clock.

## Software Support Required for Multi-ppm Pull-In to Be Stratum 3 Compliant

With a bandwidth  $\leq 0.06\text{Hz}$  and only one phase update per second available, a DS314xx DPLL locked to a 1Hz input clock changes frequency very slowly. For example, it may take more than 10 minutes to make a 9.2ppm frequency change while in the Locked state. For stratum 3 compliance a system is required to lock to a new input clock within 100s. If the frequency of that input clock is up to 9.2ppm away from the DPLL's current frequency, then clearly the DPLL cannot meet the 100s requirement with its normal tracking mechanism.

Fortunately, system software can greatly speed up the process by using the following procedure:

1. Get the frequency of the new 1Hz input clock from a clock monitor outside the DS31400.  
(This could also be the new frequency of the current 1Hz clock signal if the signal had a frequency step change.)
2. Calculate the difference between the new frequency and the DPLL's current frequency read from the FREQ register field.
3. Write the DPLL's current frequency to the manual holdover frequency field, HOFREQ.
4. Set DPLLCR2.HOMODE and MINHO to 01 to configure the DPLL for manual holdover.
5. Force the DPLL into holdover by setting DPLLCR2.STATE=010.

6. Manually ramp the manual holdover frequency in the HOFREQ field to the new frequency. The rate of change should be < 2.9ppm/s for GR-1244 stratum 3 compliance.
7. Allow the DPLL to do automatic state transitions by setting DPLL2CR.STATE=000.
8. Clear and then set the appropriate VALCR bit to allow the DPLL to exit the holdover state.
9. Set DPLL2CR.HOMODE and MINHO back to 10.

The DPLL quickly pulls in and locks to the 1Hz input clock.

## Phase Difference Between Output and Input Is Not Zero

When a DS314xx DPLL starts to pull in to a 1Hz input clock, it sets the input clock's current phase as its phase target. That phase target typically is not 0°. When the DPLL is locked, a zero or near-zero value in the DPLL's PHASE register field indicates that the DPLL has locked to the chosen phase target. Output clock signals from that DPLL are aligned with the DPLL's phase target and, therefore, have a fixed, typically nonzero phase relationship with the 1Hz input clock.

There are applications where outputs must be in phase with the 1Hz input or where outputs must have a system-controlled output vs. input phase relationship. Maxim offers two products that meet those requirements, the [DS31408](#) and [DS31415](#), that include an additional block called a time engine. This time engine enables these devices to lock to 1Hz input clocks and create output clocks with precisely specified phase.

## Conclusion

Maxim's DS314xx clock-synchronization ICs can be field upgraded to lock to 1Hz (1PPS) input clock signals. When the 1Hz signals are monitored externally and system software provides the small amount of support described in this application note, then a system built using DS314xx devices can have standards-compliant clock synchronization behavior while operating with any mix of 1Hz and higher speed input clocks.

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### More Information

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