AN_65XX_054 NOVEMBER 2008

The Real-Time Clocks of the 71M65XX Metering ICs

This document describes how to use the real-time clock (RTC) circuits of the three families of Teridian meter SOCs, the 71M651X, 71M652X and 71M653X series.

In addition, recommendations are given for sequencing production processes of meters containing batteries.

Introduction

All Teridian meter SOCs support time-of-use metering. They have real-time clocks that are adjustable to better than 5 ppm, providing excellent time-keeping capabilities. This document describes the features and peculiarities of the Teridian electricity meter ICs with respect to their real-time-clocks.

Shared RTC Features

All existing Teridian meter ICs have the following RTC features:

1. A 24-hour clock with a number range from 00 to 23.
2. Minutes and seconds with a number range from 00 to 59.
3. Calendar year with a number range from 00 to 256 (representing the year 2000 to 2256).
4. Month with a number range from 1 to 12.
5. Day of month with a number range of 1 to 31.
6. Day of week (Sunday = 1). This datum is not set automatically and must be set under firmware control to be valid.
7. A reliable way to read and set the clock. The method varies by product line.
8. A reliable way to adjust the clock for crystal drift. The method varies by product line.
9. Normal leap years are detected and tracked automatically: On years divisible by 4, the month of February has 29 days.
10. Reset, watchdog reset and transitions from battery modes to mission mode and vice versa do not clear or change the clock value.

A list of RTC registers is provided in Table 1.

Table 1: RTC Register Comparison

I/O RAM Location	Register Name	651X	652X	653X	Function
0x2015[5:0]	*RTC_SEC*	X	X	X	Seconds
0x2016[5:0]	*RTC_MIN*	X	X	X	Minutes
0x2017[4:0]	*RTC_HR*	X	X	X	Hours (0 to 23)
0x2018[2:0]	*RTC_DAY*	X	X	X	Day of the week (1 = Sunday)
0x2019[4:0]	*RTC_DATE*	X	X	X	Day of the month
0x201A[3:0]	*RTC_MO*	X	X	X	Month
0x201B[7:0]	*RTC_YR*	X	X	X	Year
0x2010[7:0]	*RTC_SUB_SEC*			X	Sub-second counter
0x201C[1]	*RTC_DEC_SEC*	X	X		Decrement second count
0x201C[0]	*RTC_INC_SEC*	X	X		Increment second count
0x201F[7:0]	*WE*		X	X	Write enable

Shared Characteristics of the RTCs to Watch out for

Not all functions of crystal oscillators and real-time clocks are intuitive. Below is a list of effects that the meter designer should be aware of when working with the RTCs of the Teridian electricity metering ICs:

1. Crystals drift because of manufacturing tolerances, temperature and aging. Even at room temperature, most crystals combined with capacitors and the 71M65XX IC will not oscillate at the nominal frequency of 32,768 Hz. This difference is called initial accuracy. Applying a temperature different than room temperature will change the frequency drastically. Without an adjustment for crystal drift, the clock usually has unacceptable long-term accuracy. See Teridian Application notes AN_651X_009, AN_6521_035, and AN_653X_003.
2. The day of week must be set accurately by firmware in order to read accurately. Demo Code is available to set the day of week from the date.
3. The RTC does not maintain a fully perpetual calendar. This is not a practical matter in most meters, which have lifetimes of 50 years or less. However, the following firmware corrections are needed to maintain a true Gregorian calendar:
    a. The firmware must maintain a count of centuries.
    b. On years divisible by 100, the year needs to be reset to zero.
    c. Year 00 is always treated as a leap year. To implement the Gregorian calendar correction, on the second after 23:59:59 on February 28th, on years divisible by 400, the date needs to be advanced to March 1.
4. Residual charges in capacitors on the meter PCB can keep the RTC running even when the board is perceived to be “off”. On the bench, some RTCs have been observed to function with VBAT below 1.0 VDC.
5. Sleep mode is defined as the operating mode where the main 3.3 VDC power to the IC is missing while a voltage within specifications is applied to the VBAT pin of the IC.
6. RTC tests under emulator control may falsify the results by providing operating current to the RTC.
7. The XIN and XOUT pins of the 71M65XX ICs should not be probed directly. For measuring the frequency, the TMUX output should be used.

Summary of RTC Differences

The 71M651X series is designed to use software drift rate adjustment. Reading must occur after two consecutive reads of *RTC_SEC* are unchanged. Writes to clock registers must be separated by at least 300 microseconds. The oscillator runs slower in sleep mode.

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The 71M653X series provides both capacitive hardware to adjust the oscillator rate and digital rate adjustment of the RTC's second register, using the I/O RAM registers *RTCA_ADJ* and *PREG and QREG*. Software must read the temperature using the CE, and change the rate to compensate for temperature. Therefore temperature compensation stops in the battery modes. Reading must occur after two consecutive reads of the second register are unchanged. Writes to clock registers must write *SUBSEC* to zero before starting, and finish before the change of second. Writes must be preceded by a write to *WE* (write enable). A sub-second register *SUBSEC* is available. The oscillator does not slow in battery mode, but it can stop if no voltage is supplied to the VBAT pin, even though V3P3SYS is powered.

Detecting RTC Validity and/or Power Failure

It is often desirable to detect an invalid RTC value. Loss of main power in meters without battery or loss of battery power while mains power is not applied will usually corrupt the RTC registers. In that case, the meter will have to apply a default time and date or signal that it has lost the RTC information.

The values that the RTC registers assume after losing power depend on a variety of factors, such as the residual voltage present on the board, the temperature, the timing, and on the individual IC itself. A powered-down Demo Board with a 71M65XX IC tends to assume the time 00:00:00 and the date 01/01/2000, but this is not always the case and cannot be used for a power failure test. Despite the fact that the RTC lacks a reliable power-failure detection circuit, a test can be designed that delivers good results. This test works as follows:

a) Read the RTC. If the time is 00:00:00 and the date is 01/01/2000, a power failure has occurred.

b) If the time is not 00:00:00 and the date is not 01/01/2000, compare the date with the production date of the meter, which can be stored in the flash memory of the 71M65XX or externally in a non-volatile memory, e.g. a serial EEPROM. If the RTC date is earlier than the production date, it can be concluded that a power failure has occurred.

c) If the RTC date is later than the production date, but the day of week is wrong, it can be concluded that a power failure has occurred.

d) Additional checks can be included, such as checking the calendar year for obviously invalid entries, such as a calendar year that is beyond the intended deployment period of the meter.

Another method involves storing the current date and/or time in an external non-volatile memory, such as a serial EEPROM. If the date and/or time are stored every n hours and if the RTC date/time is differing from the store date more than n hours when the meter recovers from a reset, it can be concluded that a power failure has occurred, unless the power failure lasted more than n hours.

71M651X Series

Product Part Numbers

TSC71M6511, TSC71M6513, TSC71M6515

Events Affecting the Clock

Neither a reset nor a shift to battery power affects clock values.

Power must be removed from both V3P3D and VBAT for the clock to become corrupted.

The highest failing battery voltage is 2V. The typical minimum is much lower but not guaranteed.

When operating from a battery, the oscillator is 20 ppm slower than when operating from mains power. See Teridian Application Note AN_651X_032 (Crystal Frequency Variations) for more information. Firmware can compensate at reset. See the section “Adjustment” below.

In battery mode (sleep mode), the MPU is not operating, and therefore the recommended firmware clock compensation stops. Firmware can compensate for this effect at power-up. See the section “Adjustment” below.

Reading the Clock

The seconds should be read until it returns the same value twice, and then the rest of the clock data can be read without danger of a turn-over.

Setting the Clock

The firmware can copy new values to the clock. However, the clock registers run on a very slow internal clock signal in order to save power. This means that at least 300 microseconds of delay must occur between writes to the clock registers.

When the clock is set, the exact time is known to the firmware. Therefore, the accumulated crystal drift error measured by the firmware rate adjustment should be cleared to zero, and the adjustment interval restarted. The rate of error is not affected, just the amount of accumulated adjustment.

Adjustment during Operation

Crystal Drift

During operation, the firmware should accumulate fractions of a second of error for each second. When the error exceeds a half second, it can write to the *INC_SEC* or *DEC_SEC* registers to adjust the clock time plus or minus one second. For example, the demo code uses a 32-bit variable to count calculated nanoseconds of error on each one-second interrupt. When more than 500,000,000 nanoseconds of error accumulate, the clock is adjusted.

Crystal drift rate follows a parabola with regard to temperature. This drift is described in a crystal data sheet. Crystals are much slower when hotter or cooler than the center temperature. The 6510 series measures its temperature, and the MPU software can calculate a parabola to adjust the drift rate so that the error accumulation calculation, above keeps the clock accurate.

Crystals also develop a long-term drift from aging. This must be measured by comparing the crystal against an outside time constant. Once measured, the difference in rate can be added to the overall crystal drift rate. This is usually done either when the meter’s clock is set (the best practice), or by counting cycles of mains over a long period, such as a month.

For more information, see Teridian Application Note 651X_009 (Temperature Compensation).

Adjustment for Battery Mode

When the meter is in low-power mode, the MPU is inactive. Therefore, when the MPU starts, it must measure the time it was off, and apply the correction for the total time it was off. The basic plan is to save the clock time when power fails. At start-up, the number of seconds elapsed can be calculated. This number of seconds can be multiplied by the drift rate, including the extra drift added by the battery-mode oscillator slow-down on the 71M6510

series. This number of seconds can then be added to the clock's time, and the clock can be set. See Teridian Application Note 651X_032 (Crystal Frequency Variations) for details.

Firmware Initialization and Cold Start

The clock should be marked unset if the year is zero, or the day does not match the date, or the indicated date and time are earlier than a nonvolatile date and time recorded once per day.

If the clock is valid, the firmware should perform the adjustment for battery mode (see above).

Battery Mounting Sequence

As described in Application Note AN_651X_056 "Operation with Batteries", the board supply voltage should be active when the battery is inserted into the target PCB, and the battery should stay connected to the VBAT pin of the 71M651X IC.

71M652X Series

Product Part Numbers

71M6521FE, 71M6521DE, 71M6521BE, 71M6521F, 71M6521D, 71M6521B, 71M6523FE

Events Affecting the RTC

Neither a reset nor a shift to battery power affects the clock values.

Power must be removed from both V3P3SYS and VBAT for the clock to become corrupted.

The highest failing battery voltage is 2 VDC. The typical minimum is much lower, but not guaranteed.

In sleep and LCD mode, the MPU stops operating, and therefore the recommended firmware clock compensation stops. Firmware can compensate at reset. See "adjustment" below.

In brownout mode, the MPU can run, and could perform compensation, but this is not economical of the battery power, and not recommended. Firmware can compensate more economically at reset. See "adjustment" below.

The oscillator circuit does not generate a measurable difference in frequency between mission and battery modes.

Reading the Clock

The seconds should be read until it returns the same value twice, and then the rest of the clock data can be read without danger of a turn-over.

Setting the Clock

The firmware can copy new values to the clock.

Unlike in the 71M6510, a write operation to the "WE" (write enable) register must precede each write operation to a clock register.

Like in the 71M6510, the clock registers run on a very slow internal clock signal in order to save power. This means that at least 300 microseconds of delay must occur between write operations to the clock registers.

When the clock is set, the exact time is known to the firmware. Therefore, the accumulated crystal drift error measured by the firmware rate adjustment should be cleared to zero, and the adjustment interval restarted. The rate of error is not affected, just the amount of accumulated adjustment.

Adjustment during Operation

Crystal Drift

During operation, the firmware should accumulate fractions of a second of error for each second. When the error exceeds a half second, it can write to the *INC_SEC* or *DEC_SEC* registers to adjust the clock time plus or minus one second. For example, the 6521 Demo Code uses a 32-bit variable to count calculated nanoseconds of error on each one-second interrupt. When more than 500,000,000 nanoseconds of error accumulate, the clock is adjusted.

Crystal drift rate follows a parabolic function with regard to temperature. This drift is described in the data sheet provided by the crystal manufacturer. Crystals are much slower when hotter or cooler than the center temperature. The 71M6520 series ICs can measure the die temperature, which enables the MPU firmware to calculate a parabola to adjust the drift rate so that the error accumulation calculation above keeps the clock accurate.

Crystals also develop a long-term drift resulting from aging. This drift must be measured by comparing the crystal against an outside time constant. Once measured, the difference in rate can be added to the overall crystal drift rate. This is usually done either when the meter's clock is set (the best practice), or by counting cycles of mains over a long period, such as a month.

For more information, see Teridian Application Note 6521_035 (Temperature Compensation).

Adjustment for Battery Modes

When the meter is in low power mode, the MPU should not adjust the clock, in order to save battery power.

Therefore, when power resumes, it must measure the time it was off, and apply the correction for the total time it was off. The basic plan is to save the clock time when power fails. At start-up, the number of seconds elapsed can be calculated. This number of seconds can be multiplied by the drift rate. This number of seconds can then be added to the clock's time, and the clock can be set.

Firmware Initialization and Cold Start

The clock should be marked unset if the year is zero, or the day does not match the date, or the indicated date and time are earlier than a nonvolatile date and time recorded once per day.

If the clock is valid, and the meter is not in a battery mode, the firmware should perform the adjustment for battery mode (see above).

Other Firmware Precautions

Firmware programmed into the flash memory of the 71M652X ICs must ensure that the IC transitions to sleep mode when a battery is present and when main power is not available. This avoids premature loss of battery charge due to the current draw in brownout mode.

Note: The 71M652X ICs does not automatically enter sleep mode when main power is not available.

71M653X Series

Product Part Numbers

TSC71M6531D/F, TSC71M6532D/F, TSC71M6533/6533H, TSC71M6534/6534H

Events Affecting the RTC

Neither reset nor a shift to battery power affects clock values.

Operation of the oscillator, and therefore the clock, is not guaranteed if VBAT falls below 2 VDC.

Performing a battery test with power removed from VBAT will cause the oscillator to stop on most PCBs. The oscillator will usually run or restart from leakage currents, but the clock will lose time, and the meter may appear to have spurious resets.

The highest failing battery voltage is 2 VDC. The typical minimum is much lower, but not guaranteed.

In sleep mode, the MPU stops running, but the basic clock drift compensation is in hardware, and continues.

In brownout mode, temperature cannot be measured since the ADC and CE are disabled. Therefore the software-based temperature compensation stops in brownout, LCD and sleep modes.

The oscillator circuit does not generate a measurable difference in frequency between mission and battery modes.

Reading the Clock

The seconds should be read until it returns the same value twice, and then the rest of the clock data can be read without danger of a turnover.

Alternatively, the firmware can read the subsecond register, and if it is not in the last fraction of second, read the value.

Setting the Clock

The firmware can copy new values to the clock at any time before the end of the second.

An practical way to set the clock is to clear the subsecond register first, which removes any possibility of reaching the end of a second before the registers are written.

Unlike in the 71M6510, a write operation to the “WE” (write enable) register must precede each write operation to a clock register.

Since the crystal drift adjustment time is only four seconds, clearing it is not needed.

Adjustment during Operation

Crystal Drift

Crystal drift rate follows a parabola with regard to temperature. This drift is described in a crystal data sheet. Crystals are much slower when hotter or cooler than the center temperature. The 71M653X series ICs measure the die temperature, and the MPU software can calculate a parabola to adjust the drift rate so that the error accumulation calculation in the electronics keeps the clock accurate.

Crystals also develop a long-term drift from aging. This must be measured by comparing the crystal against an outside time constant. Once measured, the difference in rate can be added to the overall crystal drift rate. This is usually done either when the meter’s clock is set (the best practice), or by counting cycles of mains over a long period, such as a month.

For more information, see Teridian Application Note AN_653X_003 (RTC Compensation).

Adjustment for Battery Modes

When the meter is in low power mode, the MPU should not adjust the clock, in order to save battery power.

However, hardware adjustment continues in all modes. Therefore, when power resumes, there is no need to measure the time it was off, and apply the correction for the total time it was off.

Firmware Initialization and Cold Start

The clock should be marked unset if the year is zero, or the day does not match the date, or the indicated date and time are earlier than a nonvolatile date and time recorded once per day.

Other Firmware Precautions

Firmware programmed into the flash memory of the 71M653X ICs must ensure that the IC transitions to sleep mode when a battery is present and when main power is not available. This avoids premature loss of battery charge due to the current draw in brownout mode.

Note: The 71M653X ICs does not automatically enter sleep mode when main power is not available.

Revision History

Revision	Date	Description
Rev. 1.0	9/19/2008	First publication.
Rev. 1.1	11/18/2008	Added recommended battery mounting sequence for 71M651X ICs. Added pre-cautionary notes regarding firmware required for proper transition to sleep mode when main power is missing (71M652X and 71M653X).

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