Keywords: MAX13300, MAX13301, Class D, Class D audio, high power audio, automotive audio, automotive Class D, automotive Class D audio

APPLICATION NOTE 4943

Diagnosing Automotive Faults with Class D Audio Amplifiers

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Mar 31, 2011

Abstract: This application note explains how to run the diagnostics for the MAX13300/MAX13301/MAX13302 automotive Class-D amplifiers.

Introduction

The MAX13300 automotive Class D audio amplifiers incorporate many built-in diagnostics to help locate faults in the system. The amplifiers detect the following fault conditions on the speaker outputs when there is no audio present. Since audio may not be present during these tests, those tests are typically run once at startup or only when requested in factory diagnostic mode.

- Short to ground
- Short to battery
- Open load
- Resistance measurement
- Tweeter present
- Output offset

There is another set of diagnostics designed to run continuously while audio is present. These diagnostics give the system feedback on the state of the MAX13300/MAX13301/MAX13302.

- Clipping detection
- Thermal warning detection
- Charge pump undervoltage
- Supply undervoltage
- Supply overvoltage

Startup Procedure

To avoid unwanted click-and-pop at startup, use the following procedure (**Figure 1**):

1. Set the state of active-low MUTE_CL1 to select the LSB of the I²C address.

2. Pull the EN pin high.
3. Release active-low MUTE_CL1.
4. If more than two I²C address's are needed, first write to CTRL4.ADR[1:0] to set the new address and then write CTRL5.ADRDF = 0 to enable a new address.
5. Increase the short-circuit current threshold by setting CTRL1.CLTH = 0. This guarantees that there is no false trigger of the short-circuit diagnostic because of a current imbalance at startup.
6. Enable the device by setting CTRL2.STBY = 0.
7. Enable a precharge of inputs by setting CTRL1.PRE = 1.
8. Set CTRL2.MD01 = 10 and CTRL2.MD23 = 10. This will precharge the output capacitors to PVDD/2.
9. Set CTRL0, CTRL1.CLVL[1:0], CTRL1.MD[1:0], CTRL3.HCL, CTRL3.LDM, CTRL4, and CTRL5 to desired values based on application requirements.
10. Wait at least 10ms from step 7. Disable the precharge circuit by setting CTRL1.PRE = 0.
11. Wait 100ms × C_{DCB} (µF) for the input bias voltage to stabilize. This means that if you are using a 2.2µF DC-blocking capacitor on the inputs, then wait at least 220ms. Decreasing this time will increase the click-and-pop noise generated at startup.
12. Optional: set CTRL2.MD23[1:0] = CTRL2.MD01[1:0] = 01 and delay at least 50ms before proceeding. This sets the outputs to MUTE mode.
13. Set CTRL2.MD23[1:0] = CTRL2.MD01[1:0] = 11. This sets the outputs to PLAY mode.
14. Set the short-circuit diagnostic threshold back to normal by setting CTRL1.CLTH = 1.

ADRDF	ADR1	ADR0	Active-Low MUTE_CL1	I²C ADDR (WR)	I²C ADDR (RD)
0	0	0	—	0xD8	0xD9
0	0	0	—	0xDA	0xDB
0	1	1	—	0xDC	0xDD
0	1	1	—	0xDE	0xDF
1	—	—	0	0xD8	0xD9
1	—	—	1	0xDA	0xDB

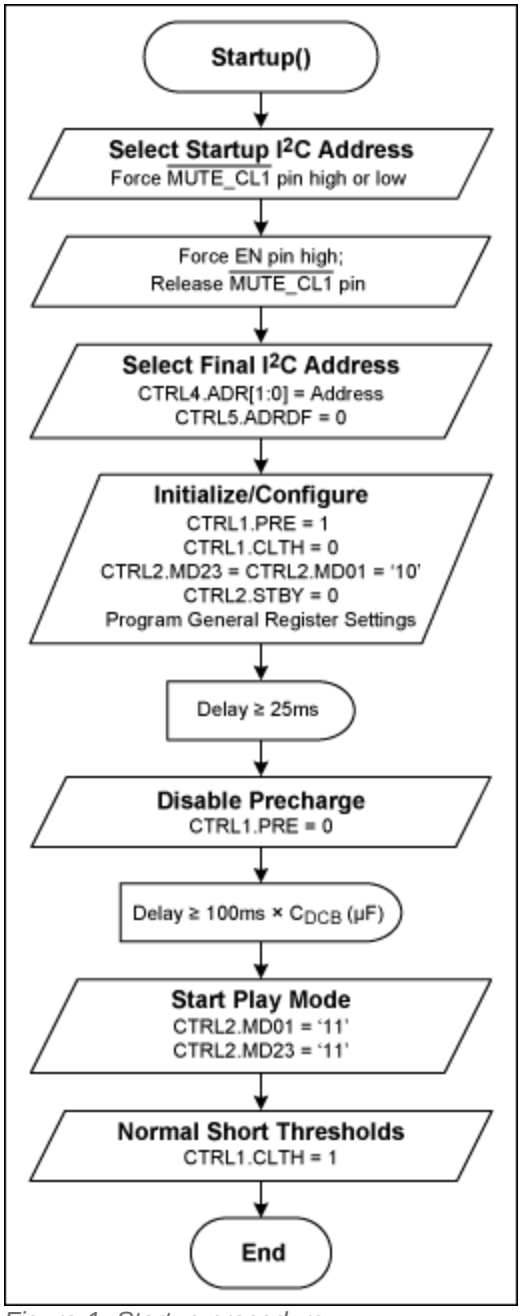


Figure 1. Startup procedure.

Three-State Procedure

To avoid unwanted click-and-pop at shutdown, use the following procedure (**Figure 2**):

1. If the audio source is already muted, then go to step 4.
2. Set the outputs to mute mode by setting CTRL2.MD23[1:0] = CTRL2.MD01[1:0] = 01.
3. Wait at least 50ms to ensure no click-and-pop from a 20Hz signal.
4. Three-state the outputs by setting CTRL2.MD23[1:0] = CTRL2.MD01[1:0] = 00.

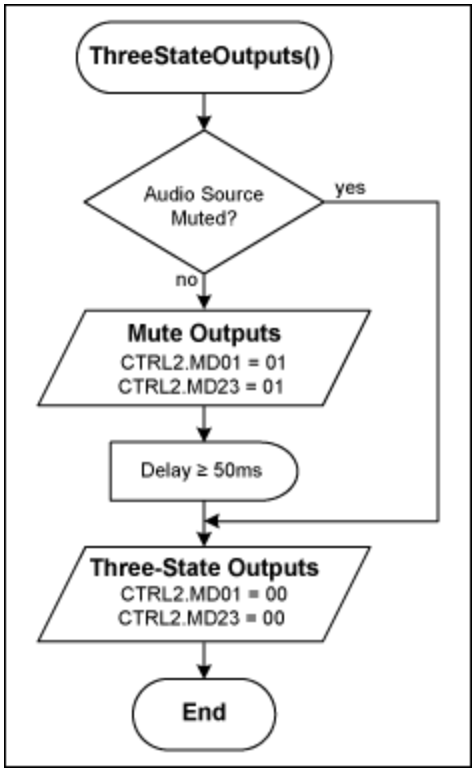


Figure 2. Three-State procedure.

Shutdown Procedure

To avoid unwanted click-and-pop at shutdown, use the following procedure (**Figure 3**):

1. Three-state the outputs by following the three-state procedure outlined above.
2. Enter standby mode by setting CTRL2.STBY = 1.
3. Pull the EN pin low.

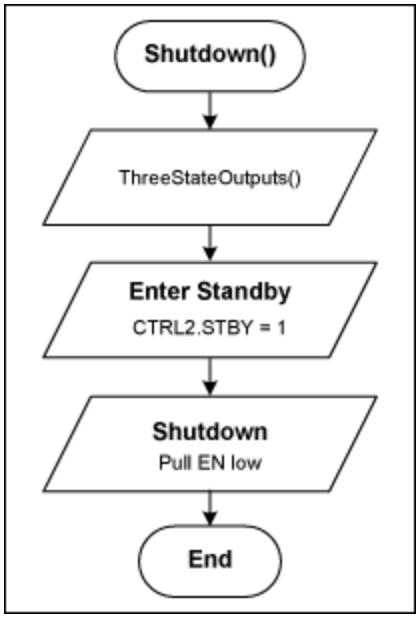


Figure 3. Shutdown procedure.

Load Diagnostics

Short-to-Battery Diagnostic Procedure

This diagnostic detects a short to battery or ground of less than 1kΩ on any output. The diagnostic for short to battery and ground is done at the same time and in the same diagnostic mode, however, the device must be out of standby mode to run the short-to-ground diagnostics. None of the results are latched, so the OSTAT2 register must be read while running this diagnostic to obtain a valid status.

If the load is present, a short on either of the differential outputs results in a short on the other output. Therefore, the OSTAT2 status register only indicates which channel's output is shorted and not which of its differential outputs is shorted. The I²C status register can indicate, for example, that output 1 is shorted to battery; it cannot differentiate between an OUT1+ and OUT1- short to battery.

To determine if a short to ground or battery exists on any of the outputs, three-state all outputs through I²C and enter standby (CTRL2.STBY = 1). Run the short-to-ground/battery diagnostic by setting the CTRL3.SDET (short-to-ground/battery diagnostic enable) bit to 1. The results of the diagnostic are reported in the OSTAT2.SBAT[3:0] (short-to-battery indicator) bits. Ignore all other fault indications as they are not valid.

Because no latch is set, a short to ground or battery does not prevent the device from powering up. Therefore, the microcontroller can enable the device into a short, although this configuration is discouraged. Should the device be enabled into a short, the real-time overcurrent will latch the shorted channel off. The MAX13300/MAX13301 offer real-time protection for short to battery, short to ground, and shorted load to prevent damage to the device.

Step-by-Step Procedure (**Figure 4**)

1. The device must be in standby mode to complete this diagnostic. If starting from MUTE or PLAY mode, follow the normal shutdown procedure to prevent click-and-pop.
2. Enable the short-to-battery diagnostic by setting CTRL3.SDET = 1.
3. Wait a minimum of 200µs.

4. Read the OSTAT2.SBAT[3:0] bits for results.
5. Disable the short-to-battery diagnostic by setting CTRL3.SDET = 0.

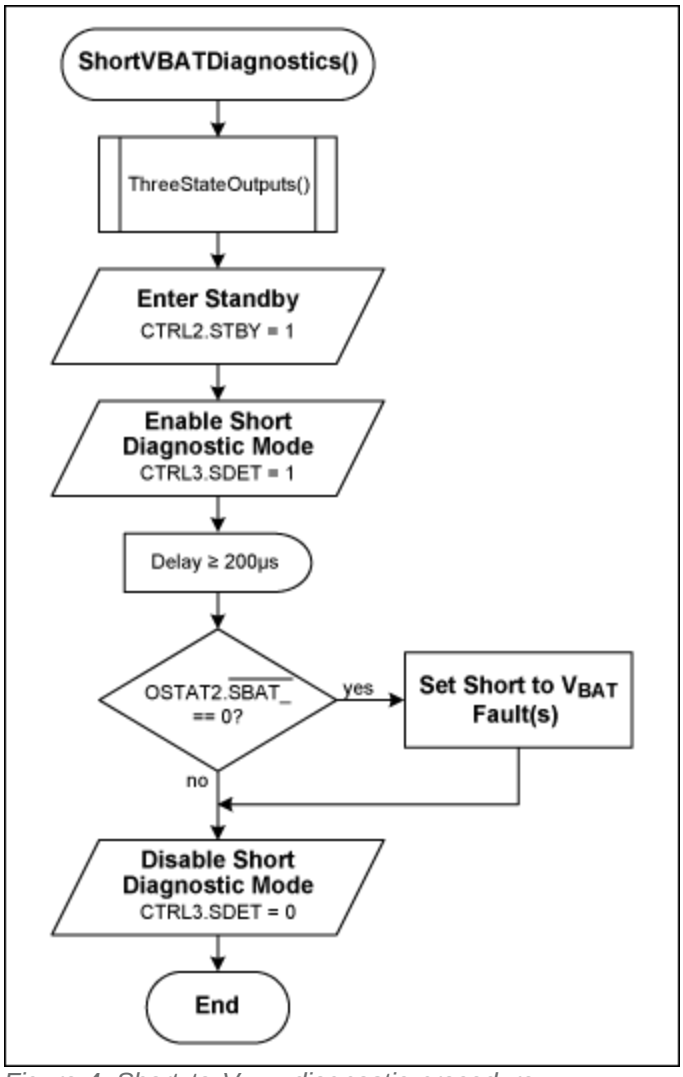


Figure 4. Short-to-V_{BAT} diagnostic procedure.

Short-to-Ground Diagnostic Procedure

This diagnostic detects a short to ground of less than 1kΩ on any output. The diagnostic for short to battery and ground is done at the same time and in the same diagnostic mode. None of the results are latched, so the OSTAT2 register must be read while running this diagnostic to obtain a valid status.

If the load is present, a short on either of the differential outputs results in a short on the other output. Therefore, the status register only indicates which channel's output is shorted and not which of its differential outputs is shorted. The I²C status register can indicate, for example, that output 1 is shorted to battery, but it cannot differentiate between an OUT1+ and OUT1- short to battery.

To determine if a short to ground or battery exists on any of the outputs, three-state all outputs through I²C. Run the short-to-ground/battery diagnostic by setting the CTRL3.SDET (short-to-ground/battery diagnostic enable) bit to 1. During the diagnostic, the device shunts a 3kΩ resistor across each

differential output to ground and sources 2mA of current to each output from PVDD. Under normal conditions, 6V is developed at each output. An output voltage > 6V is interpreted as a short to battery. An output voltage < 6V is interpreted as a short to ground. Results of the diagnostic are reported in the OSTAT2.SBAT[3:0] (short-to-battery indicator) and OSTAT2.SGND[3:0] (short to ground) bits.

Because no latch is set, a short to ground or battery does not prevent the device from powering up. Therefore, the microcontroller can enable the device into a short, although this configuration is discouraged. Should the device be enabled into a short, the real-time overcurrent will latch the shorted channel off. The MAX13300/MAX13301 offer real-time protection for short to battery, short to ground, and shorted load to prevent damage to the device.

Step-by-Step Procedure (**Figure 5**)

1. The outputs must be in three-state mode with the charge pump active (CTRL2.STBY = 0). If starting from MUTE or PLAY mode, follow the normal shutdown procedure to prevent click-and-pop.
2. Enable the short-to-ground diagnostic by setting CTRL3.SDET = 1.
3. Wait a minimum of 200µs.
4. Read the OSTAT2.SGND[3:0] bits for results.
5. Disable short-to-ground diagnostics by setting CTRL3.SDET = 0.

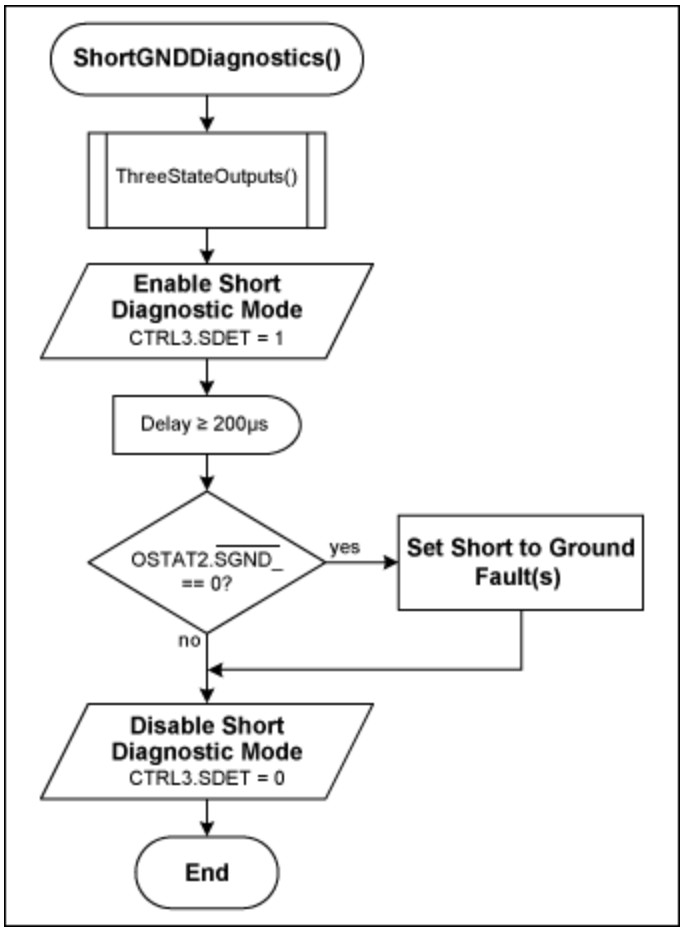


Figure 5. Short-to-ground diagnostic procedure.

Open Load Detection

This diagnostic detects an open between OUT_+ and OUT_- of > 70Ω or > 200Ω, depending on the value of the CTRL.LDM (load detect threshold) bit.

To detect open loads, three-state the outputs through I²C and discharge the output capacitors by setting the CTRL3.DIS (discharge) bit to 1. Run the open-load diagnostic test by setting CTRL3.RDET (open-load diagnostic enable) to 1. During the diagnostic, all low-side FETs on negative outputs (OUT_-) are turned on while all other FETs are turned off. The device sources a 2mA current from OUT_+ to OUT_-. If a load is not present, OUT_+ swings high and its relatively high VOUT_+ is interpreted as an open output. Results of the diagnostic are reported in the OSTAT0./LDOK[3:0] (load OK indicator) bits.

Step-by-Step Procedure (**Figure 6**)

1. The outputs must be in three-state mode with the charge pump active (CTRL2.STBY = 0). If starting from MUTE or PLAY mode, follow the normal shutdown procedure to prevent click-and-pop.
2. Set CTRL3.LDM based on application requirements.
3. Discharge the outputs to ground by setting CTRL3.DIS = 1 to prevent click-and-pop during diagnostics.
4. Wait at least 200µs.
5. Enable the open-load diagnostic by setting CTRL3.RDET = 1 and CTRL3.DIS = 0.
6. Wait at least 200µs.
7. Read OSTAT0.OC[3] bits. If any of the OSTAT0.OC[3:0] bits are low, the OSTAT1.LDOK[3:0] bits are not valid due to a short to V_{BAT} on the channel(s) indicated by the OSTAT0.OC[3:0] bits. Therefore, go to step 9.
8. Read OSTAT1.LDOK[3:0] for results.
9. Disable the open-load diagnostic by setting CTRL3.RDET = 0.

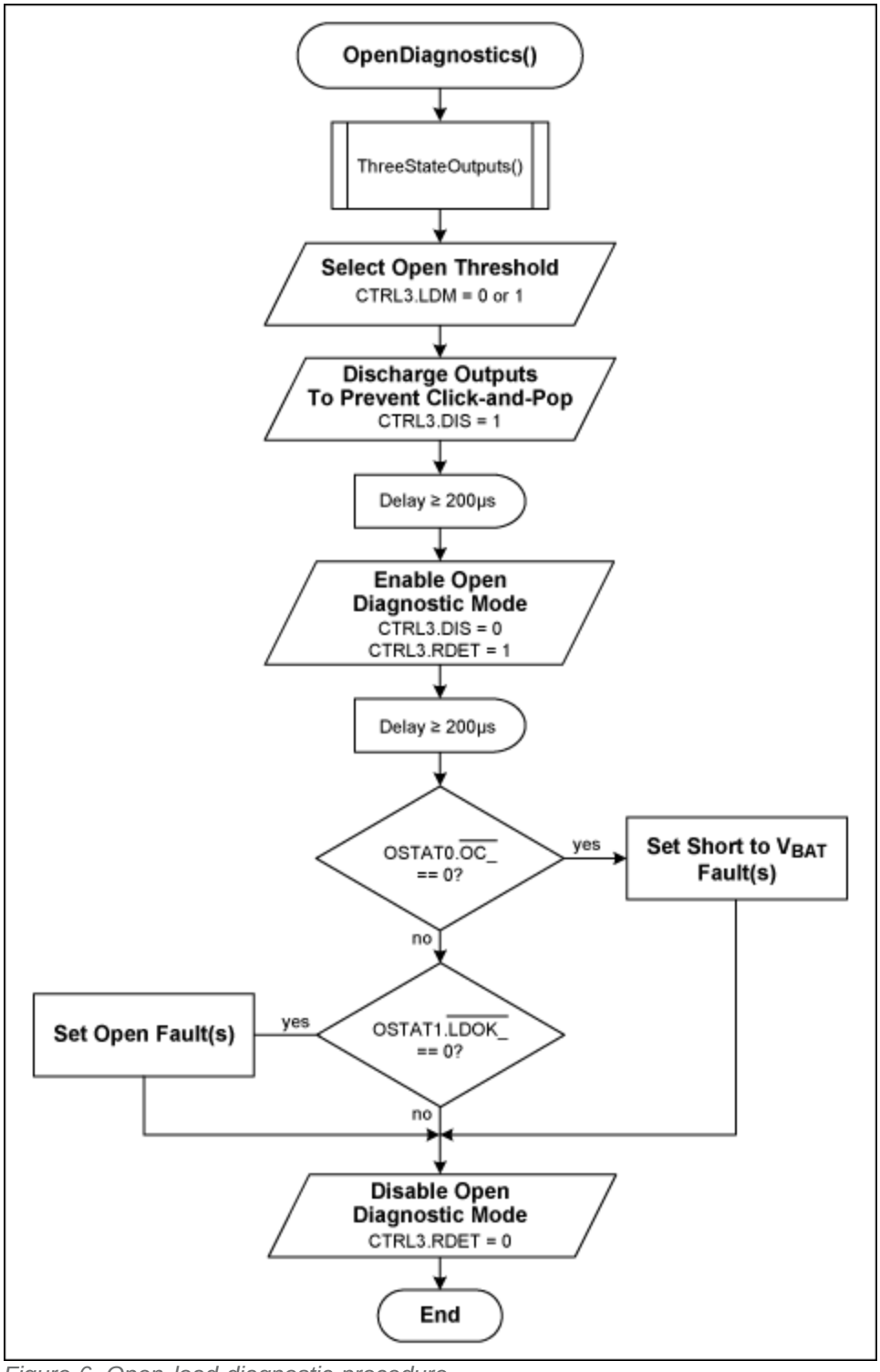


Figure 6. Open-load diagnostic procedure.

Shorted Load/Resistance Measurement Detection

This diagnostic can measure the resistance of the load so that shorted loads on any of the outputs can be detected. Since a resistance can be calculated from the diagnostic, this diagnostic can also be used

as an alternate method to detect open load or to determine if the speaker is present. To detect shorted loads, place the device in normal mode; set the CTRL3.TW (tweeter/shorted load diagnostic select) bit to 0; set MAP.LCTM to 1 to map the active-low LOAD_ fault bits to the active-low CL0 pin; and apply a ≤ 20Hz sinusoidal signal or single half-sine signal pulse to the inputs under test. The amplitude of the signal will depend on application requirements. The device compares the load current to the shorted load-current threshold. If the load current exceeds the threshold, the corresponding STAT3./LOAD_ (load indicator) bit is set to 1, indicating that there is a shorted load. The shorted load-current threshold depends on the programmed current limit. (See the Electrical Characteristics table in the data sheet.) A similar procedure can be used to detect an open load by using a larger amplitude sinusoidal signal.

Note that the active-low LOAD_ bits do not latch high upon detecting a short. During zero crossings, the load current does not exceed the threshold and the active-low LOAD bits are cleared to 0. There are two ways to obtain the results of the shorted-load diagnostic:

1. Continuously read the active-low LOAD_ bits to determine if any have been set high.
2. Monitor the open-drain active-low CL0 output. Because active-low CL0 is the NORed function of the active-low LOAD bits, active-low CL0 pulls low if a short exists on any of the outputs.

Mask the active-low LOAD_ bits to the active-low CL0 output by setting the MAP.LCTM (tweeter and shorted load mask) bit to 0 when the shorted-load diagnostic is not longer running. Clearing this bit prevents active-low CL0 from being asserted when the shorted load-current threshold is exceeded during play.

A load-resistance-measurement diagnostic is done on all outputs. A shorted load is traceable to the output on which it exists by examining the active-low LOAD_ bits or injecting the sinusoidal signal into one channel at a time.

Step-by-Step Procedure (**Figure 7**)

1. Enter PLAY mode by following the normal startup procedure.
2. Select the low-current threshold by setting CTRL3.HCL = 0. This current is approximately 1.3A. (See the Electrical Characteristics table in the data sheet.)
3. Map the diagnostic current threshold to the active-low CL0 pin by setting MAP.LCTM = 1.
4. Set the current threshold to a high setting for short detection by setting CTRL3.TW = 0. If you are running an open test, set CTRL3.TW = 1 to select the lower current threshold setting.
5. For each output [0 to 3]:
    - Generate a low-frequency sine wave (typically ≤ 20Hz) or single-pulse half-sine wave with the amplitude based on application requirements. If the amplitude of the sine wave is ramped until active-low CL0 is active, then the exact speaker impedance can be measured.
    - Monitor active-low CL0 or read OSTAT1.LOAD[3:0] to determine whether the current threshold is crossed. This status is not latched, so it will toggle on/off based on the signal amplitude. If monitoring active-low CL0, you must apply the input signal to one channel at a time. You can also read the active-low LOAD status bits through the I²C to determine which output caused the active-low CL0 pin to assert.
6. Remove the diagnostic current threshold mapping by setting MAP.LCTM = 0.

There are several ways to measure the exact resistance of the load:

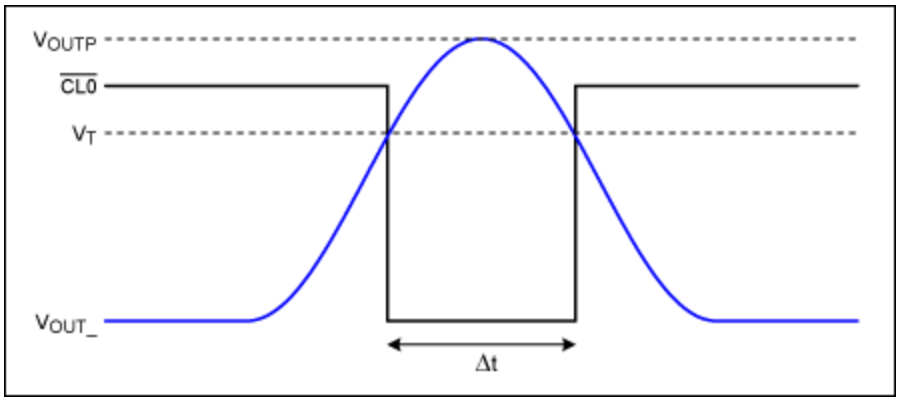
1. Ramp up the sine wave or half-sine pulses slowly until the active-low CL0 pin is asserted for the first time. The resistance is then calculated by:

$$R_L = \frac{V_{INP} \times GAIN}{I_T}$$

Where:

I_T = Threshold current set by CTRL3.HCL
V_{INP} = Peak input voltage signal
GAIN = Gain setting of the channel

2. Use a sine wave or a single half-sine pulse with an amplitude guaranteed to trip the selected threshold current with expected load resistance. When the test signal is applied, measure the amount of time that active-low CL0 is low. From this the load resistance can be calculated as follows:



$$R_L = \frac{V_{OUTP} \times \cos(pf\Delta t)}{I_T} \qquad 0 \le \Delta t \le \frac{1}{4f}$$

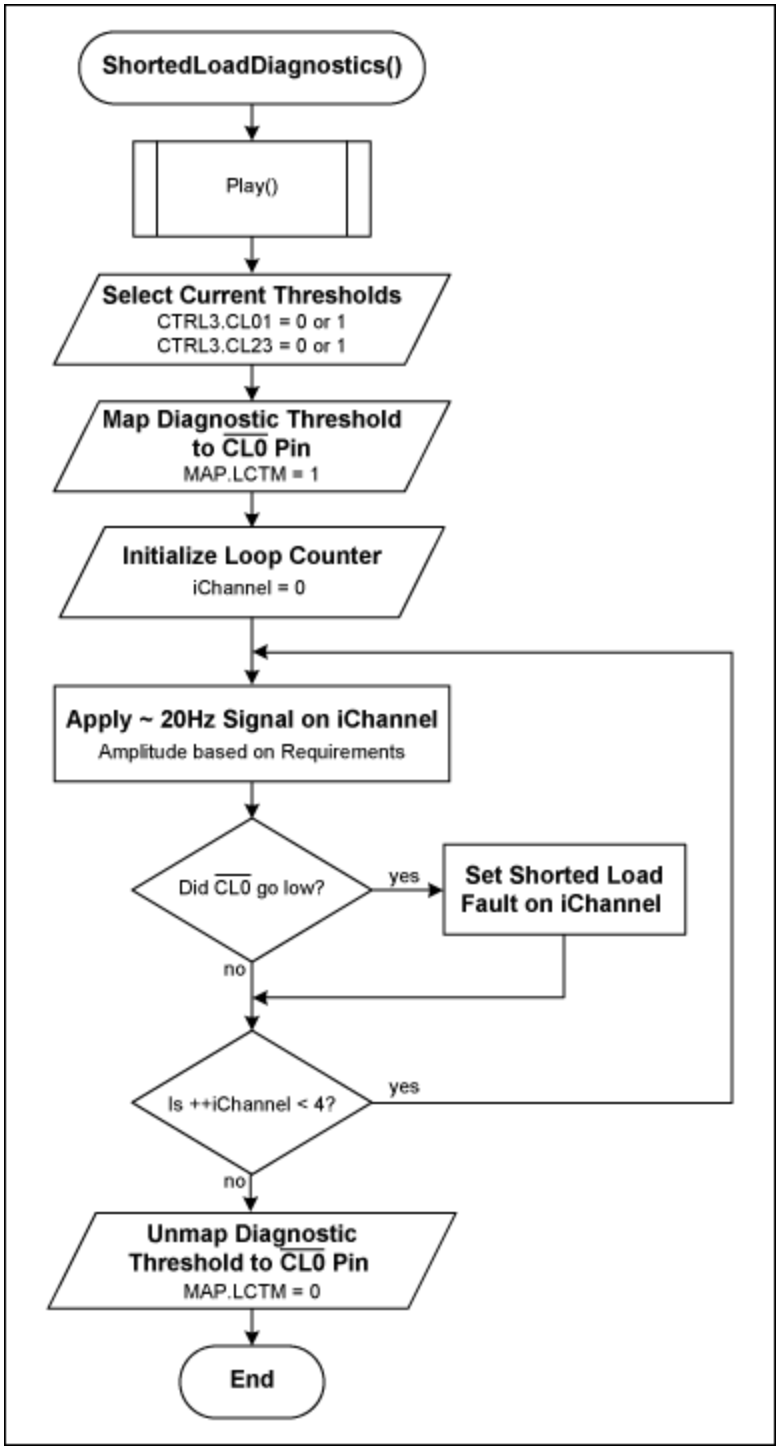


Figure 7. Shorted-load diagnostic procedure.

Tweeter Detection

This diagnostic detects whether a tweeter is properly connected when a passive crossover is used. To detect shorted loads, place the device in normal mode; set the CTRL3.TW (tweeter/shorted load diagnostic select) bit to 1; set MAP.LCTM to 1; and apply a 15kHz to 25Hz sinusoidal signal to all the

inputs. The device compares the load current to the tweeter-detect current threshold. If the load current exceeds the threshold, the corresponding STAT3./LOAD_ (load indicator) bit is set to 1, indicating that there is a tweeter. The amplitude of the input signal depends on the impedance versus frequency characteristics of the tweeter. Correct tweeter detection requires that the amplitude be large enough to trip the threshold when a tweeter is present.

Note that the active-low LOAD_ bits do not latch high upon detecting a tweeter. During zero crossings, the load current does not exceed the threshold and the active-low LOAD_ bits are cleared to 0. There are two ways to obtain the results of the tweeter detection diagnostic:

1. Continuously read the active-low LOAD_ bits to determine if any have been set high.
2. Monitor the open-drain active-low CL0 output. Because active-low CLP0 is the NORed function of the active-low LOAD_ bits, active-low CLP0 pulls low if a short exists on any of the outputs.

Mask the active-low LOAD_ bits to the active-low CL0 output by setting the MAP.LCTM (tweeter and shorted load mask) bit to 1 when the tweeter detection diagnostic is no longer running. Doing this prevents active-low CL0 from being asserted when the tweeter-detect current threshold is breached during play.

The tweeter detection diagnostic is done on all outputs. The presence of a tweeter is traceable to any output by examining the active-low LOAD_ bits. The presence of a tweeter on output 3 causes active-low LOAD3 to go high, etc.

Step-by-Step Procedure (**Figure 9**)

1. Set CTRL3.HCL = 0.
2. Map the diagnostic current threshold to the active-low CL0 pin by setting MAP.LCTM = 1.
3. Enter PLAY mode by following the normal startup procedure.
4. Set the diagnostic current threshold to low by setting CTRL3.TW = 1.
5. For each output [0 to 3]:
    - Generate a high-frequency sine wave (15kHz to 25kHz) with an amplitude based on application requirements. You must check one output at a time to determine which output has an open tweeter.
    - Monitor active-low CL0 or read OSTAT1.LOAD[3:0] to determine whether the current threshold is crossed. This status is not latched, so it will toggle on/off based on the signal amplitude.
6. Remove the diagnostic current-threshold mapping by setting MAP.LCTM = 0.
7. Select the normal diagnostic current threshold by setting CTRL3.TW = 0.

To select the optimum input-voltage amplitude, measure the speaker impedance with and without a tweeter present at the test frequency selected. Below is a typical 4Ω speaker impedance curve with and without the tweeter present.

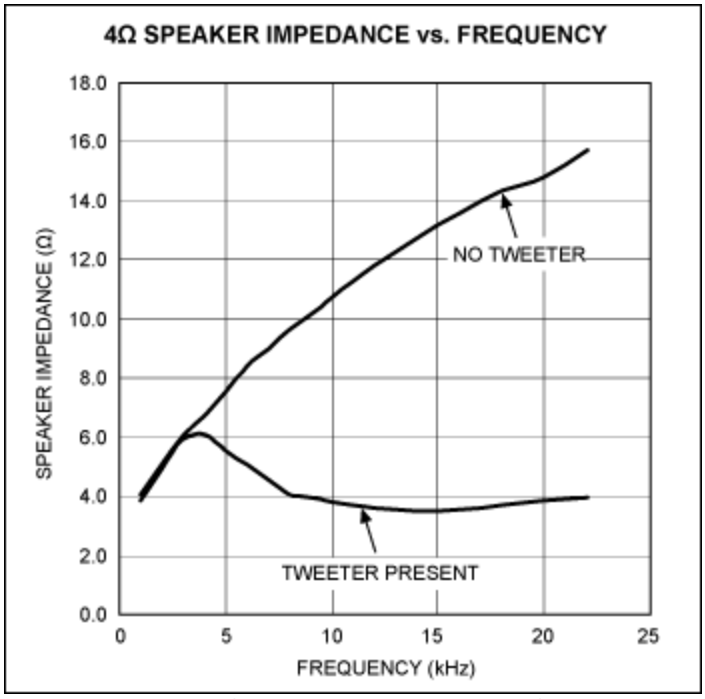


Figure 8. Typical 4Ω speaker impedance vs. frequency.

With a test frequency of 20kHz the optimum input voltage is where the active-low CL0 pin asserts with a speaker impedance of:

$$R_T = \frac{R_{TW} + R_{NO\text{-}TW}}{2}$$

Where:
R_{TW} = Speaker impedance with tweeter presen
$R_{NO\text{-}TW}$ = Speaker impedance with no tweeter

Using the equation above and the data in **Figure 8**:

$$R_T = \frac{14.8\Omega + 3.9\Omega}{2}$$
$$R_T = 9.4\Omega$$

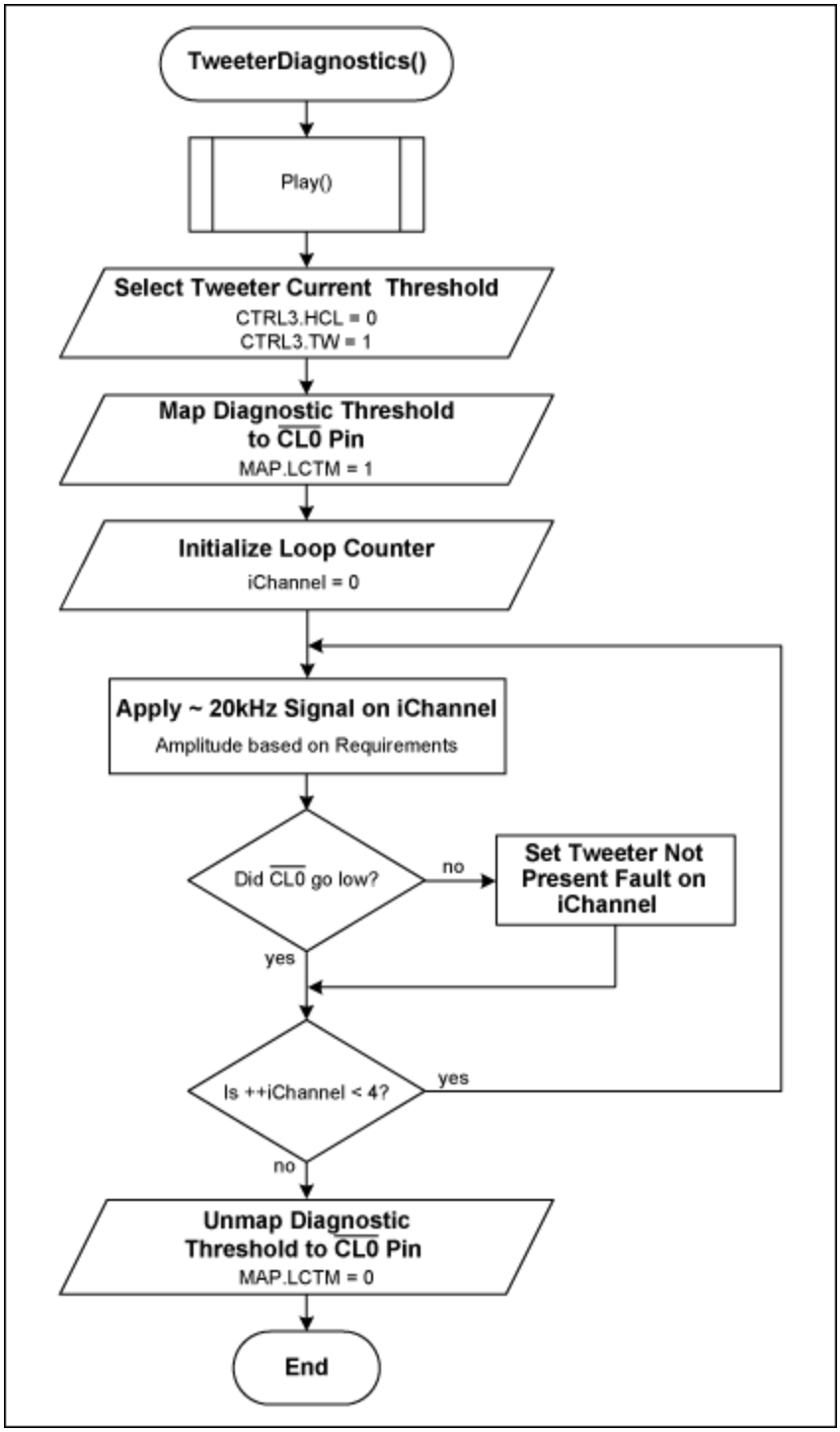


Figure 9. Tweeter diagnostic procedure.

Continuous Diagnostics

The MAX13300/MAX13301/MAX13302 constantly monitor critical performance and safety parameters such as output offset voltages, output clipping, thermal faults, and under- and overvoltage conditions. The results are reported and continuously updated in the status registers (STAT and OSTAT_).

Offset Diagnostic

Run the offset diagnostic to determine if there is an offset between the differential outputs. To run this diagnostic, place the device in play mode and apply no input signals. The results of this diagnostic are reported in the OSTAT3./VOS[3:0] (offset voltage indicator) bits. VOS_ indicates whether the offset voltage is less or greater than the offset voltage threshold. The threshold is typically 800mV for the MAX13300/MAX13302 and typically 1.0V for the MAX13301.

Clipping Diagnostic

Use the clipping diagnostic to detect clipping outputs. Program the CTRL1.CLVL[1:0] (clip level) bits for a threshold of either 2%, 4%, 6%, or 10% THD. Clip indication is provided by the OSTAT0./CLIP[3:0] (clip indicator) bits. These bits are set to 1 only during the times when an overdriven output is actually clipping. A clipping output indictor is available for each output; OSTAT0./CLIP[3] is for output 3, etc. The open-drain outputs, active-low CL0, and active-low MUTE_CL1, also provide clip indication.

Thermal Warning Diagnostic

If the junction temperature exceeds the programmed temperature limit, then a temperature fault is set immediately. The device does not act upon a temperature warning to the programmed limit. The temperature warning self-clears when the temperature drops below the threshold. If the junction temperature exceeds the maximum junction temperature of +150°C, the device disables all channels. The digital interface remains active and the contents of the registers are unchanged. When the die temperature drops below +140°C, normal operation is restored. The programmed temperature limit is set by software from +110°C to +140°C in 10°C increments.

Charge-Pump Undervoltage Diagnostic

The MAX13300/MAX13301 drive the high-side FETs with the aid of a charge pump. The charge pump charges the hold capacitor, C_{CHOLD}, to 5V at the end of each switching cycle. When the voltage on C_{CHOLD} falls below 3.45V, the device asserts the STAT./CPUV (charge pump undervoltage indicator) bit and three-states all outputs. The device deasserts the bit only after voltage on the hold capacitor rises above 3.75V.

Undervoltage Diagnostic

An undervoltage monitor detects low voltages on PVDD (< 6V). During an undervoltage condition, the device three-states all outputs, sets the STATE./UV (undervoltage indicator) bit to 0, and asserts the open-drain output active-low FLT_OT.

Overvoltage Diagnostic

The MAX13300/MAX13301/MAX13302 detect overvoltage and load-dump conditions on PVDD and protect the DMOS devices from damage. During an overvoltage condition, the device sets the STAT./OV (overvoltage indicator) bit to 0, asserts the open-drain output active-low FLT/OT, and is latched into standby mode. All differential outputs are regulated to ½ VPVDD to minimize the drain-source voltage of the low- and high-side FETs and to prevent breakdown. Once the overvoltage condition is removed, bring the device out of standby mode by clearing the CTRL.STBY (standby) bit. The MAX13300/MAX13301 can withstand 50V load-dump voltage spikes. Battery charger voltages from 26V to 35V can be withstood for up to 1 hour. Figure 7 illustrates the behavior of the device during a load dump.

Conclusion

The diagnostics capabilities built into the MAX13300/MAX13301/MAX13302 devices allow the devices to meet OEM diagnostic requirements. Flexibility built into specific tests such as load and tweeter diagnostics allow OEM-specific thresholds to be used.

Related Parts		
MAX13300	4-Channel, Automotive Class D Audio Amplifier	Free Samples
MAX13301	4-Channel, Automotive Class D Audio Amplifier	Free Samples
MAX13302	4-Channel, Automotive Class D Audio Amplifier	Free Samples

More Information
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For Samples: http://www.maximintegrated.com/samples
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Application Note 4943: http://www.maximintegrated.com/an4943
APPLICATION NOTE 4943, AN4943, AN 4943, APP4943, Appnote4943, Appnote 4943