A Maxim Integrated Products Brand

78M6613 Printed Circuit Board Layout Guidelines

APPLICATION NOTE

AN_6613_050 **October 2010**

Introduction

The highly integrated 78M6613 SOC minimizes the external component count and reduces the complexity of the printed circuit board layout design. However, some design issues require consideration for optimum measurement accuracy and reliability. This application note discusses these topics:

- Printed Circuit Board Stackup
- Crystal Oscillator Components
- LINE Voltage Resistor Network
- Shunt Current Sensor
- Dual Outlet 2-Shunt Current Sensor Topology
- V3P3 Decoupling Capacitors
- In-Circuit Emulator Connector
- System Communication Interface

This application note covers the layout for Teridian chips. It specifically does not discuss creepage and clearance. Refer to the discussion of creepage and clearance in UL 60950-1.

Printed Circuit Board Stackup

The 78M6613 can achieve excellent measurement accuracy using a 2-layer printed circuit board stackup. If the component density becomes too high resulting in insufficient plane flooding surface area, a 4-layer stackup must be employed. The plane flooding surface area is insufficient when the critical components presented in this application note are not properly shielded and isolated from external noise or each other. Additionally, there must be multiple redundant connection paths across the board's surface area to present low impedance paths for the various power and ground connections.

For 2-layer printed circuit boards, begin by assigning the layer where the 78M6613 resides as the V3P3 layer. Assign the opposite layer as the Ground layer. The following discussion regarding the respective critical components uses the 78M6613 Evaluation Board as an example. The board has a 2-layer plane assignment. Refer to the schematics in Appendix A.

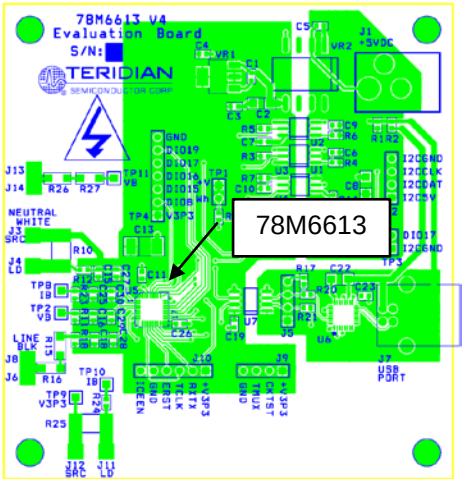

Figure 1: V3P3 Layer

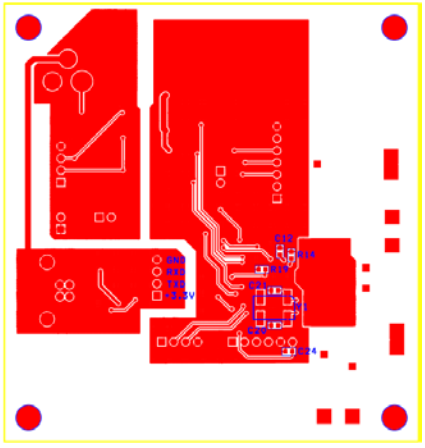

Figure 2: GND Layer

Crystal Oscillator Components

The 32.768 kHz crystal and its two 27 pF capacitors are placed on the GND layer. This allows the crystal and the two capacitors to be surrounded with a ground shield. Place the XIN and XOUT vias as close as possible to the 78M6613 pins. Shield the XIN and XOUT signal vias with copper plane on the V3P3 layer.

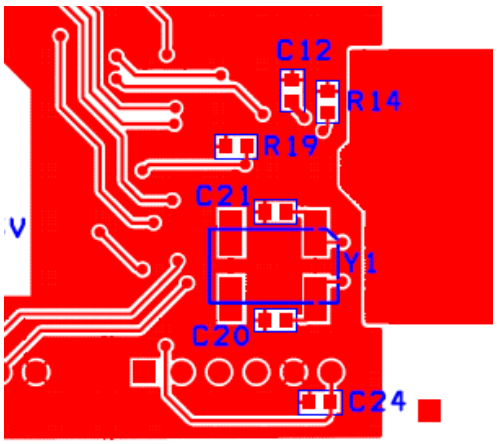

Figure 3: Crystal Y1 and Capacitors C20/C21

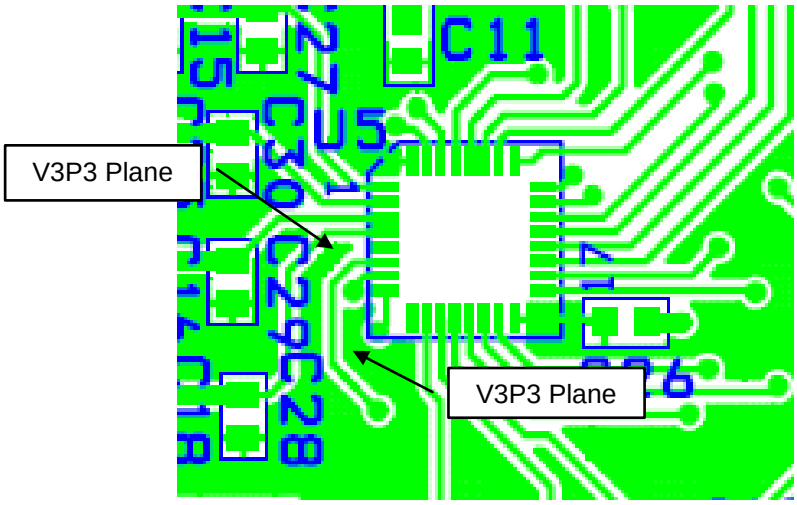

Figure 4: V3P3 Plane Surrounds Crystal Traces

LINE Voltage Resistor Network

Place the LINE voltage resistor network and its associated filter components on the V3P3 layer. Provide adequate high voltage isolation clearance around the 1 MΩ resistors. The 1000 pF and 0.1 µF anti-aliasing capacitors are placed next to the 78M6613's ADC inputs pins sensing the Line voltage (in this case A0 and A2). Place the 1000 pF capacitor closest to the 78M6613. Provide a V3P3 plane in the GND layer under the voltage resistor network components. Excluding the 1 MΩ resistors, include the 750 Ω resistor, anti-aliasing capacitors and the A0 and A2 pins over this V3P3 plane. Surround these components with V3P3 copper on the V3P3 layer. Interconnect the top and bottom V3P3 planes with multiple vias to provide a low impedance shield.

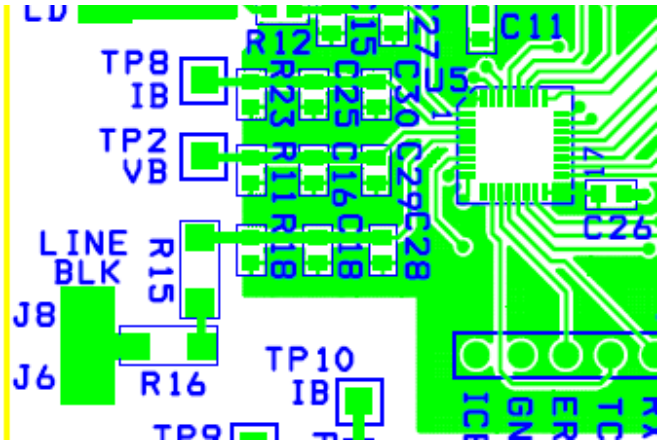

Figure 5: LINE Voltage Resistor Network

R16 and R15 are the 1 MΩ resistors and C18 and C28 are the anti-aliasing filter components.

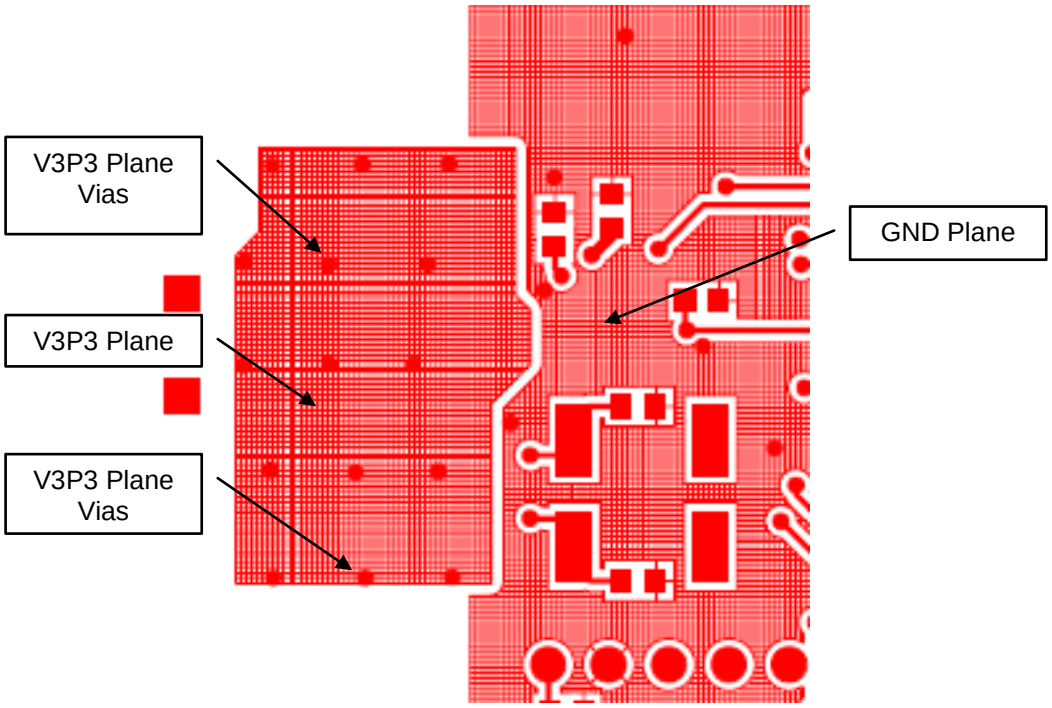

Figure 6: V3P3 Plane Sectioned Out of GND Layer

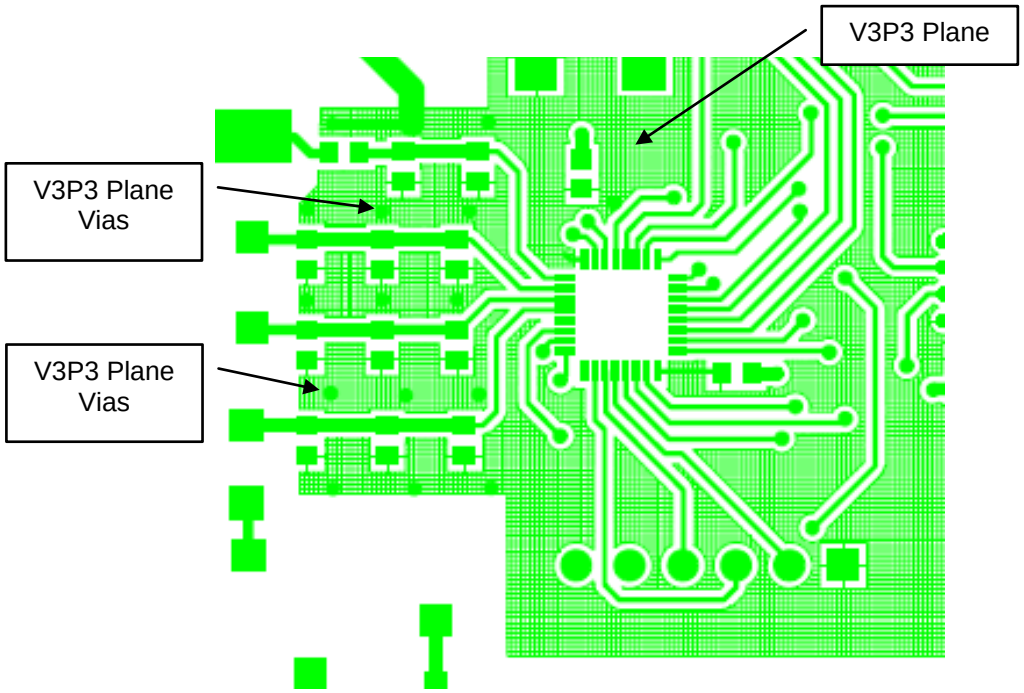

Figure 7: V3P3 Plane

Shunt Current Sensor

Place the shunt resistor and its associated filter components on the V3P3 layer. Provide adequate high-voltage isolation clearance around the shunt resistor. The 1000 pF and 0.1 µF anti-aliasing capacitors are placed next to the 78M6613's current sensing input (A1 and A3) pins. Place the 1000 pF capacitor closest to the 78M6613. Provide a V3P3 plane in the GND layer under the shunt filter components. Excluding the shunt resistor, include the 750 Ω resistor, anti-aliasing capacitors and the A1 and A3 pins over this V3P3 plane. Surround these components with V3P3 copper on the V3P3 layer. Interconnect the top and bottom V3P3 planes with multiple vias to provide a low impedance shield.

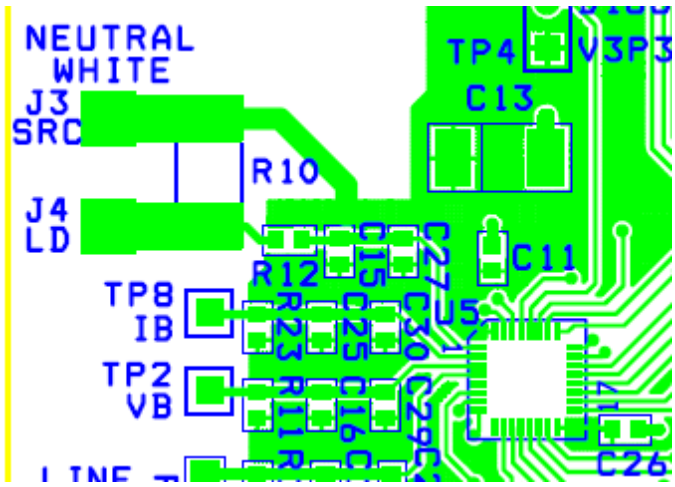

Figure 8: Shunt Current Sensor

R10 is the shunt resistor and C15 and C27 are the anti-aliasing filter components.

Dual Outlet 2-Shunt Current Sensor Topology

The 78M6613 supports two current sensors for dual outlet energy measurement applications. The same recommendations regarding isolation clearance, anti-aliasing filter component placement and V3P3 and GND plane shielding presented above apply to a dual-shunt printed circuit board layout.

However, placement of the two shunts is a very critical printed circuit board layout consideration. The two shunts must be located adjacent and equidistant from their common NEUTRAL connection. The sheet resistance of the copper trace is not “insignificant” relative to the low-ohms value of the current sensing shunt. Any extra trace length or unequal trace length from the NEUTRAL connection to each of the two shunts will produce measurement errors.

The following printed circuit board image (from a different evaluation board) shows two shunts in close proximity to their common NEUTRAL connector.

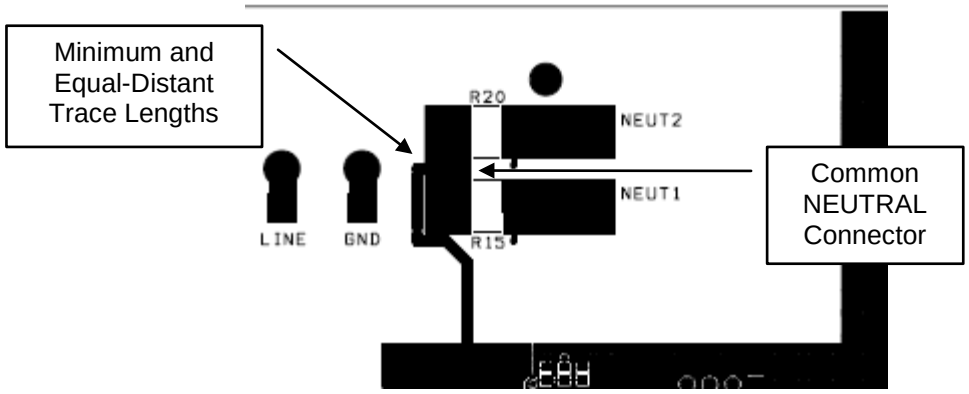

Figure 9: Dual Shunt Topology

R15 and R20 are the two current sensing shunt resistors. The NEUTRAL connector hole is in the middle of the two surface mount pads for R15 and R20.

V3P3 Decoupling Capacitors

Place the 1000 pF and 0.1 µF capacitors next to the 78M6613’s V3P3A pin. Add a 22 µF bulk capacitor in the vicinity of the V3P3D pin. Use multiple vias to connect the V3P3 plane sectioned out of the GND layer to bridge across the V3P3 layer. For example, the A0, A1, A2, A3 signals create islands in the V3P3 layer. The lower layer V3P3 plane reconnects the top side V3P3 plane for a solid reference plane.

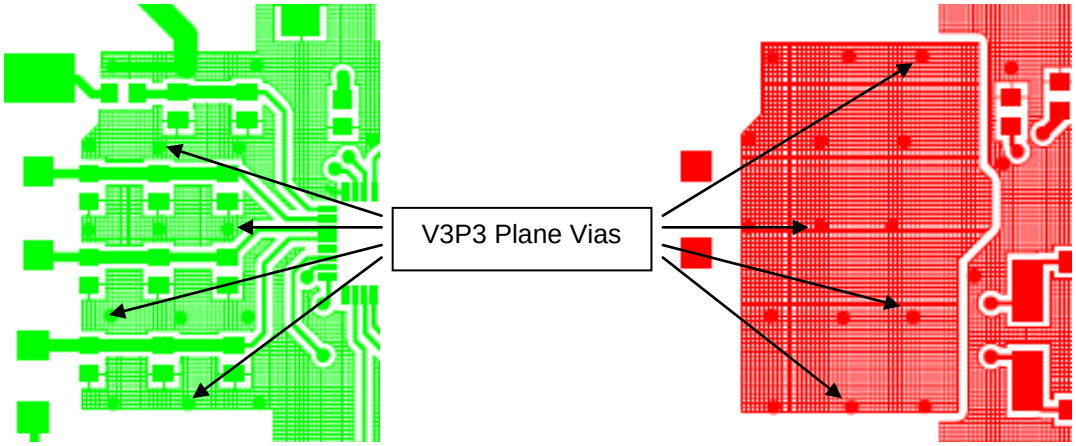

Figure 10: V3P3 Via Connections

In-Circuit Emulator Connector

Minimize the trace lengths of the ICE signals. This minimizes EMI susceptibility reducing the need for additional suppression components. Place the ICE_EN pull-down resistor close to the 78M6613. Place its companion 1000 pF capacitor at the ICE connector.

Systems Communication Interface

Any systems communication interface (UART, SPI, I2C) between the 78M6613 and external circuitry must be isolated to accommodate the -3.3V disparity in their GND pins (or, in the event of a LINE reversal). Depending on various requirements, a minimum clearance barrier must exist under the isolating components. A gap of 3 mm is the minimum requirement. Verify the isolating component's maximum barrier voltage meets your system requirements.

Appendix A – 78M6613 Evaluation Board Schematics

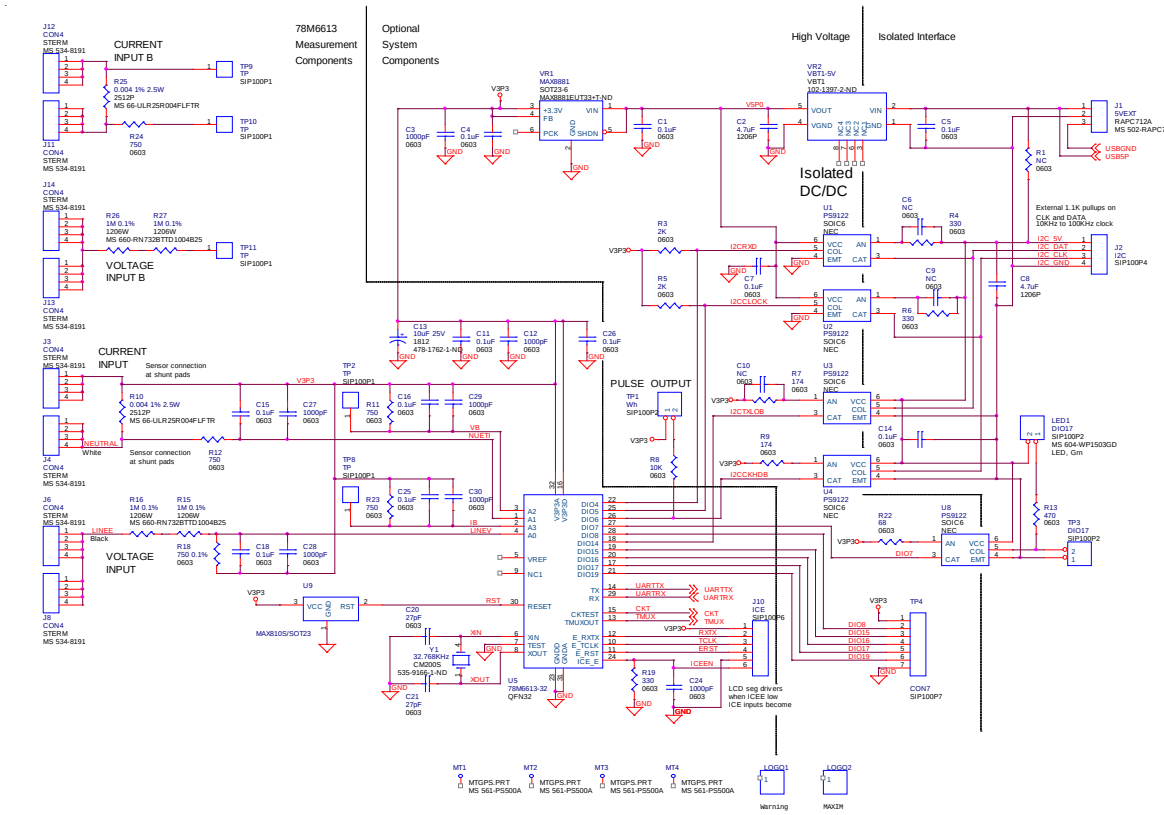

Figure 11: 78M6613 Evaluation Board Electrical Schematic (1 of 2)

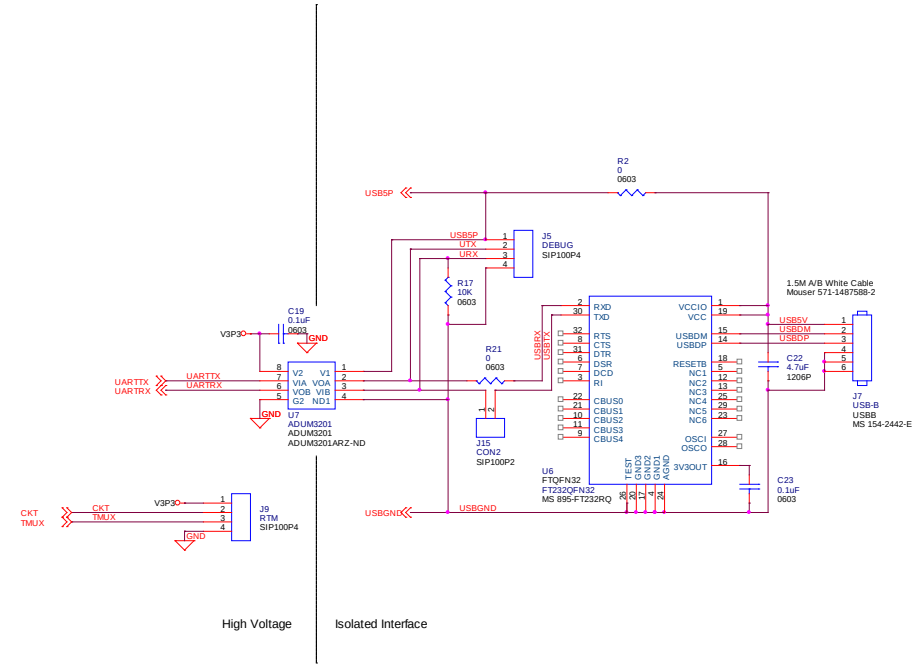

Figure 12: 78M6613 Evaluation Board Electrical Schematic (2 of 2)

Revision History

Revision	Date	Description
1.0	10/29/2010	First publication.

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