APPLICATION NOTE

AN_651X_043 MARCH 2008

Using the SSI Interface with the 71M651X Energy Meter Chips

The SSI Interface is designed to provide a fast data stream directly from the CE DRAM of the 651X Metering ICs to an external processor or data logger. Since any contiguous region of the CE DRAM can be selected to be the data source, any type of data accessible to the CE, such as front end ADC values, intermediate results, or energy-related data is easily accessible to the external processor. Since the data rate of the SSI is 5MHz or 10MHz (selectable), and the CE data is available in increments of four bytes (32 bits), a fast processor, such as a DSP must be used to capture the stream provided by the SSI Interface.
This Application Note describes how to configure and use the SSI Interface.

SSI Basics

SSI Signals

The four signals shown in Table 1 form the hardware part of the SSI Interface.

Signal	Description	Type	Pin Number (6511)	Pin Number (6513)	Pin Number (6515H)
SSCLK	Bit clock	Output	6	6	5
SSDATA	Data	Output	10	10	8
SFR	Frame synchronization	Output	11	11	9
SDRY	Handshake	Input	23	35	24

Table 1: SSI Signals

On the 71M6511 and 71M6513 chips, these pins are multiplexed with LCD segment outputs. This means that the SSI pins cannot be used as LCD segment drivers at the same time. On the 71M6515H chips, the SSI Interface can be used without restrictions.

The SFR pin provides a synchronizing (frame) pulse that can be used to identify the proper bit assignment in the data stream and/or to clock the data stream into registers. The polarity of this pin is selectable.

The SRDY pin is an optional handshake input.

It is not recommended to use the SRDY pin.

The SRDY pin must be tied to GNDD.

On the Teridian Meter Demo Boards, the SSI pins are accessible via headers or test points (6513: TP19, 6511: TP20, 6515H: JP6). In-line resistors are used between the pins of the meter chips and the test points, but not all Demo Boards are shipped with the resistors installed.

SSI Control Registers

The SSI Interface can be controlled via certain registers in I/O RAM (configuration RAM). These registers are accessible for the 71M6513 and 71M6511 via the command line interface (CLI) or via the emulator (ICE), and, of course, via MPU software. For the 71M6515H, access to the SSI control functions works indirectly via the serial communication protocol. The graphical user interface shipped with the 71M6515H Demo Kits allows access to the SSI Interface via a secondary menu. See the 71M6515H Demo Board Users Manual (DBUM) for details.

The I/O RAM registers of the 71M651X chips controlling the SSI Interface are shown in Table 2.

Register	Location	Description
LCD_EN	0x2021[5]	If SSI pins are used as LCD segments, this bit must be reset to 0 to disable the LCD before using the SSI Interface (71M6511 and 71M6513 only).
SSI_EN	0x2070[7]	This bit enables the SSI Interface.
SSI_10M	0x2070[6]	When this bit is set, the SSI clock speed is 10MHz, otherwise it is 5MHz.
SSI_CKGATE	0x2070[5]	This bit controls SCLK. When 0, the clock is continuous, when 1, the clock appears only when data is present, otherwise SCLK remains low.
SSI_FSIZE	0x2070[4:3]	These two bits control the function of the frame signal on the SFR pin: **Bit 4** / **Bit 3** / **Frame Format** 0 / 0 / One pulse for the whole SSI sequence 0 / 1 / One pulse every 8 bits 1 / 0 / One pulse every 16 bits 1 / 1 / One pulse every 32 bits
SSI_FPOL	0x2070[2]	This bit controls the polarity of the SFR pulse (0: positive, 1: negative).
SSI_BEG	0x2071[7:0]	The byte entered here defines the start address for the CE data block to be transmitted wit the SSI Interface.
SSI_END	0x2072[7:0]	The byte entered here defines the end address for the CE data block to be transmitted with the SSI Interface. *SSI_END* must be > *SSI_BEG*.

Table 2: I/O RAM Registers Controlling the SSI Interface

SSI_BEG and *SSI_END* are pointers to CE word addresses. Thus, entering 0x20 in *SSI_BEG* means that the byte address corresponding to word address 0x20 is selected, which amounts to 0x1000 + 4 * 0x20 = 0x1080.

Table 3 shows the bits in I/O RAM register 0x2070.

Bit	Name	Function	Comment
7	*SSI_EN*	Enables the SSI Interface.	
6	*SSI_10M*	SSI clock speed control	
5	*SSI_CKGATE*	SCLK control.	See Figure 6.
4	*SSI_FSIZE*	These two bits control the function of the frame signal (SFR)	See Figure 2, Figure 3, Figure 4
3	*SSI_FSIZE*		
2	*SSI_FPOL*	Controls the polarity of SFR	See Figure 5.
1	*SSI_RDYEN*	Flow control	**This bit must be zero.**
0	*SSY_RDYPOL*	Polarity control for SRDY	**This bit must be zero.**

Table 3: Bits of I/O RAM Register 0x2070

SSI Timing

Figure 1 shows the SSI timing. SFR is shown for three different formats: On top is the SFR pulse preceding the whole SSI data block (when *SSI_FSIZE* is 0). One line below, SFR (16 bits) shows the SFR bits marking every 16 bits (when *SSI_FSIZE* is 2), and SFR (32 bits) shows the SFR bits marking every 32 bits (when *SSI_FSIZE* is 3).

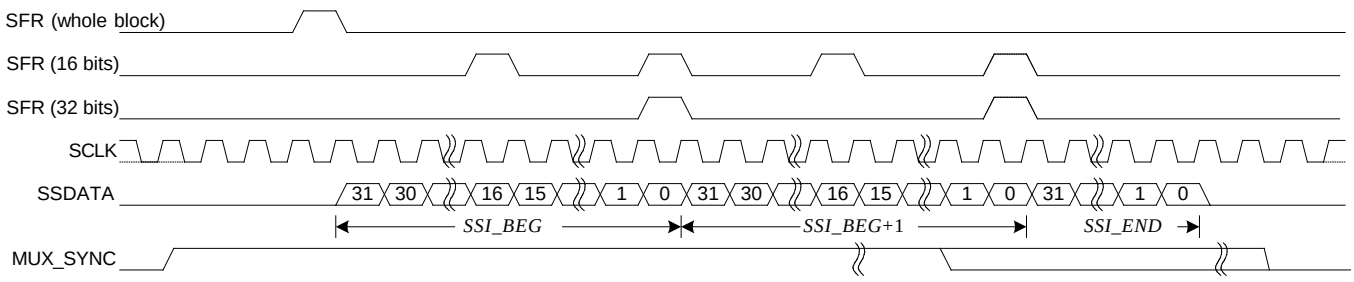

Figure 1: SSI Timing

The SFR pulse is one SSCLK cycle wide and precedes the first bit of each field. CE DRAM words are shifted out with the MSB first, starting at the address selected by *SSI_BEG*.

The SSI data stream starts one cycle of the 32kHz clock before each CE code pass. This time interval is equivalent to 30.5µs, and at 4.9152MHz SSI clock speed, 150 bits will fit into this time interval, which is equivalent to four complete CE DRAM words (or nine CE words at 9.8304MHz).

If more CE DRAM words are selected for transmission, the data stream will continue into the CE code pass without any effect on CE performance or data. The only caution in this case is that a particular CE DRAM data location may be changed by the CE before it is streamed out to the SSI or after it is streamed out, depending on the relative timing between SSI data stream and CE code progress. In other words, it is generally unknown to the user whether a particular datum will be the result of the previous CE code pass or of the current CE code pass.

The maximum time period for a SSI transmission is equivalent to the selected ADC multiplexer frame, which defaults to 397.7µs, or 1950 SSI data bits (60 CE DRAM words). At 9.8304MHz SSI clock speed, 3900 bits, or 121 CE words, can be transferred.

Figure 2 through Figure 6 show timing examples, obtained from a 71M6513 chip.

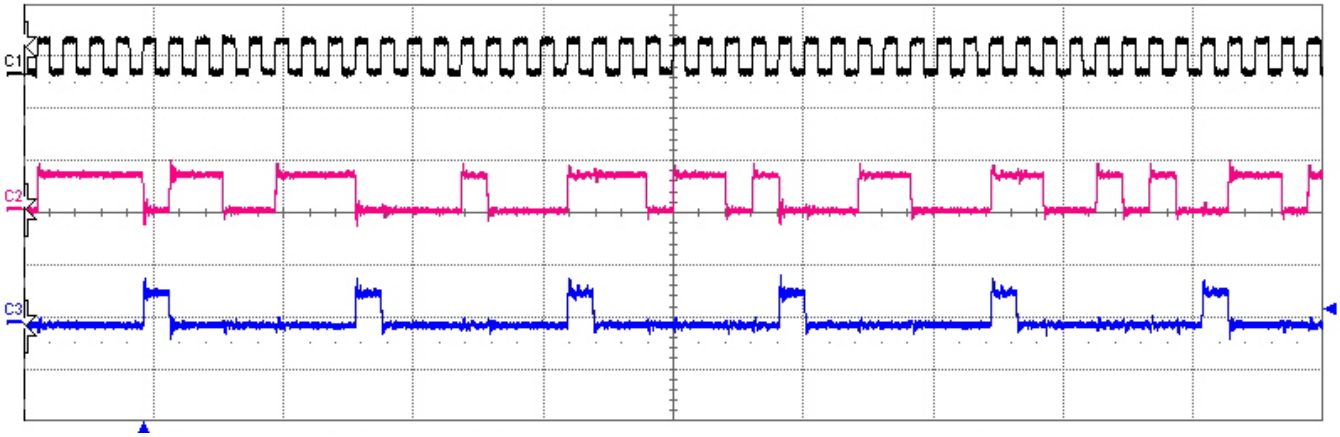

Figure 2: SSI Timing – SFR Set for 8 Bits

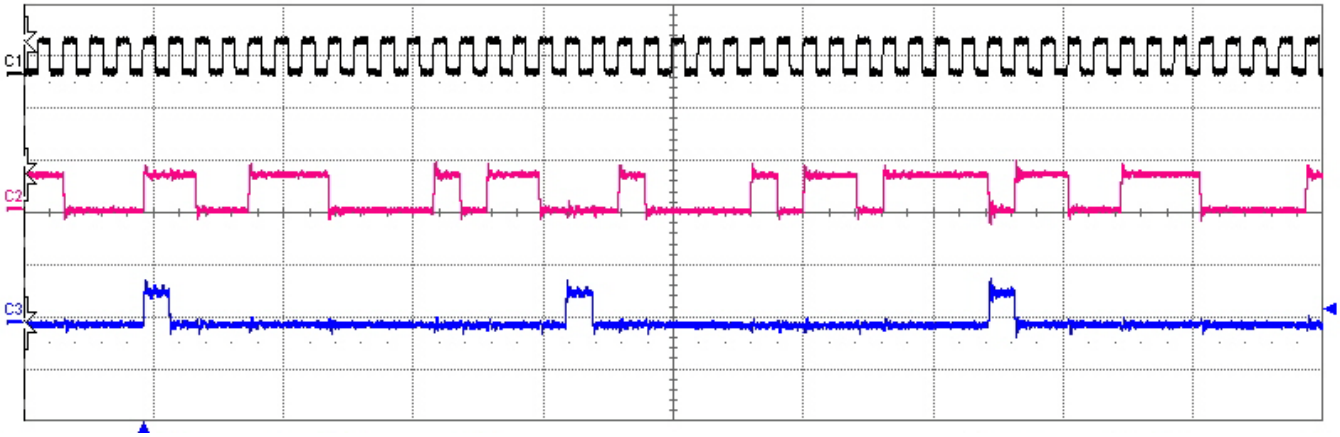

Figure 3: SSI Timing – SFR Set for 16 Bits

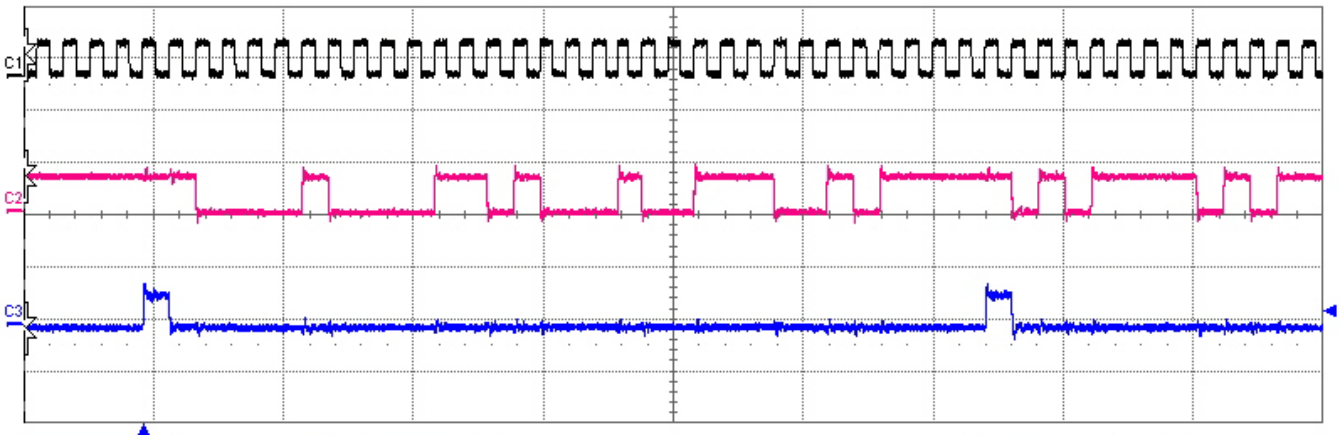

Figure 4: SSI Timing – SFR Set for 32 Bits

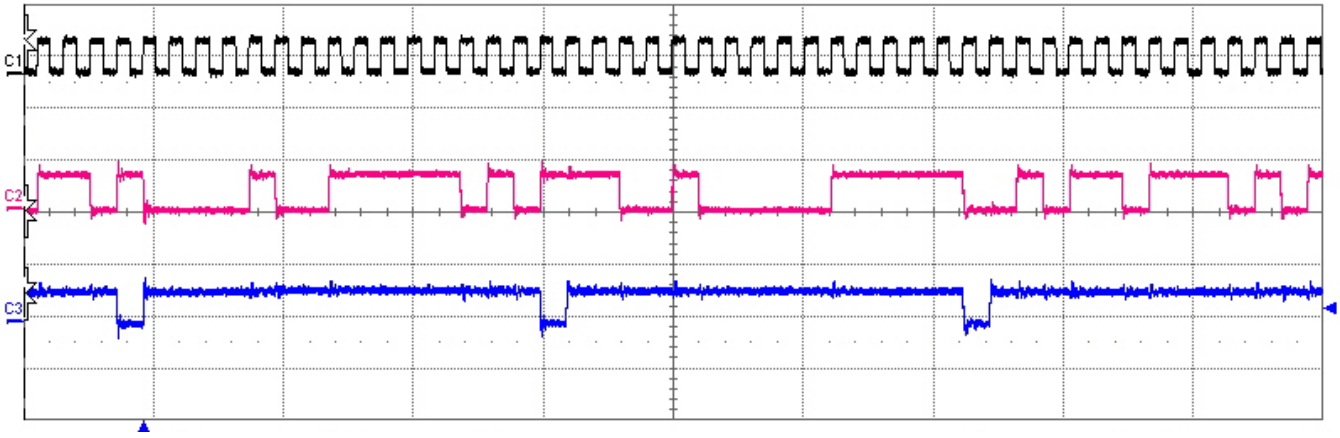

Figure 5: SSI Timing – SFR Polarity Inverted

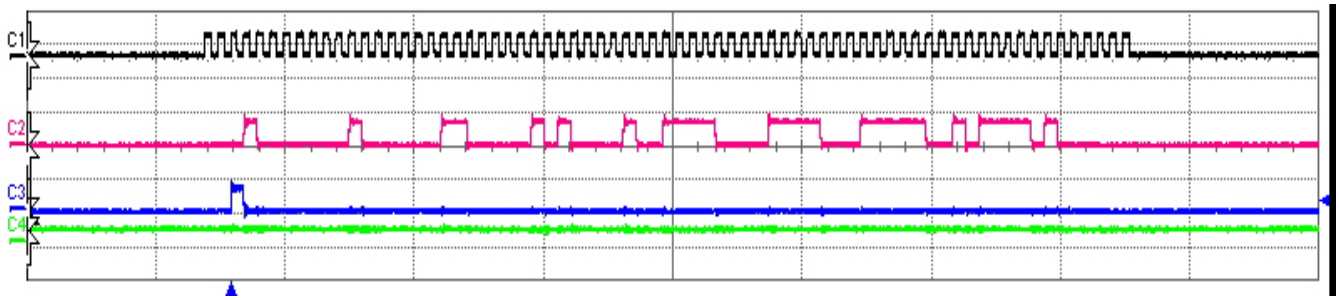

Figure 6: SSI Timing – SSCLK Gated Using *SSI_CKGATE*

Considerations for the DSP or Data Logger

It is obvious that only a device capable of processing a high-speed data stream, such as a DSP or FPGA should be used to access SSI data.

Multi-channel buffered serial ports, clock-stop modes, and selectable data sizes, as used on many common DSPs and other processors can take advantage of the SFR bits and gated SSCLK to process the data stream from the 71M651X SSI.

If no provision for serial data input at 5MHz or 10MHz exists, the SSI data stream from the 71M651X can still be serially clocked into serial-to-parallel registers and then read out as parallel bytes or words. Serial-to-parallel shift registers that can be used for that purpose are widely available (for example 8 bits: 74HCT164, 16 bits: 74LS673).

Revision History

Revision	Date	Description
Rev. 1.0	3/29/2007	First publication.
Rev. 1.1	3/29/2007	Updated Teridian street address information and added e-mail address. Corrected typo in register description table. Added text at *SSI_END*: "The byte entered here defines the end address for the CE data block to be transmitted with the SSI Interface. *SSI_END* must be > *SSI_BEG*."

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