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Using the Optical Port of the Teridian 71M6511/71M6513

Many designers want to use the optical port of the 71M6511/6513 to have the chip communicate with portable devices. In end applications, this way of communicating is necessary for optical meter reading, maintenance or updates. The optical isolation helps keeping dangerous voltages away from the outside of the meter and maintains the integrity of the meter enclosure.

Using IR Diodes and Phototransistors

Optical interfaces to electricity meters are usually designed to IEC1107 or ANSI C12.18 standards. These standards specify data rates, character format, transmission protocol as well as the optical and mechanical parameters of the optical interface.

Only two optical components are required: A transmitter (usually an infrared emitting diode) and a receiver (usually a photo-transistor). Using only a few additional passive components an optical interface can easily be implemented. A variety of manufacturers offer optical components with comparable parameters, such as performance, spectral characteristics, and operating currents.

Optek, a manufacturer of photo-semiconductors (http://www.optekinc.com) recommends the combination of their devices OP233 and OP804SL to bridge a 1" or larger distance. The selection of these two devices is not arbitrary: First, there has to be a spectral match (890nm wave length in this case), and second, it helps to select a transmitter that "bundles" the light in a relatively sharp cone, very much like a flash light, plus a receiver that has a narrow receiving angle.

As a safe starting point, one of the circuits shown in Figure 1 should be used. The resistor R1 can either be at the collector or at the emitter of the photo transistor. Depending on desired communication speed and distance, various parameters of this circuit can be modified once it is tested.

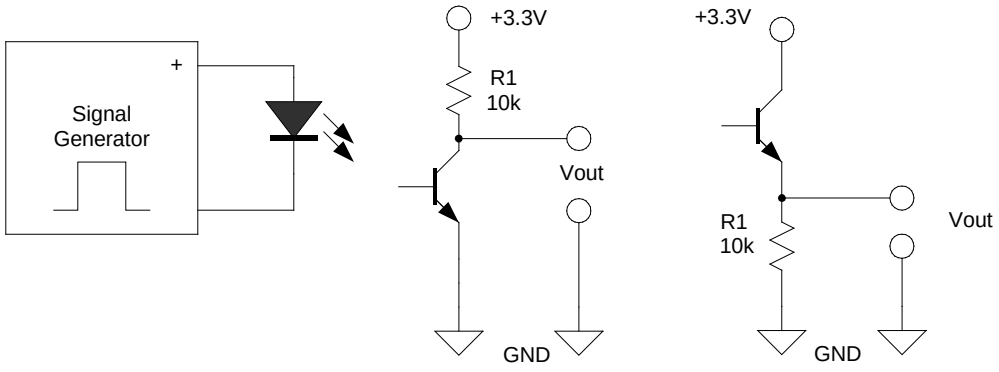

Figure 1: Basic Optical Circuits: Transmitter (left), non-inverting receiver (center), inverting receiver (right)

With the IR light off, the transistor will be in the off state and it will provide only its residual current, consisting of leakage current and the current caused by the background radiation. If R1 is connected to the emitter, this residual current will lift the output voltage V_{out} slightly above zero Volts. The lower R1 is chosen, the lower the "logic" output level will be. Once the transistor is irradiated with IR light, it transitions to its on state, pulling the output voltage up. The OP408SL easily generates between 7 and 20mA when saturated. That way, the transition of the output signal from low to high is usually very fast. In the opposite direction, the resistor R1 has to remove the charges from the saturated transistor and overcome charges in parasitic capacitors. This usually causes the transition from high to low to be much slower.

When R1 is connected to the collector, the transistor has to "work" to get the output voltage close to zero. However, this circuit has the advantage that no signal inversion occurs.

In bench tests it was possible to bridge more than 2" with the circuit from Figure 1, when the IR diode was driven with a peak amplitude of only 0.6V. It should be noted that the OP233W device used for this test has a **wide** irradiance pattern. This means, larger distances will be possible with devices such as the OP233 that bundle the emitted light.

The "base" of the photo-transistor is brought out as a pin for some transistor models. In the test circuits, the base pin was left unconnected. It may as well be cut off to limit interference from electromagnetic fields. One potential application for the base is when background radiation has to be suppressed. This can be done by tying the base with a high-ohmic resistor (1MΩ) to the collector.

For practical tests, it is best to mount both photo devices in a tube that keeps them axially aligned while the distance between them can be manipulated (Figure 2).

While driving the OP233W with the 100Ω series resistor, a 25mm distance was bridged at 9,600bps. To achieve this, R1 was reduced to 1kΩ (R1 at emitter). This reduced the switching time and varied the output amplitude, which was then close to 0V in the off state and above 2V in the on state. The signal obtained at the phototransistor is shown in Figure 3, the slower signal resulting from using a 5kΩ resistor for R1 is shown in Figure 4. With R1 = 5kΩ, a settling time around 100µs was achieved, with R1 = 1kΩ the settling time decreased to around 40µs.

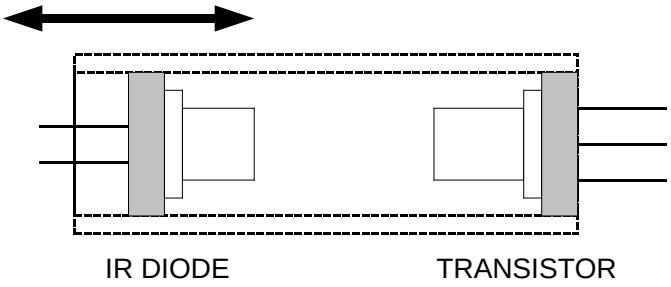

Figure 2: Mechanical Arrangement for IR Diode and Photo-Transistor

The voltage swing achieved with R1 = 1kΩ is ideal for driving the 71M6511/6513 OPT_RX input pin with its threshold voltage specified between 200mV and 300mV. The output voltages of the photo-transistor should be adjusted to stay safely away from the 200 to 300mV band in all operating conditions. IR diodes and photo-transistors have temperature effects that have to be taken into consideration. For instance, the light output of the OP233W decreases to 75% at 50°C.
Much faster switching times may be achieved by using so called photo-logic devices such as the OPTEK OPL801-OC. These devices guarantee CMOS logic output levels while keeping rise and fall times below 1µs.

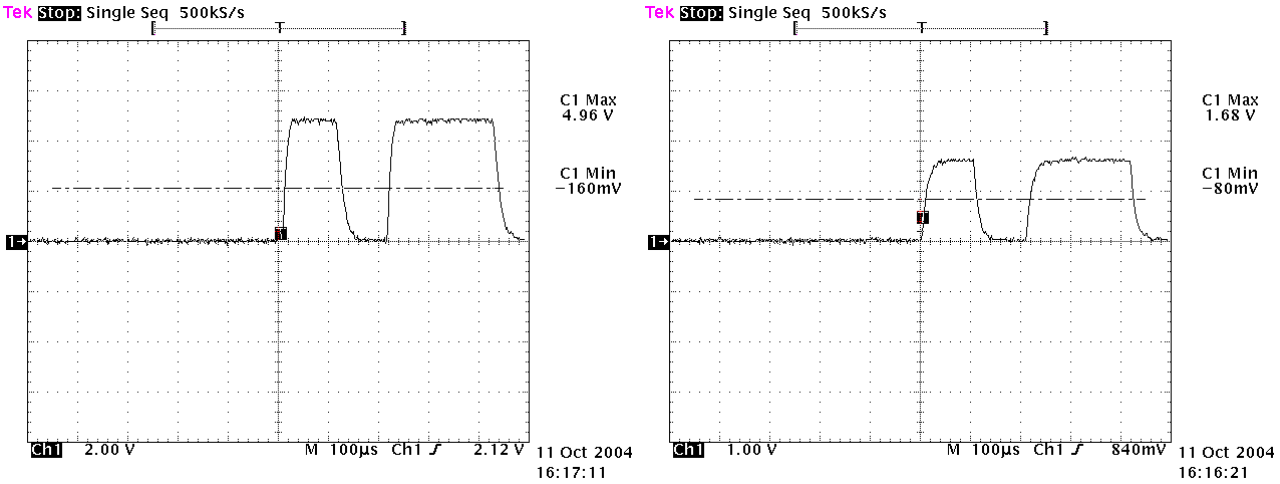

Figure 3: 9600 bps signal at Phototransistor w/ R1 = 1kΩ at 12.5mm (left), 25mm (right)

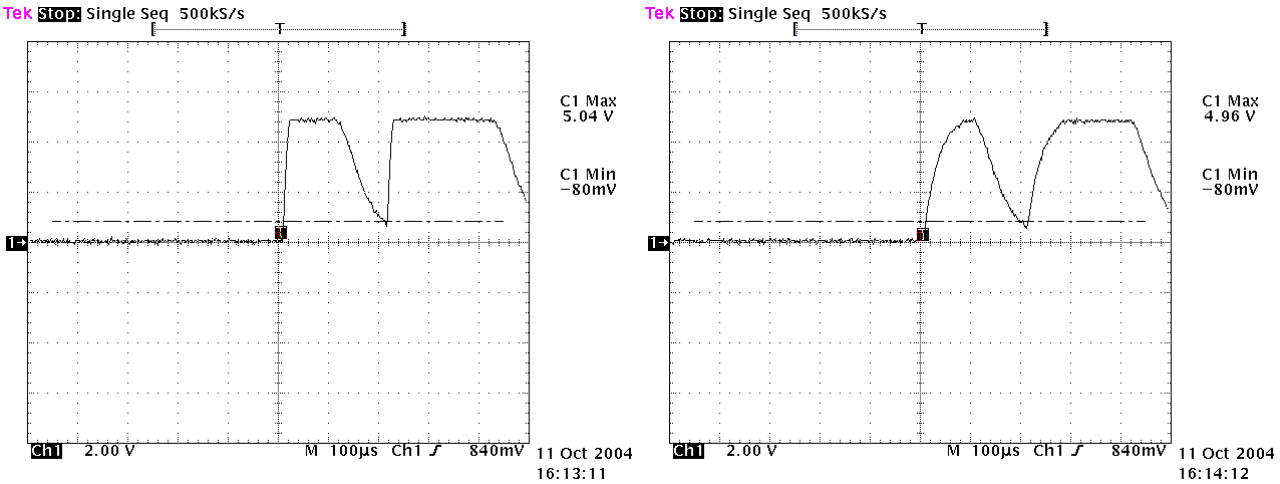

Figure 4: 9600 bps signal at Phototransistor w/ R1 = 5kΩ at 12.5mm (left), 25mm (right)

The Optical Port of the 71M6511/6513

In the data sheets, the optical port consisting of pins OPT_TX and OPT_RX are specified for the connection of electro-optical components. In order to make a transmission, the OPT_TX pin which is normally tri-stated, has to be enabled (the *OPT_TXDIS* bit must be cleared). This can be done manually by issuing the command **>RI08=0C** via the serial interface (normally, the DIO location 2008 reads 0x2C, which means that the *OPT_TXDIS* bit is set, disabling the OPT_TX pin). Demo code firmware generated after 10/6/2004 will automatically enable the OPT_TX pin when the serial ports are switched from primary to optical port using the **>SP1** command.

For test purposes, the command **>)1=8** can be issued. This command will cause the demo code to send a string of about 32 characters in a loop, repeating once a second. Even without the presence of an optical link, port activity can then be monitored with an oscilloscope, and the contents of the test string can be displayed on a terminal if a CMOS-to-RS232 level translator is used. This test is usually the first step of establishing an optical link.

Shorting the pins 1 and 2 of header J12 provides simulation of a zero-Ohm IR diode (see Figure 5). A short-circuit sink current of roughly 30mA can be obtained from the OPT_TX pin, which is usually sufficient to bridge a 1” to 2” distance between an IR diode and a matched photo-sensitive transistor.

Implementing an Optical Link with the Demo Board

If the Demo Board is used its schematic should be studied carefully in order to determine the proper connection of the optical components. R85 could be used to implement the emitter resistor for the inverting configuration. If the non-inverting configuration is used, R85 must be removed. For proper coupling of the high potential to the OPT_RX pin, the capacitor C21 is bridged with a wire (see Figure 5).

In the Demo Boards, the current limiting resistor R79 is provided in between the OPT_TX pin of the chip and pin 2 of J12 (see Figure 5).

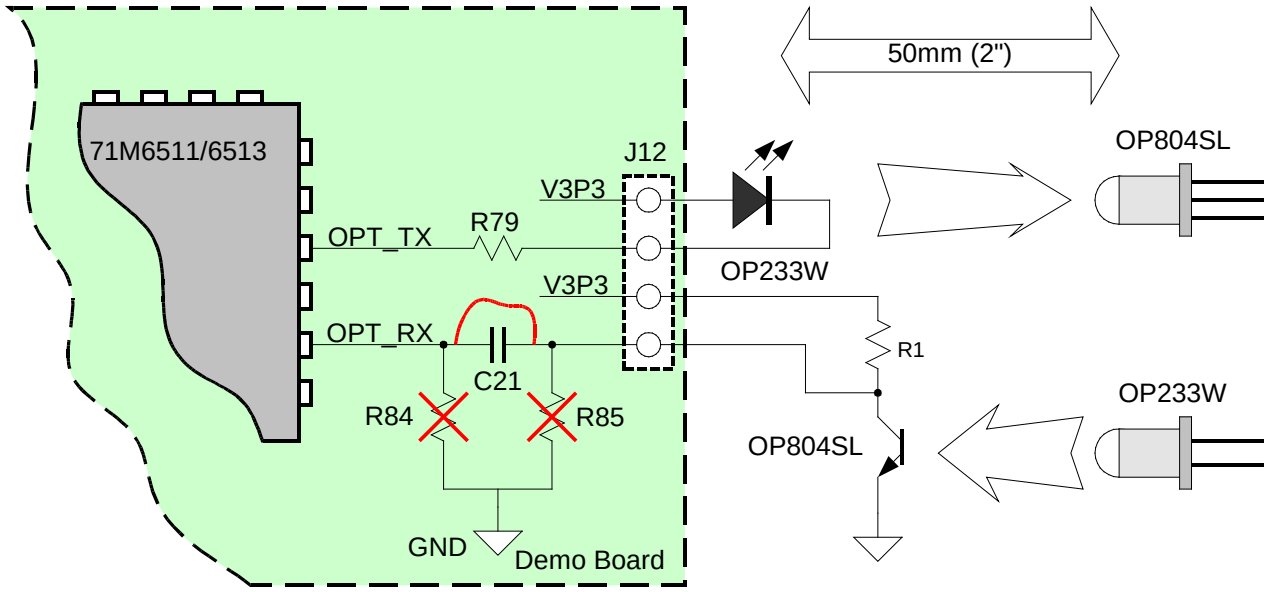

Figure 5: Connecting an IR diode and photo transistor on the Demo Board

The IR diode should be connected between terminal 2 of header J12 on the Demo Board (cathode) and the V3P3 voltage (anode), which is accessible at terminal 1 of header J12 (see Figure 3). If the diode current must be varied, R79 can be increased or decreased.

Diode Current

Current can be saved by increasing R79. Consequently, a certain decrease in signal will occur. However, with careful selection of the components on the receiving side, the signal can still be received at minimum diode drive currents.
Figure 6 shows the output voltage swing of the receiving transistor OP804SL as a function of the current-limiting resistor (Rx = R79) at two distances. As can be seen, even at 1600Ω, a useable amplitude of 160mV can be achieved with a distance of 12.5mm (1/2”).

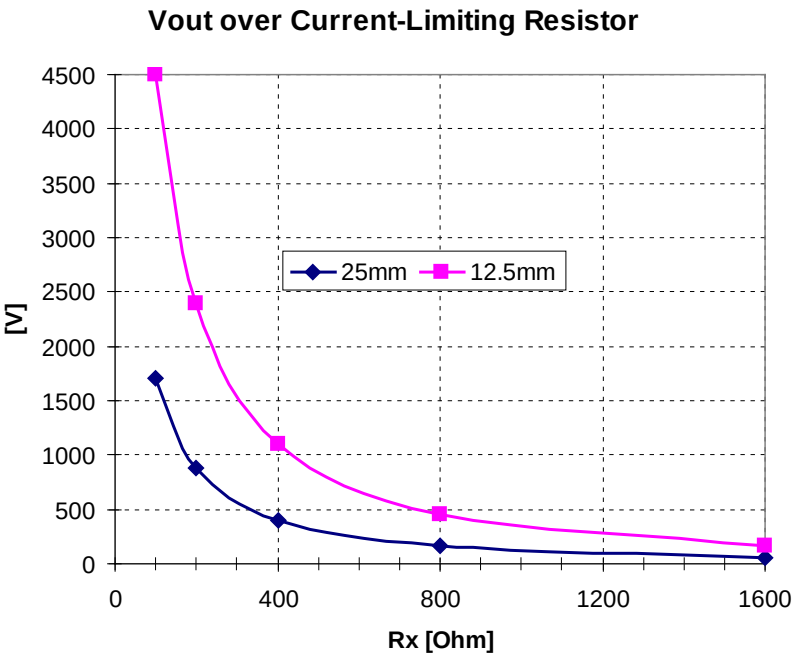

Figure 6: Useable Receiver Voltage

Figure 7 shows the diode current as a function of the current limiting resistor Rx (R79). As can be seen in the graph, at Rx = 100Ω, the diode current does not exceed 16mA.

Note: Optek recommends to operate the diode above 5mA in order to guarantee operation in the linear region.

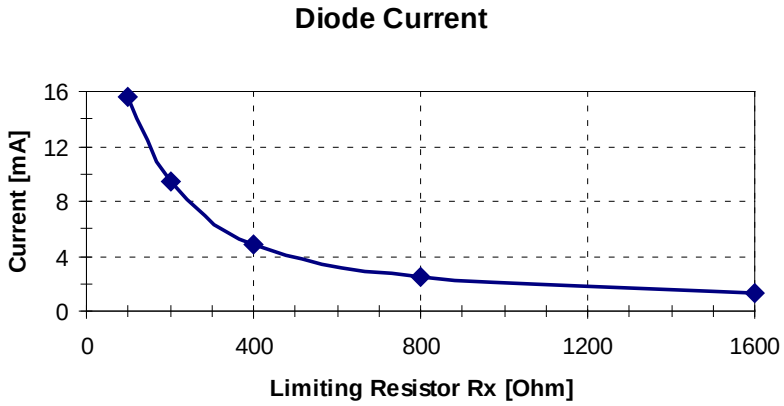

Figure 7: Diode Current

Signal Polarity

Components for asynchronous interfaces almost always treat "HIGH" (CMOS/TTL levels) as the quiescent state. Once, the signal is pulled "LOW" by the transmitter, the start of the character is detected by the receiver.

This polarity is maintained in our optical circuit if we use the basic circuit that has the resistor connected to the collector of the photo transistor. The transmitter pulls the cathode of the IR diode "**LOW**" in order to generate light. Receiving the light (active) will generate a "**LOW**" signal which, again, is defined as active (see Figure 8).

Care must be taken to generate the proper active voltage level (i.e. <200mV if connected to the OPT_RX pin of the 71M651X) when the transistor receives light. Higher values of R1 will promote clean signal levels while lower values of R1 will improve the timing. Figures 9 through 12 show signals received with the circuit from Figure 8. Up to 40kHz could easily be transmitted while maintaining clean signal levels for the active state.

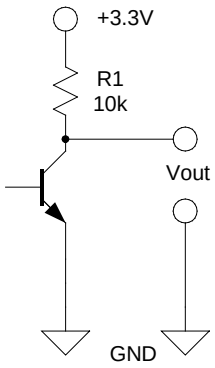

Figure 8: Alternative Receiving Circuitry

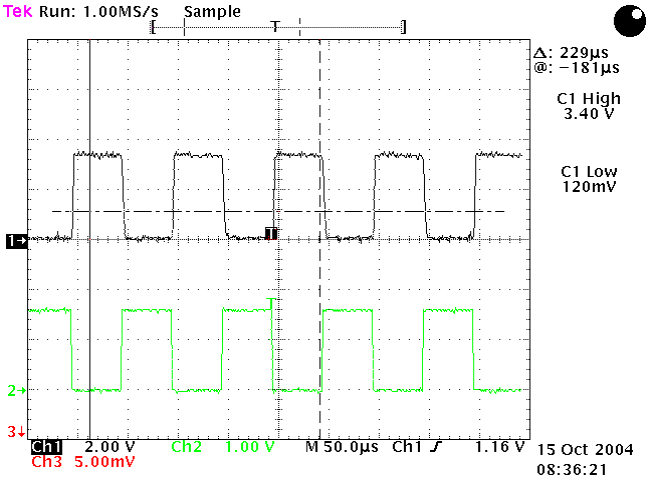

Figure 9: Rc = 800Ω, 10kHz

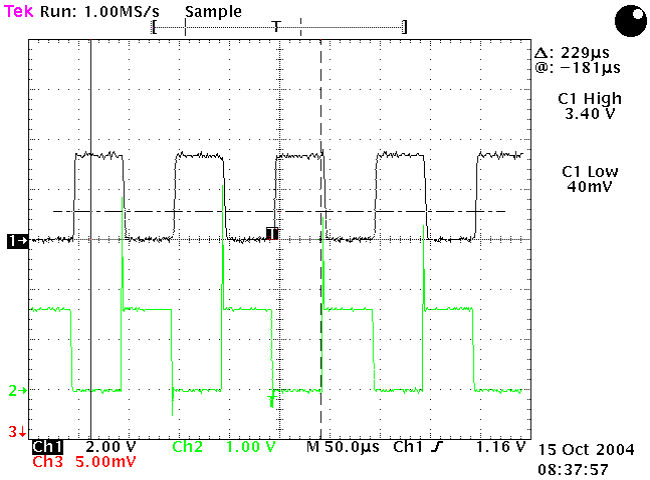

Figure 10: Rc = 3.2kΩ, 10kHz

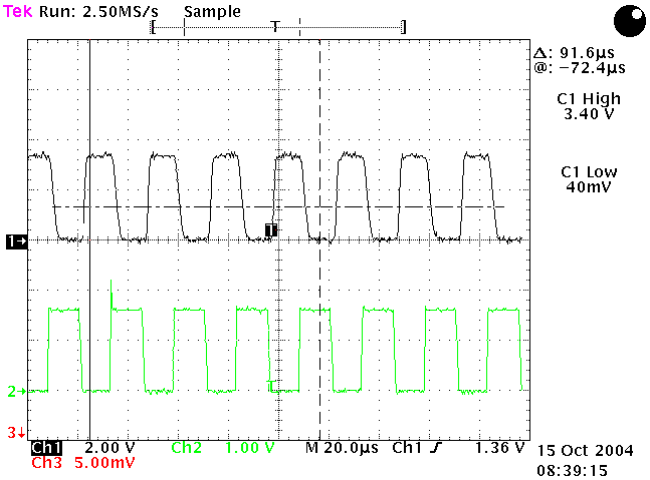

Figure 11: Rc = 3.2kΩ, 40kHz

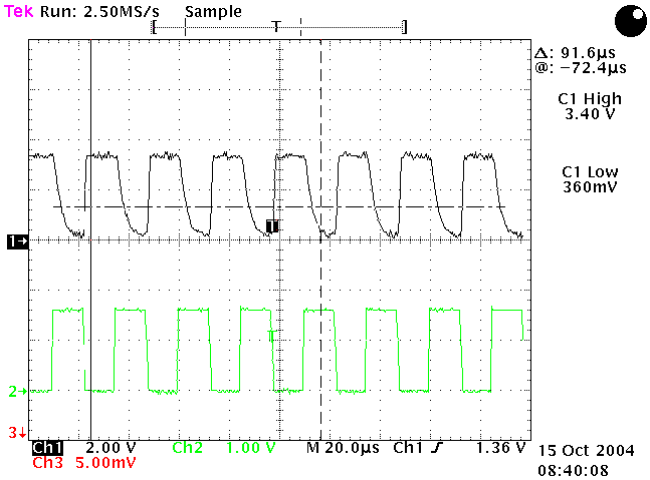

Figure 12: Rc = 400Ω, 40kHz

Inter-Byte Delay

Inter-byte delay can be measured with an oscilloscope directly at the OPT_TX pin of the 71M6511/6513 while transmitting the test string in a loop (see above). Typically, the delay is 400µs to 600µs (see Figure 13). Occasionally, a larger gap of about 1ms can be observed, probably due to a higher priority interrupt being serviced by the demo code

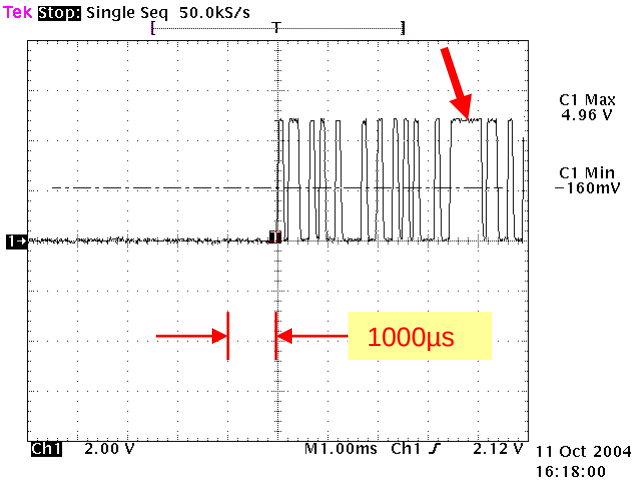

Figure 13: Asynchronous 9600bps Signal with inter-byte delay (arrow)