AN_651X_009 MAY 2010

Temperature Compensation for the 71M651x/651xH, 71M652x, and 71M653x Energy Meter ICs

Meters based on the 71M6511H, 71M6513H, 71M6533H, and 71M6534H are expected to be accurate within 0.126% over the industrial temperature range. The 71M6511, 71M6512, 71M6521, 71M6523, 71M6531 and 71M6513 ICs provide 0.5% accuracy. For both types if ICs, the high accuracy of energy measurements is achieved by applying temperature correction techniques. This application note explains how electricity meters based on the TERIDIAN 71M65xx Family of ICs can be programmed to compensate for temperature effects.

The second part of this application note examines compensation techniques for the RTC.

Temperature Effects in Meters

Meters based on the TERIDIAN Energy Metering ICs will be exposed to various temperatures during service. Usually, changes in temperature cause parameters of electronic components to change. Since a typical meter consists of the metering IC surrounded by mostly passive components, the temperature characteristics of the meter will depend on both the metering ICs' characteristics and the characteristics of the other meter components.

Internal and External Temperature Compensation

If we consider only the temperature characteristics of the TERIDIAN Metering ICs while ignoring the other meter components, we find that the temperature-dependent functions are concentrated solely in the reference for the ADC.

The AC-nature of the analog front end eliminates temperature-dependent offsets. As with many sigma-delta converters, there is no gain circuit, buffer or other analog circuitry between the analog input pins and the ADC. Thus, temperature effects are narrowed down to one area: The drift of the reference voltage itself over temperature. Drift of the amplifier for the reference voltage is eliminated by operating this amplifier in chopping mode. Since the TERIDIAN Metering ICs implement an absolute (not ratio-metric) measurement scheme, the stability of the reference itself becomes very important for overall meter accuracy.

The behavior of a typical band-gap reference voltage over temperature is plotted in Figure 1. The curve shape is basically a parabola with a slight tilt and can be sufficiently described with a second order polynomial.

If the reference voltage is lower by only 2.0 mV at +85°C, or roughly 1,675 PPM, the meter will have a temperature dependency of the energy measurement of 2 x 1,675/60 PPM/°C, or close to 56 PPM/°C between +25°C and +85°C. Measured energy will be 0.335% higher at +85°C with respect to +25°C, which is acceptable for a class 0.5 meter, but not for a class 0.2 meter.

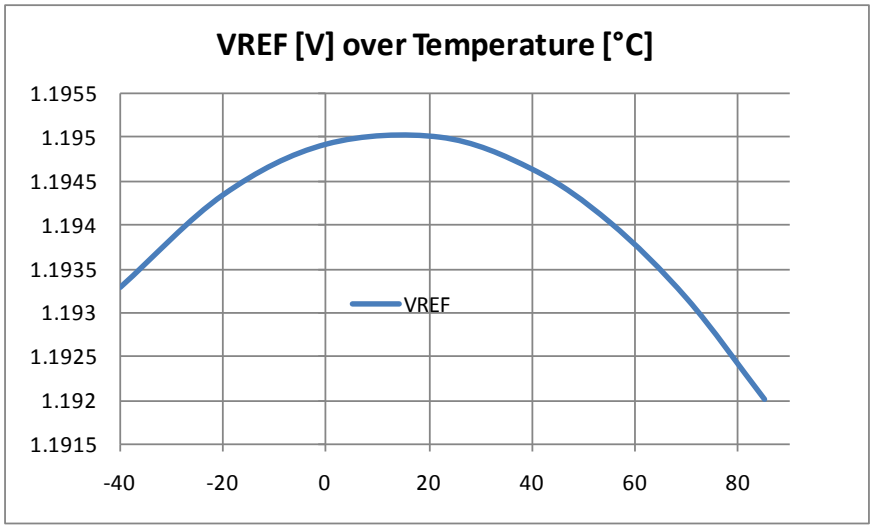

Figure 1: Typical Reference Voltage over Temperature

To improve accuracy over temperature, the CE code has a mechanism that can compensate for the linear and quadratic characteristics of the voltage reference over temperature. This is called internal temperature compensation, and the magnitude of compensation will be based on the CE variables *PPMC1* and *PPMC2*.

If we consider both the metering ICs and the other meter components with their temperature characteristics, we are treating the meter as a system. From this perspective we have to recognize that many more effects influence the meter characteristics over temperature than just the fluctuation of the reference voltage. These effects may be much more complex than what can practically be implemented with the simple compensation mechanism of the CE. The task of complex compensation can be offloaded to the MPU. This mode is called external temperature compensation. In this mode, the MPU calculates a gain correction based on all its input parameters and commands the CE to adjust the gain accordingly.

Figure 2 shows functional block diagrams of internal and external temperature compensation for comparison.

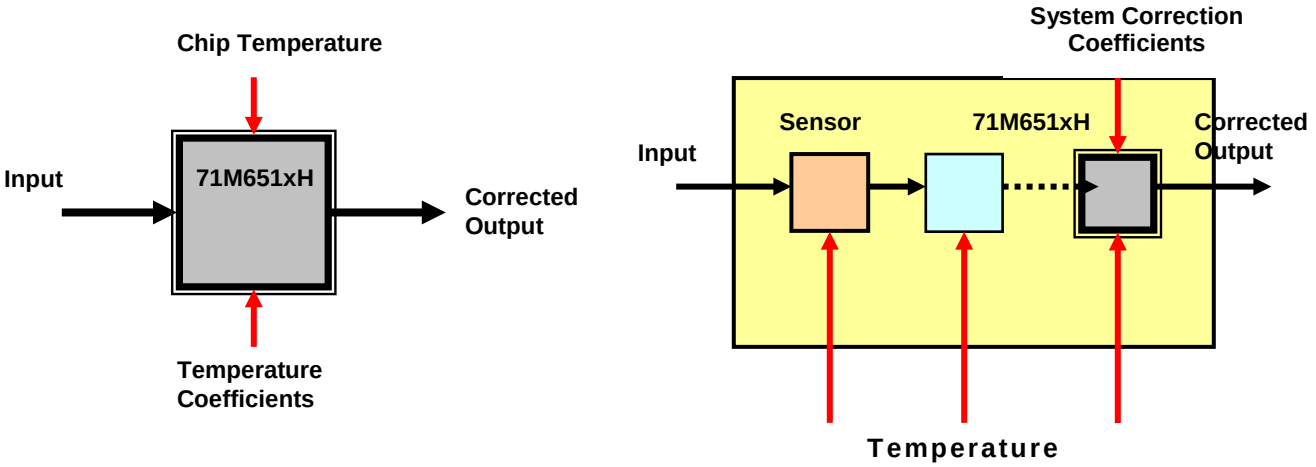

Figure 2: Internal (Left) and External (Right) Temperature Compensation

For the 71M651x CE codes, the register *EXT_TEMP* controls which type of compensation is used (see Table 1). For the other Teridian Metering ICs equivalent bit fields exist in the CE code addresses.

EXT_TEMP	Type of Compensation	Compensation by	Compensation based on
0	Internal	CE	*PPMC1, PPMC2*
15	External	MPU	Parameters implemented in MPU code

Table 1: Function of *EXT_TEMP*

Temperature Coefficients for 71M651x and 71M651xH Parts

For the 71M651x, 71M652x, 71M653x and other parts without the "H" suffix, typical temperature coefficients (TC1 and TC2) are given that make it possible to compensate the behavior of the reference voltage to within ±40 PPM/°C over the temperature range of –40°C to +85°C. TC1 and TC2 represent the average of all chips and thus approximate the temperature coefficients of a typical chip with reasonable tolerance.

This concept is reflected in the data sheets for the non-H parts as the deviation of VREF from VNOM (±40 PPM/°C).

The 71M651xH and other parts with the "H" suffix receive an additional process step: During production these chips are heated up to +85°C, and the reference voltage is measured at that temperature. The deviations from the nominal reference voltage at room temperature and at +85° are then stored in on-chip fuses that can later be read by the MPU firmware in order to generate individualized coefficients TC1 and TC2, allowing the reference voltage to be predicted within ±10 PPM/°C. This value is specified in the data sheet for the H-parts as the deviation of VREF from VNOM (±10PPM/°C). This tight tolerance allows the measured signals to be reconstructed with high accuracy under any temperature environment.

If we examine the data sheet closely (see Table 2), we notice that the achievable deviation is not strictly ±10 PPM/°C over the whole temperature range: Only for temperatures for which T-22 > 40 (i.e. T > 62°C) or for which T-22 < -40 (T < -18°C), the data sheet states ±10 PPM/°C. For temperatures between -18°C and +62°C, the error can be considered constant at ±400 PPM, or ±0.04%.

VREF(T) deviation from VNOM(T) $\frac{VREF(T)-VNOM(T)}{VNOM}\frac{10^6}{\max(\lvert T-22\rvert,40)}$		-10		10	ppm/ºC

Table 2: VREF Definition for 6513H

Figure 3 shows this concept graphically. The “box” from -18°C to +62°C reflects the fact that it is impractical to measure the temperature coefficient of high-quality references at small temperature excursions. For example, at +25°C, the expected error would be ±3°C * 10 PPM/°C, or just 0.003%.

The maximum deviation of ±620 PPM is reached at the temperature extremes. This deviation is equivalent to ±0.062%. If the reference voltage is used to measure both voltage and current, as is the case with Metering ICs of the 71M651x, 71M652x, and 71M653x families (and also 71M654x in CT mode), the identical errors of ±0.063% add up to Wh registration error of ±0.126%.

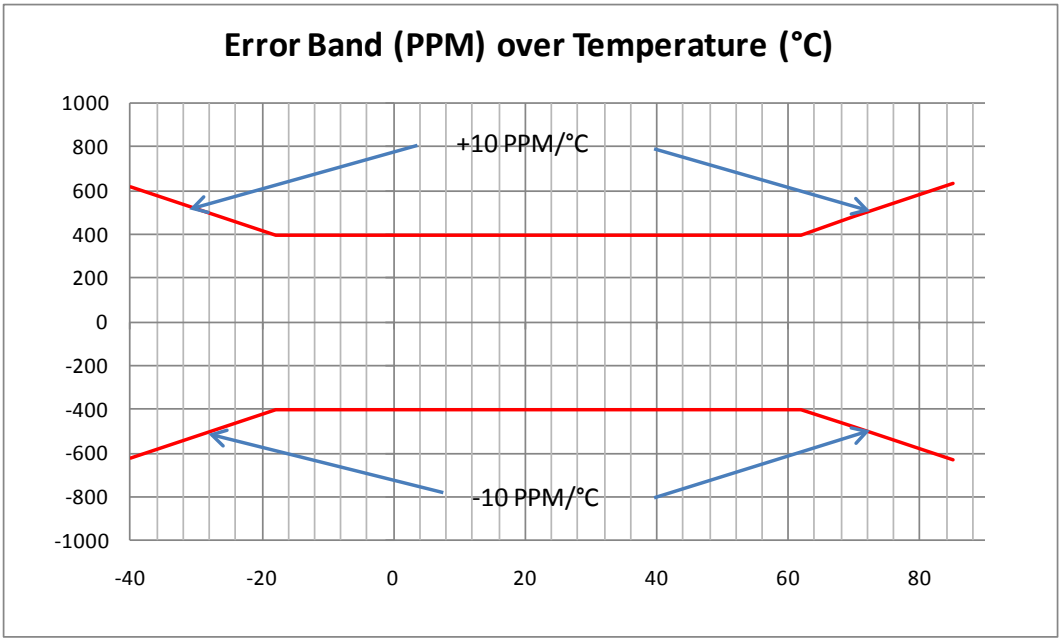

Figure 3: Error Band for VREF

Measuring Temperature

Teridian Metering ICs of the 71M651x, 71M652x, and 71M653x families do not measure absolute temperature. Instead, they measure the deviation (*TEMP_X*) from a standard, or calibration temperature:

The formula for *TEMP_X* is:

$$TEMP\_X = -DEGSCALE * 2^{-22} * (TEMP\_RAW\_X - TEMP\_NOM)$$

TEMP_X is measured in 0.1°C. To obtain the temperature in °C, we have to scale by 10 and ad the calibration temperature:

$$T = -DEGSCALE * 2^{-22} * (TEMP\_RAW\_X - TEMP\_NOM)/10 + 22°C$$

The Internal Temperature-Compensation Mechanism

The CE code used in the TERIDIAN Metering ICs allows the gain for voltage and current signals to be adjusted based on linear and quadratic coefficients, as shown in Figure 3. The non-calibrated gain, as controlled by *GAIN_ADJ*, is normally 2^{14} = 16,384. If neither temperature compensation nor calibration are performed, *GAIN_ADJ* remains at that value, and the CE will apply equal gain at all temperatures.

When calibration is performed, the gain for each channel is adjusted slightly (using the CE variables *CAL_VA*, *CAL_IA* and so on), depending on the error caused by the passive components (usually ±1% to ±3%). Temperature compensation will change the calibrated or non-calibrated overall gain for all channels determined by *GAIN_ADJ* depending on the chip temperature.

Note that *GAIN_ADJ* works on all channels, thus a change of 0.5% of *GAIN_ADJ* will affect both the voltage and current channels, thus causing a 1.0% change on energy measurements. Ideally, *GAIN_ADJ* mimics the characteristics of the reference voltage over temperature: For example, if VREF were 99.8% of its nominal value at +85°C, both voltage and current readings would be roughly 100.2% of their true values, and the energy would

be measured at 100.4%. With good compensation however, *GAIN_ADJ* is set to 99.8% (16,351) causing both voltage and current signals to be scaled to 100%.

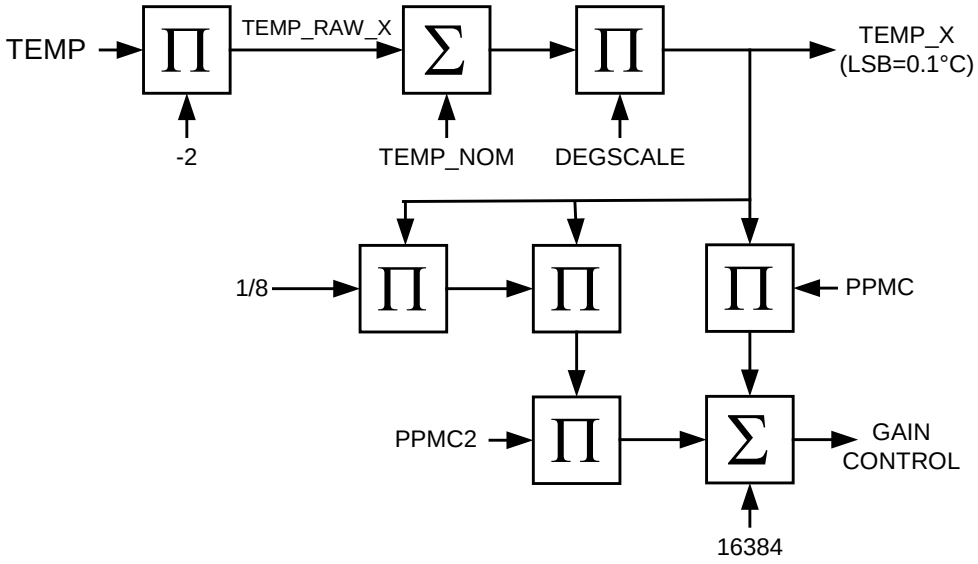

Figure 4: Simplified Temperature Compensation Flow Diagram

Using Figure 3, we can examine how the temperature compensation works: The temperature summing block (symbol Σ) subtracts the actual substrate temperature (*TEMP_RAW*, which is the *TEMP* reading from the CE multiplied by 2) from the standard temperature reading at room temperature (*TEMP_NOM*). The compensation is always relative to nominal temperature, i.e. if *TEMP_RAW* equals *TEMP_NOM*, no compensation is performed.

In the Demo Boards, the values for the temperature settings and readings can easily be obtained by using the serial interface commands of the Demo Code.

Table 1 shows the location of the temperature-related data and typical values.

The output of the summing block is multiplied (symbol Π) with the *DEGSCALE* constant (and then divided by 2^{14}), yielding the temperature difference *TEMP_X*, measured in 0.1°C. The exact formula for *TEMP_X* is:

$$TEMP\_X = -DEGSCALE * 2^{-22} * (TEMP\_RAW\_X - TEMP\_NOM)$$

In another branch of the flow diagram, the temperature difference is multiplied with *PPMC1* and then fed into the summing block that controls *GAIN_ADJ*. The third branch multiplies the temperature difference with a fraction of itself, basically yielding a quadratic term of the temperature difference. The result is multiplied with *PPMC2* and fed into the same summing block as the previous branch. The summing block has a third constant input, namely $2^{14} + 1$, which causes it to output the default value of 16,384, if *PPMC1* and *PPMC2* are zero, or if the temperature difference is zero.

Note that Figure 3 omits the scaling multipliers needed in this digital application that help keeping the signals from overflowing or losing accuracy due to rounding. Thus, no direct calculations can be derived from this diagram.

Name	Location	Address (hex)	Typical Value 6513 (decimal)	Typical Value 6511 (decimal)	Comment
TEMP	CE	0x06	427230	1000840	At room temperature
TEMP_RAW	CE	0x54	854460	2001680	At room temperature (= 2 x *TEMP*)
TEMP_NOM	CE	0x11	0	0	The value is 0 for an uncompensated part. The *TEMP_RAW* reading at calibration temperature should be entered in this memory location.
DEGSCALE	CE	0x30	22721	9585	Constant – should not be changed
TEMP_X	CE	0x40	-2	-2	For this reading, the chip temperature is 0.2° higher than *TEMP_NOM*
TRIMM[2:0]	**DIO**	0x20FD=4	8	8	Read value at 0x20FF
TRIMBGA	**DIO**	0x20FD=5	-1	-1	Read value at 0x20FF
TRIMBGB	**DIO**	0x20FD=6	-21	-21	Read value at 0x20FF
PPMC1	CE	0x39	-80	-80	0 for uncompensated part
PPMC2	CE	0x3A	-546	-546	0 for uncompensated part
EXT_TEMP	CE	0x38	0	0	0 for CE-internal temperature compensation, 15 for temperature compensation by the MPU using *GAIN_ADJ*.
GAIN_ADJ	CE	0x2E	16385	16385	This variable scales all voltage and current inputs. 16384 provides unity gain. Controlled by the CE or by the MPU, depending on the selection of *EXT_TEMP*.

Table 3: Memory Locations for Temperature-Related Data

The exact formula for *GAIN_ADJ* is:

$$GAIN\_ADJ = 16385 + \frac{TEMP\_X \cdot PPMC}{2^{14}} + \frac{TEMP\_X^2 \cdot PPMC2}{2^{23}}$$

In the Demo Code, this formula is calculated in several steps, using factorization to save memory space:

$$GAIN\_ADJ = 16385 + \frac{TEMP\_X \cdot}{2^{14}}\left(PPMC1 + \frac{TEMP\_X \cdot PPMC2}{2^{9}} \right)$$

The control of *GAIN_ADJ* will compensate the temperature characteristic of the 71M6511/6511H or 71M6513/6513H IC if the following conditions are met:

- The gain over temperature can be expressed with a linear and quadratic term with sufficient accuracy.
- The calibration coefficients *PPMC1* and *PPMC2* are chosen wisely, i.e. they implement the temperature characteristic of the 71M6511H or 71M6513H IC.

In order to explain the underlying philosophy of the compensation via gain control, let us assume that a temperature effect causes the reference voltage to decrease with increasing temperature. Lower reference voltage means that the chip generates higher outputs since all signals are scaled relative o the reference voltage. Thus, the temperature compensation adjusts the overall gain down by the exact factor that the reference decreases.

Due to the physical laws governing semiconductors, the characteristics of the bandgap reference over temperature follow the linear and quadratic representation using TC1 and TC2 closely. As the demo code

calculates the best coefficients for *PPMC1* and *PPMC2* automatically, very accurate temperature compensation can be implemented with the 71M6511/6511H or 71M6513/6513H ICs.

Location of Temperature-Related Data in the 71M6511/6511H and 71M6513/6513H ICs

The temperature coefficients TC1 and TC2 are coded during production test in the fuses *TRIMM[2:0], TRIMBGA,* and *TRIMBGB.* These fuses can be read by first writing either 4, 5 or 6 to *TRIMSEL* (0x20FD) and then reading the value of *TRIM* (0x20FF). If manual access is required to the fuses, this can be done using the following commands of the serial interface of the demo code:

```
>RI20FD=4
>RI20FF?
```

9 (*TRIMM[2:0]*) – 3 bits from this value are used, the range is from –4 to +3, thus *TRIMM*[2:0] = 1

```
>RI20FD=5
>RI20FF?
```

19 (*TRIMBGA*) – the range is from –128 to +127

```
>RI20FD=6
>RI20FF?
```

-28 (*TRIMBGB*) – the range is from –128 to +127

TEMP_NOM is accessible through address 11 (hex) of the CE data:

```
>]11?
```

854200 – the range is from +700,000 to +900,000 for the 71M6513, and around 2,000,000 for the 71M6511 (see Table 2).

The temperature compensation coefficients are located at the following addresses:

- *PPMC1* = 0x39 in the CE data space
- *PPMC2* = 0x3A in the CE data space

The coefficients can be manually read or written via the CE read/write commands of the serial command interface. The following command reads the contents of the *PPMC1* register:

```
>]39?
>0
```

The following command writes the decimal value of 23 into the *PPMC1* register:

```
>]39=+23
```

Locations for temperature-related data for the 71M652x, 71M653x, and 71M654x ICs can be found in their respective data sheets and Demo Board User Manuals (DBUMs).

Differentiating between 71M6511/71M6513 and 71M6511H/71M6513H

For the Demo Kits, the same Demo Code (firmware) is used for the H and non-H parts. The only difference in operation is that once an H-part is identified, temperature compensation is enabled based on the values stored in the fuses. The value of the register *TRIMGB* determines whether an H or non-H part is used:

If (*TRIMBGB* = 0) then the IC is a non-H part

else the IC is an H part;

Determining *PPMC1*/*PPMC2* for the 71M6511 and 71M6513

Before the CE can perform temperature compensation it needs to know the *PPMC1* and *PPMC2* coefficients that it has to apply to the compensation scheme shown in Figure 3.

If *TRIMBGB* is equal to zero, then the part is not an H part. Once *TEMP_NOM* is entered, *PPMC1* and *PPMC2* are set by the Demo Code to the nominal values derived from TC1 = +7µV/C and TC2 = -0.341µV/C^2.

It should be noted that no boundary check is performed for *TEMP_NOM* by the Demo Code. Thus, if a grossly unrealistic value is entered, unpredictable behavior of the temperature compensation will be observed.

In average, the part will expose a temperature dependency similar to the one shown in Figure 1. By examining the values in Figure 1 it can be determined that the reference voltage is off by –90µV at the lower temperature limit and –150µV at the higher temperature limit.

TC1 and TC2 are given in µV/°C, i.e. voltage deviations per change in temperature. *PPMC1* and *PPMC2* are relative deviations, i.e. with respect to the voltage reference (VREF). Since VREF = 1.195V, the relative deviations are scaled by 1/1.195 with respect to TC1 and TC2. In addition, *PPMC1* and *PPMC2* are scaled to match the quantities internally used by the CE. This determines the factors 22.463 and 1150.1 used to translate TC1 and TC2 to *PPMC1* and *PPMC2*.

The demo code uses the following settings for *PPMC1* and *PPMC2*:

PPMC1 = 22.463 x 7.0 = 157

PPMC2 = 1150.1 x -0.341 = -391

These are to be considered standard settings that apply well to the average of shipped 71M6511 or 71M6513 units. Temperature characteristics of individual units may differ from this. Thus, the temperature compensation of the 0.5% ICs cannot be as accurate as the compensation for the 71M6511H, 71M6513H, 71M6533H, or 71M6534H ICs (“H-parts”).

Meter Demo Codes may use slightly different default values for *PPMC1* and *PPMC2*. The *PPMC1* value for some Demo Codes had been derived from an outdated value for TC1 (6.68 µV/°C) rather than from the rounded value published in recent data sheets. In practical terms, this does not make a significant difference.

When using the TERIDIAN Demo Code, the only step required by the user is to read the value of *TEMP_RAW* at calibration temperature and to enter this value into the *TEMP_NOM* register. All other operations are performed automatically by the Demo Code. It should be noted that *TEMP_NOM*, along with the meter calibration coefficients at CE locations 0x08 through 0x10 (voltage, current and phase adjustment coefficients for a 3-phase meter), has to be stored into EEPROM memory after the calibration is done. In the 71M651x Demo Boards, this can be easily achieved by issuing the `]CLS` command via the serial interface.

Determining *PPMC1*/*PPMC2* for the 71M6511H and 71M6513H

If *TRIMGB* is **not** equal to zero, the device is an H part. The Demo Code will not apply temperature compensation if *TEMP_NOM* equals zero (default). Once, the user has entered *TEMP_NOM*, *PPMC1* and *PPMC2* the Demo Code will automatically calculate and enter *PPMC1* and *PPMC2* into the proper registers.

PPMC1 and *PPMC2* can still be manually obtained from the fuse values and *TEMP_NOM*. Since the values for *TEMP_NOM* are different between the 71M6513H and the 71M6511H (due to the differences in ADC resolution), individual calculations have to be applied for each IC as follows:

71M6511H:

$$a = \frac{\frac{TEMP\_NOM}{4.74074} - 500 \cdot TRIMBGA - 370{,}000}{900}$$

b = 0.1 * *TRIMBGB* - 0.14 * (*TRIMM[2:0]* + 0.5)

TC1 = b * (33 – 0.28a) + 0.33a + 7.9

TC2 = b * (0.02 – 0.0002a) – 0.46

PPMC1 = 22.463 * TC1

PPMC2 = 1150.1 * TC2

71M6513H:

$$a = \frac{\frac{TEMP\_NOM}{2} - 500 \cdot TRIMBGA - 370{,}000}{900}$$

b = 0.1 * *TRIMBGB* - 0.14 * (*TRIMM[2:0]* + 0.5)

TC1 = b * (33 – 0.28a) + 0.33a + 7.9

TC2 = b * (0.02 – 0.0002a) – 0.46

PPMC1 = 22.463 * TC1

PPMC2 = 1150.1 * TC2

Naturally, the calculated values for *PPMC1* and *PPMC2* will vary form chip to chip.

Measurement Results for Temperature-Compensated Meters

Several 71M6513H ICs were tested in both uncompensated and compensated modes. The improvement in performance when using temperature compensation is significant, as shown in Figure 4.

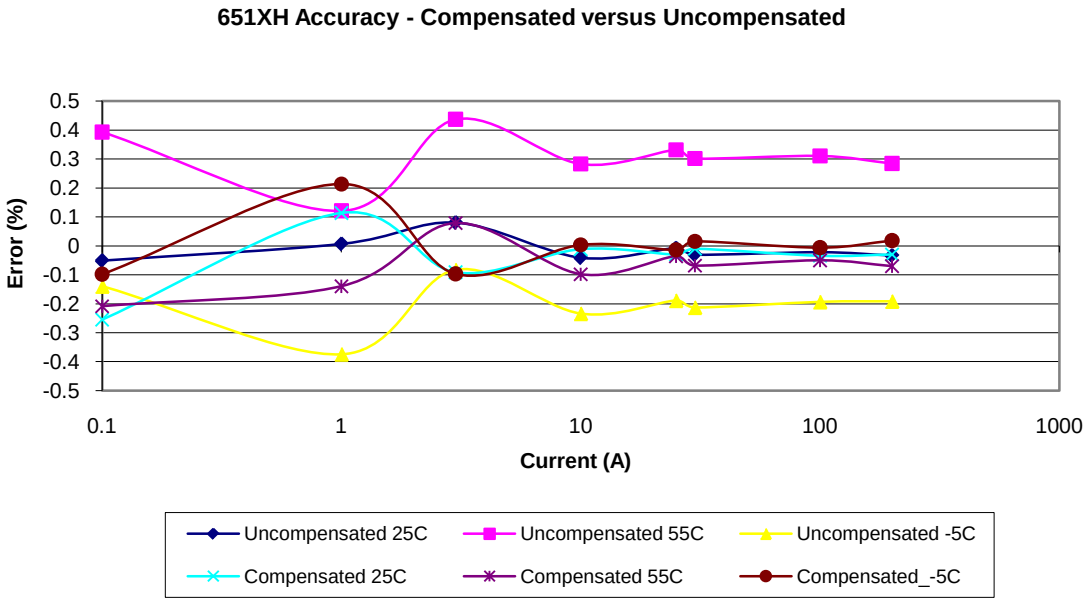

Figure 5: Performance with and without Temperature Compensation

The numbers for Figure 4 were obtained in laboratory tests of a regular Demo Board. The 71M6511H IC was exposed to thermal stream temperature cycling while the rest of the circuitry was reasonably isolated from the applied temperature, using a foam barrier. The current transformers type CR8459-200-N (manufacturer CR Magnetics) were mounted underneath the Demo Board (at about 1" distance from the PCB surface) and thus not affected by the thermal stream. The resistors forming the voltage dividers were 0805 SMT type film resistors with 0.1% and 0.5% tolerance (type RR1220P and RR0816P by manufacturer SUSUMU) with ±25PPM/°C temperature coefficient, located on the bottom side of the PCB at ½" to 2" distance from the 71M6511H IC. The Demo Board was powered externally through a wall-mount 5VDC power supply.

Temperature Effects on a Meter System – External Temperature Compensation

In a realistic meter, the 71M6511H or 71M6513H IC is not the only component contributing to temperature dependency. In fact, a whole range of components will exhibit slight or even pronounced temperature effects. Examples for these components are:

- Current transformers
- Resistor dividers
- Power sources
- Capacitors used for filtering

If all system components have their own temperature dependency f_n (T), the overall temperature function will be:

(1) $f(T) = f_1(T) * f_2(T) * \ldots f_n(T)$

Each temperature function can be expressed as a polynomial as follows:

(2) $f_n(T) = a + bT + cT^2 + dT^3 + \ldots + nT^m$

If the coefficients d through n for the polynomial representing each f_n are insignificantly small, all polynomials can be simplified to first and second order terms. If this is the case, the overall temperature function itself will be of only first and second order and can then be expressed as:

(3) $f(T) = a' + b'T + c'T^2$

Temperature compensation of a function given by (3) is possible using the second-order gain control built into the CE code of the 71M6511/6511H or 71M6513/6513H ICs, if the following conditions are met:

- A temperature equilibrium exists inside the meter housing, i.e. each component has moved from the transient state to the stabilized state.
- There are no hysteresis effects, i.e. components behave the same way at the same temperature, regardless whether they get to this temperature by moving up from a lower temperature or by moving down from a higher temperature.
- The over-all temperature function can be described with sufficient accuracy with only linear and quadratic terms.
- The over-all temperature function is repeatable, i.e. no other factors than temperature affect the measurements significantly. Other factors could be time (components aging), signal range or history (Hysteresis, see above) to name just a few.
- The meter system output can be observed at various temperatures in order to capture the over-all temperature function.

Since the output of the on-chip temperature sensor is accessible to the MPU, temperature-compensation mechanisms beyond the capabilities implemented in the CE are entirely possible. For example, a metering system with an overall temperature function of

(2) $f_n(T) = a + bT + cT^2 + dT^3$

can be modeled and compensated by the MPU using the *GAIN_ADJ* register while *EXT_TEMP* is set to 15.

Compensating for Temperature Effects on the RTC

Many meters, e.g. TOU meters, have internal controls that depend on the exact time of day. Since the RTC accuracy directly depends on the accuracy of the crystal oscillator used for the 71M651x ICs, uncompensated RTC accuracy may not be sufficient, particularly when significant changes in environment temperature occur or when high accuracy over long time must be maintained.

The flexibility provided by the MPU allows for compensation of the RTC using the substrate temperature. To achieve this, the crystal has to be characterized over temperature, and the three coefficients *Y_CAL*, *Y_CALC*, and *Y_CAL_C2* have to be calculated. Provided the IC substrate temperatures tracks the crystal temperature the coefficients can be used in the MPU firmware to trigger occasional corrections of the RTC seconds count, using the *RTC_DEC_SEC* or *RTC_INC_SEC* registers in I/O RAM.

It is not recommended to measure crystal frequency directly due to the error introduced by the measurement probes. A practical method to measure the crystal frequency (when installed on the PCB with the 71M6511 or 71M6513) is to have a DIO pin toggle every second, based on the RTC interrupt, with all other interrupts disabled. When this signal is measured with a precision timer, the crystal frequency can be obtained from the measured time period t (in µs):

$$f = 32768 \frac{10^6 \mu s}{t}$$

Example: Let us assume a crystal characterized by the measurements shown in Table 3.

Deviation from Nominal Temperature [°C]	Frequency Deviation [Hz]	Deviation from Nominal Frequency [PPM]
-43	-1.8	-55
-35	-1.15	-35
-25	-0.49	-15
0	0.16	5
25	0.49	15
35	-1.15	35
43	-1.8	55

Table 4: Frequency over Temperature

The values show that even at nominal temperature (the temperature at which the chip was calibrated for energy), the deviation from the ideal crystal frequency is 0.16 Hz or 5 PPM, resulting in about 0.4 second inaccuracy per day.

At temperatures deviating from nominal, the errors become increasingly larger, as Figure 5 shows. For commercially available 32-kHz crystals, the constant and quadratic components are the dominating effects.

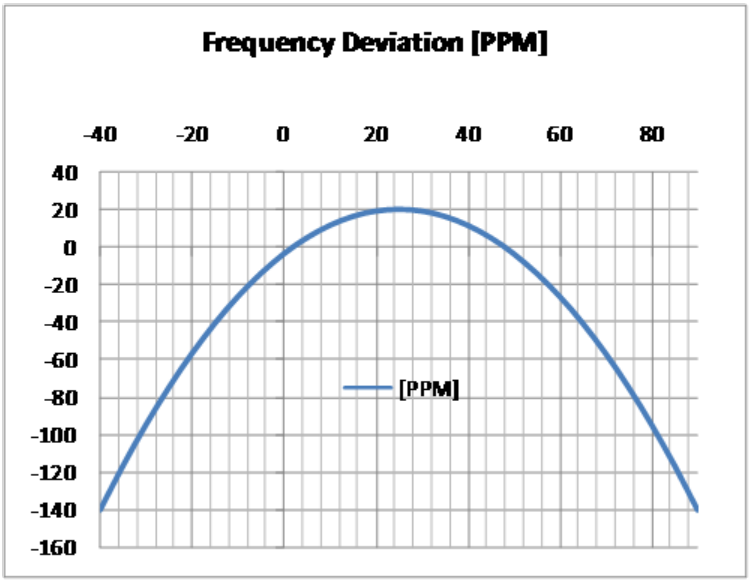

Figure 6: Frequency Deviation over Temperature for a Typical Crystal

The recommended method for correcting the temperature characteristics of the crystal is to obtain coefficients from the values in Table 3 by curve-fitting the PPM deviations. A fairly close curve fit is achieved with the coefficients a = 5, b = 0, and c = –0.0325665 (see Figure 6).

$$f = f_{nom} * (1 + a/10^6 + T * b/10^6 + T2* c/10^6)$$

When applying the inverted coefficients a'=-5, b'=0, and c'=0.0325665, an inverted curve (see Figure 6) will result that effectively neutralizes the original crystal characteristics.

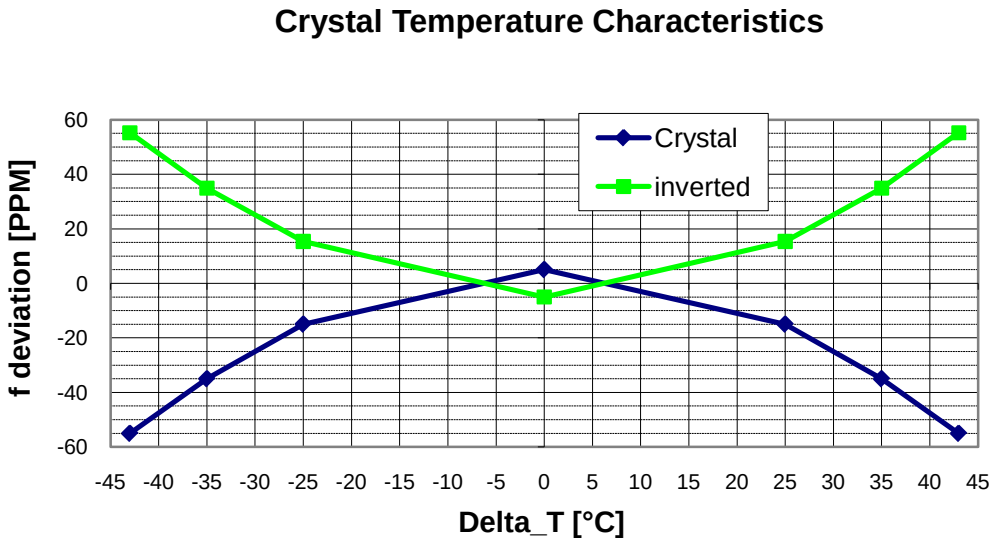

Figure 7: Crystal Compensation

The MPU Demo Code supplied with the TERIDIAN Demo Kits has a direct interface for these coefficients and it directly controls the *RTC_DEC_SEC* or *RTC_INC_SEC* registers. For the Demo Code, the coefficients have to be entered in the form:

$$CORRECTION(ppm) = \frac{Y\_CAL}{10} + T \cdot \frac{Y\_CALC}{100} + T^2 \cdot \frac{Y\_CALC2}{1000}$$

Note that the coefficients are scaled by 10, 100, and 1000 to provide more resolution. For our example case, the coefficients would then become (after rounding):

Y_CAL = 50, *Y_CALC* = 0, *Y_CALC2* = 326

After the proper coefficients are entered in the MPU locations *Y_CAL*, *Y_CALC*, and *Y_CALC2* the Demo Code will correct the RTC, as illustrated in Figure 7 (the red dotted line shows the ideal RTC time). In this example, the RTC is advanced by one second once its delay compared to ideal time reaches 0.5 seconds.

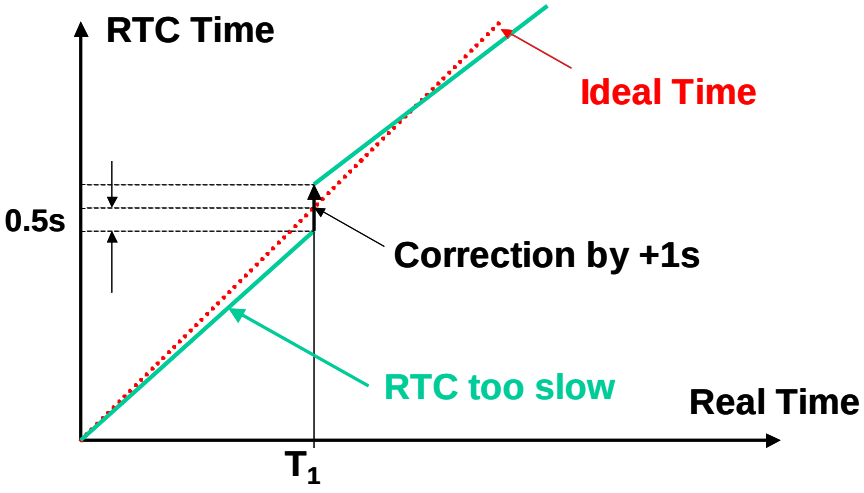

Figure 8: RTC Compensation

A common technique to achieve good RTC accuracy is to use the mains frequency for timekeeping purposes and to switch to the RTC only in the cases where the mains signal is not available. For this purpose, the CE provides a count of the zero crossings detected for the selected line voltage in the *MAIN_EDGE_X* address. This count is equivalent to twice the line frequency, and can be used to synchronize and/or correct the RTC.

Application Note AN_6521_035 describes advanced concepts for temperature compensation of the RTC. Even though this document was written for the 71M6521, its concepts can be applied to the 71M651x family.

The 71M653x family of TERIDIAN Metering ICs offer more advanced techniques for setting and correcting the RTC crystal frequency. See the data sheets for the 71M653x ICs for details on proper temperature compensation.

Revision History

Revision	Date	Description
Rev. 2.6	12/11/2007	Improved description of reference voltage over temperature. Added Figure 7. Replaced values in Table 3 and Figure 5 with those from a real crystal.
Rev. 2.7	4/17/2009	Extended description to 6521, 6531, 6533, and 6534 metering ICs. Added text describing the ideal behavior of *GAIN_ADJ* over temperature. Added reference to data sheets of 71M653x parts. Corrected calculated value for *PPMC1* based on TC1 = 7 µV/°C. Updated Figure 5.
Rev. 2.8	5/20/2010	Improved Figure 1. Added Table 1 and Figure 3. Updated all numbers for PPPM/°C and achievable accuracy throughout the document.

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