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73M1x66B Worldwide Design Guide

APPLICATION NOTE

AN_1x66_004 **March 2011**

Introduction

This application note provides guidelines and recommendations for the configuration and use of the 73M1866B and 73M1966B in preparing for worldwide homologation. These integrated circuits will be collectively referred to as the 73M1x66B in this document.

Designing for worldwide homologation is an extensive subject. This application note provides information for initial consideration. It is the intention of Teridian to expand and enhance this application note on a regular basis. For the latest version of this document, contact any sales office of Teridian Semiconductor Corporation.

The 73M1x66B MircoDAA™ provides the user with highly integrated, globally compliant, silicon DAA for ultra low-cost voice band data and fax applications. The global-compliance parameters, which provide the necessary functionality and the protection required for worldwide homologation, are programmable.

This application note describes the following built-in features for global configurations:

- AC Termination Impedance
- DC Mask Control
- Ring Detector Threshold

The final section gives an example of the 73M1x66B MicroDAA initialization sequence.

For additional information on the registers and bits, refer to the appropriate data sheet.

AC Termination Impedance

The AC termination impedance is set by selecting the ACZ bit settings in Register 0x16[3:0]. Table 1 provides the AC termination impedance settings for a number of countries.

There are several different AC termination impedances that are used worldwide. Typical AC termination requirements are either 600 Ω resistive or a specific complex impedance (resistor/capacitor network) termination such as TBR-21 or Australian. See Table 2 for a complete list of terminations supported by the 73M1x66.

The match of a device's termination impedance to the line impedance determines the return loss figure. With the following settings, a single design can be used worldwide without the need for hardware changes for specific countries.

Table 1: Worldwide AC Impedance Setting

Country	AC term	ACZ(3:0)	Country	AC term	ACZ(3:0)
Argentina	600	0000	Leichtenstein[2]	Complex	0010
Australia	Complex	0011	Lithuania[1]	Complex	0010
Austria[1]	Complex	0010	Luxembourg[1]	Complex	0010
Bahrain	600	0000	Macao	600	0000
Belgium[1]	Complex	0010	Malaysia	600	0000
Bolivia	600	0000	Malta[1]	Complex	0010
Brazil	600	0000	Mexico	600	0000
Bulgaria[1]	Complex	0010	Morocco	600	0000
Canada	600	0000	Netherlands[1]	Complex	0010
Chile	600	0000	New Zealand[3]	Complex	0100
China[3]	Complex	1110	Nigeria	600	0000
Columbia	600	0000	Norway[2]	Complex	0010
Croatia	Complex	0010	Oman	600	0000
Cyprus[1]	Complex	0010	Pakistan	600	0000
Czech Rep[1]	Complex	0010	Peru	600	0000
Denmark[1]	Complex	0010	Philippines	600	0000
Ecuador	600	0000	Poland[1]	Complex	0010
Egypt	600	0000	Portugal[1]	Complex	0010
El Salvador	600	0000	Romania[1]	Complex	0010
Estonia[1]	Complex	0010	Russia	600	0000
Finland[1]	Complex	0010	Saudi Arabia	600	0000
France[1]	Complex	0010	Singapore	600	0000
Germany[1]	Complex	0010	Slovakia[1]	Complex	0010
Greece[1]	Complex	0010	Slovenia[1]	Complex	0010
Guam	600	0000	S. Africa[3]	Complex	0011
Hong Kong	600	0000	S. Korea	600	0000
Hungary[1]	Complex	0010	Spain[1]	Complex	0010
Iceland[2]	Complex	0010	Sweden[1]	Complex	0010
India	600	0000	Switzerland[2]	Complex	0010

Country	AC term	ACZ(3:0)	Country	AC term	ACZ(3:0)
Indonesia	600	0000	Syria	600	0000
Ireland[1]	Complex	0010	Taiwan	600	0000
Israel	600	0000	TBR 21	Complex	0010
Italy[1]	Complex	0010	Thailand	600	0000
Japan	600	0000	Turkey	600	0000
Jordan	600	0000	UAE	600	0000
Kazakhstan	600	0000	UK[1]	Complex	0010
Kuwait	600	0000	Ukraine	600	0000
Latvia[1]	Complex	0010	USA	600	0000
Lebanon	600	0000	Yemen	600	0000

[1] These countries are members of the European Union, where there are no longer any regulatory requirements for AC impedance. The suggested setting complies with ETSI ES 203 021-2. Other settings can be used if desired.

[2] These countries are members of the European Free Trade Association. Their regulations generally follow the European Union model. The suggested setting complies with ETSI ES 203 021-2.

[3] These countries can use the suggested complex setting for voice or data products.

Table 2 lists the termination impedances supported by the 73M1x66.

Table 2: Termination Impedances Supported by the 73M1x66

ACZ(3:0)	Impedance	Example Countries
0000	600 Ω	USA, Japan, China (data applications)
0001	900 Ω	
0010	270 Ω + 750 Ω || 150 nF 275 Ω + 780 Ω || 150 nF	TBR-21 UK, France Spain
0011	220 Ω + 820 Ω || 120 nF 220 Ω + 820 Ω || 115 nF	Australia Germany[1]
0100	370 Ω + 620 Ω || 310 nF	New Zealand
0101	320 Ω + 1050 Ω || 230 nF	
0110	370 Ω + 820 Ω || 110 nF	
0111	275 Ω + 780 Ω || 115 nF	
1000	120 Ω + 820 Ω || 110 nF	
1001	350 Ω + 1000 Ω || 210 nF	
1010	200 Ω + 680 Ω || 100 nF	China (voice applications)
1011	600 Ω + 2.16 µF	
1100	900 Ω + 1 µF	
1101	900 Ω + 2.16 µF	
1110	220 Ω + 400 Ω || 70 nF	China
1111	270 Ω + 600 Ω || 150 nF	Global Impedance

[1] Pre-ETSI termination

DC Mask Control

As each country regulates the AC termination, there are requirements for specific DC termination in some countries. The DC mask control is set by selecting the DCIV bit settings in Register 0x13[7:6]. Table 3 provides the recommended DC mask settings for specific countries.

The ILM bit in Register 0x13[5] controls the current limit mode. This was required for operation in France and former French colonies, but is no longer a requirement. Some applications may still require this feature for compatibility with legacy systems.

The DC termination requirements can be measured by checking the DC mask compliances. See Figure 1 through Figure 3 for measured results.

Table 1: Worldwide DC Mask Settings

Country	DCIV(1:0)	Country	DCIV(1:0)	Country	DCIV(1:0)
Argentina	10	Hungary	10	Pakistan	10
Australia	11	Iceland	10	Peru	10
Austria	10	India	10	Philippines	10
Bahrain	10	Indonesia	10	Poland	10
Belgium	10	Ireland	10	Portugal	10
Bolivia	10	Israel	10	Romania	10
Brazil	10	Italy	10	Russia	10
Bulgaria	10	Japan	00	Saudi Arabia	10
Canada	10	Jordan	10	Singapore	10
Chile	10	Kazakhstan	10	Slovakia	10
China	10	Kuwait	10	Slovenia	10
Columbia	10	Latvia	10	S. Africa	10
Croatia	10	Lebanon	10	S. Korea	10
Cyprus	10	Liechtenstein	10	Spain	10
Czech Rep	10	Lithuania	10	Sweden	10
Denmark	10	Luxembourg	10	Switzerland	10
Ecuador	10	Macao	10	Syria	10
Egypt	10	Malaysia	10	Taiwan	10
El Salvador	10	Malta	10	TBR 21	10
Estonia	10	Mexico	10	Thailand	10
Finland	10	Morocco	10	Turkey	10
France[1]	10[1]	Netherlands	10	UAE	10
Germany	10	New Zealand	10	UK	10
Greece	10	Nigeria	10	Ukraine	00
Guam	10	Norway	10	USA	10
Hong Kong	10	Oman	10	Yemen	10

[1] The setting for France can be used with current limiting mode enabled by setting ILM bit in Register 0x13[5]. The use of current limiting is no longer a requirement for operation in France.

Figure 1 shows the DC line characteristics for the four DCVI1/DCVI0 settings.

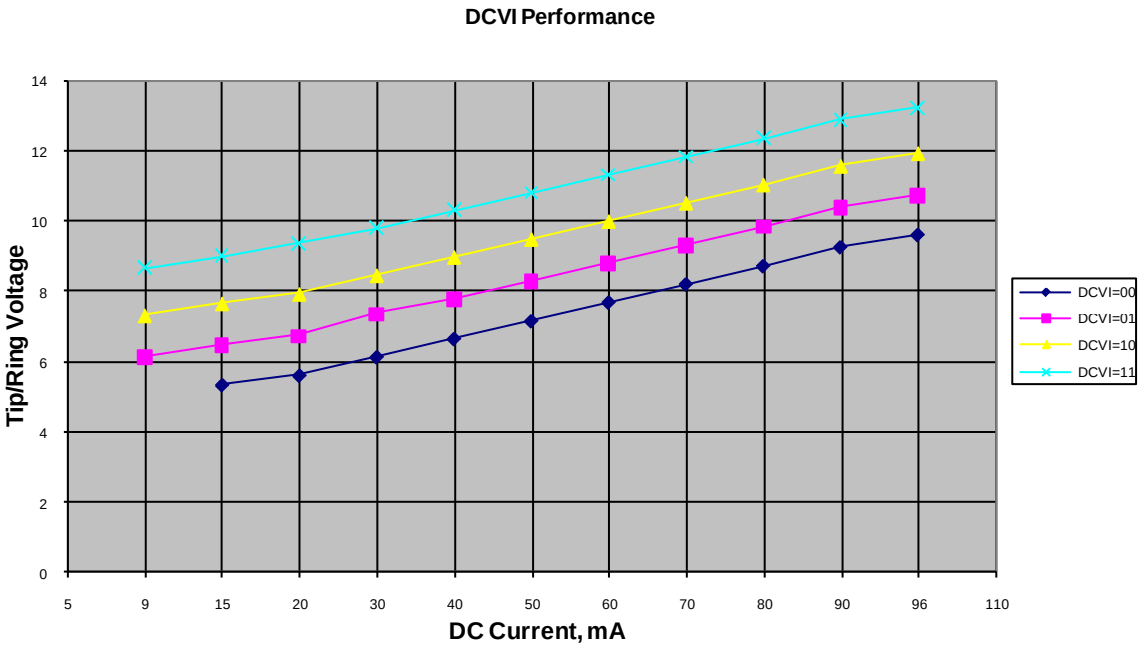

Figure 1: DC Line Characteristics with the 73M1966B DCVI[1:0] Settings

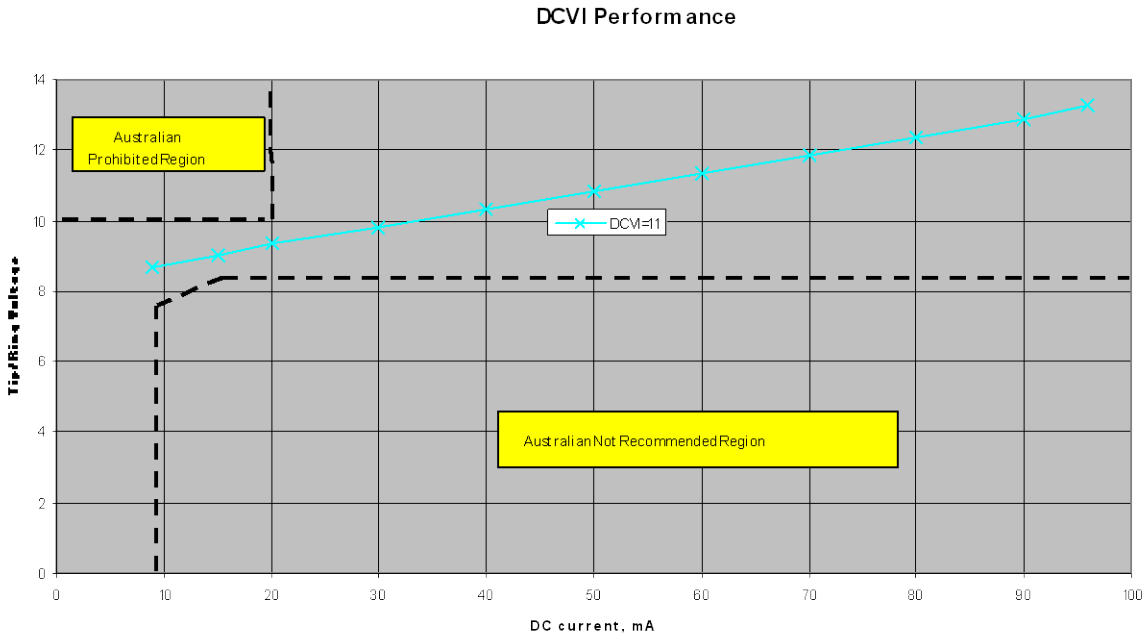

Figure 2: DCVI[1:0]=11 Setting with the Australian Hold State Template

Figure 3 shows the Seize Mode DCVI characteristics with the Australian Seize Template. The DCVI setting does not affect the DCVI characteristics in the Seize Mode.

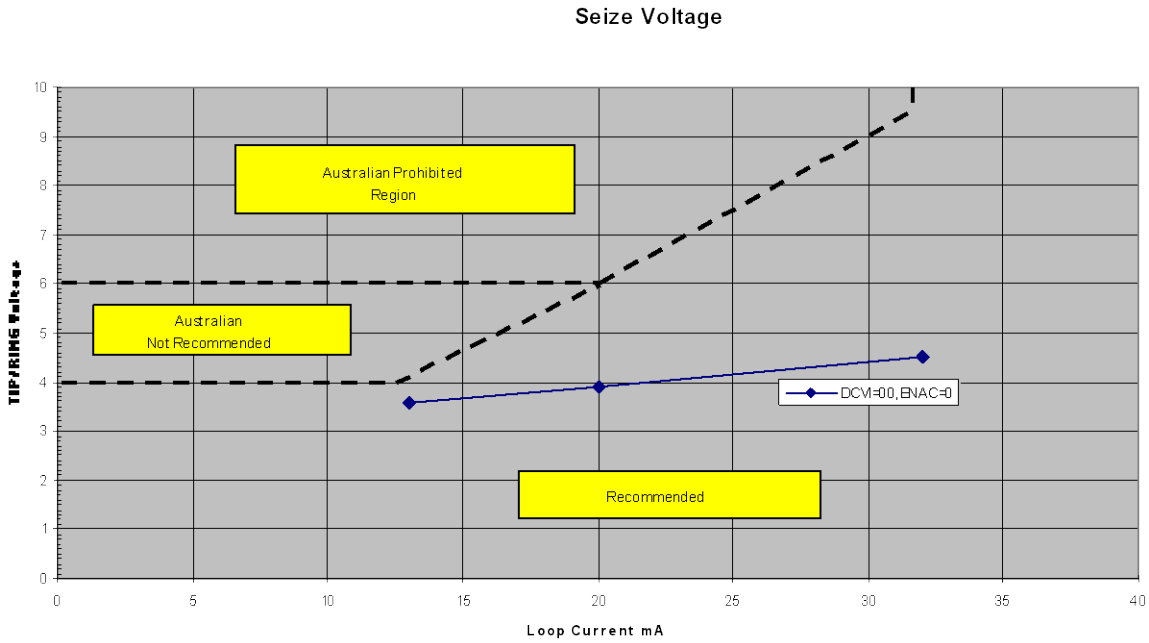

Figure 3: Seize Mode DCVI Characteristics with the Australian Seize Template

Ring Detector Threshold

The Ring Detector threshold is set by selecting the RGTH bits in Register 0x0E[1:0]. Table 4 shows the maximum and minimum ring levels and the Ring Threshold settings recommended for the 73M1x66 MicroDAA.

Ring detection is only possible if bit ENDC=0 in Register 0x12[6].

Table 1: Worldwide Ring Threshold Settings

Country	Min(V_{RMS}) To Detect	Max(V_{RMS}) Not to Detect	RGTH[1:0](V_{PK})
Austria	25	10	10 (30 V)
Belgium	25	10	10 (30 V)
Bulgaria	30	9	10 (30 V)
Cyprus	30	10	10 (30 V)
Czech Republic	25	15	10 (30 V)
Denmark	40	17	11 (45 V)
England	63	–	11 (45 V)
Finland	35	10	10 (30 V)
France	25	15	10 (30 V)
Germany	32	–	10 (30 V)
Greece	25	15	10 (30 V)
Hungary	40	12	11 (45 V)
Iceland	30	10	10 (30 V)
Ireland	25	3	10 (30 V)
Italy	26	15	10 (30 V)
Japan	24	–	10 (30 V)
Korea	24	–	10 (30 V)
Luxembourg	45	10	10 (30 V)
Norway	28	17	10 (30 V)
Netherlands	35	10	10 (30 V)
Poland	40	16	11 (45 V)
Portugal	30	12	10 (30 V)
Spain	35	–	10 (30 V)
Sweden	30	10	10 (30 V)
Switzerland	24	8	10 (30 V)
USA	45	–	11 (45 V)

Device Initialization Procedure

This section provides an example of the MicroDAA initialization sequence that includes the global configuration parameter settings.

1. Reset pulse generation by the host

The 73M1966B MicroDAA does not have an internal power on reset circuit. It is necessary for PCLK to be running before reset can occur. For proper operation, a reset signal must be asserted from the host by pulling the reset pin of 73M1906B low for a minimum of 100 ns after the power is stabilized above VDD min. The 73M1906B device will be ready to use within 100 µs after the removal of the low level from the reset pin.

2. 73M1906B Host Interface IC (HIC) Initialization

    1. After power up and reset, the Host-Side Device will sense the frequency of the incoming PCLK by comparing it to the FS frequency, which is always 8 kHz. It will then automatically adjust to the PCLK frequency so that the proper number of time slots and clocks per FS are generated. The LOKDET bit is also set (Register 0x0D[7]).
    2. Configure GPIOs as needed by selecting GPIO Data (Register 0x02), GPIO Direction (Register 0x03), GPIO Interrupt Enable (Register 0x04) and Interrupt Polarity (Register 0x05).

        ✓ GPIO pins are not available on the 20-pin 73M1966B.

    3. Enable the Analog Front End blocks by setting the ENFEH bit (Register 0x0F[7]) and make the device active by clearing the Sleep bit (Register 0x0F[5]) (these are the default settings).
    4. Program the LIC ENFEL bit in Register 0x12[04] and the ring threshold bits (register 0x0E[1:0], for ring detection. Read Register 0x0E and modify the Ring Threshold by modifying the RGTH bits (Register 0x0E[1:0]) to the desired value as shown in Table 4 and write it back to Register 0x0E. This read-modify-write procedure must be used to prevent previously set bits from being overwritten in the same register. Ring detection requires that the RGTH[1:0] bits are both non-zero. Set ENRGDT (Register 0x05[0]) to enable ring detection. For ring detection to occur, the ENDC bit (Register 0x12[6]) must be 0.

3. 73M1916 LIC (Line Interface IC) Initialization

Following the HIC Initialization and setting the ENFEH bit (Register 0x0F[70]), if the FRVCO bit (Register 0E[7], read only) is 1, this indicates that the barrier can now start powering the 73M1916 LIC. 73M1916 LIC initialization can begin after the 73M1916 LIC is fully powered up. From the activation of FRVCO, the host must wait for 100 ms for the 73M1916 LIC to be ready. To activate all the LIC functions, follow these steps:

1. Enable the Front End functional blocks by setting the ENFEL bit (Register 0x12[2]).
2. Select the appropriate DCIV and ILM settings and set the THDCEN bit (Register 0x13[4]). The DCVI characteristics should be chosen based on the country requirements shown in Table 3. ILM is not required for most applications.
3. Select the proper the AC impedance termination by setting the ACZ bits (Register 0x16[3:0]) based on the country requirements shown in Table 1. Set the ATEN bit (Register 0x16[4]) to activate the AC termination.
4. Enable transmit and receive paths by setting the TXEN and RXEN bits (Register 0x16[7:6]). For most applications the RXG bits (Register 0x14[1:0]) should be set to 10.
5. To go off hook, set bits OFH and ENDC in Register 0x12[7:6]. Optionally the ENAC bit (Register 0x12[5]) can be set at the same time, or it can be set separately to use the “seize” mode as required for Australia (Figure 3). This puts the network connection into a mode where the DC voltage is lower than what is set by the DCVI bits and is used for the first ~300 ms before the ENAC bit is set. After the ENAC bit is set, the line goes to the “hold” state and reverts to the normal DCVI mode selected by the DCVI bits (Figure 1 and Figure 2). After entering the hold state, the ENNOM bit (Register 0x12[0]) should be set to allow the operation of the line detectors (UVDT, OVDT, and OIDT) and shift the DC circuit to the low bandwidth state. At this point, the line voltage and current detectors can be enabled by setting the ENDT bit (Register 0x12[1]).

The 73M1966B is now ready for normal operation.

Related Documentation

The following 73M1x66B related documents are available from Teridian Semiconductor Corporation:

73M1866B/73M1966B Data Sheet
73M1966B Evaluation Kit User Manual
73M1866B/73M1966B Demo Board User Manual
73M1866B/73M1966B Keychain Demo Board User Manual
73M1866B/73M1966B GUI User Guide
73M1966B Layout Guidelines
73M1x22/73M1x66B Line-In-Use / Parallel Pick-Up Detection

Contact Information

For more information about Maxim products or to check the availability of the 73M1x66B, contact technical support at **www.maxim-ic.com/support**.

Revision History

Revision	Date	Description
September 2007	September 12, 2007	Preliminary version.
1.0	October 31, 2007	Added Bolivia, Turkey and Ukraine to the list of countries in Table 1 and Table 3. Made corrections to Table 1 and Table 3.
1.1	April 8, 2009	Made corrections to Table 1. Added information to Table 4.
1.2	March 30, 2011	Corrected some typos. Added the new Contact Information.