AN_1x22_018 October 2009

73M1822/73M1922 Schematic and Layout Guidelines

Introduction

This application note provides layout recommendations that should be followed when integrating the 73M1822 and 73M1922 into new designs. For the sake of brevity, the term 73M1x22 refers to both the 73M1822 and 73M1922. The 73M1x22 can receive signals with amplitudes lower than 3 mV rms, so it is imperative that the PCB layout and routing minimize noise interference, especially from AC mains, and Electromagnetic Interference (EMI) from other external sources. It is also important to design the PCB to minimize both radiated and conducted emissions from the 73M1x22 circuitry. In general, circuit performance can be attributed to careful consideration of analog signal routing and the layout of components.

This application note describes recommendations related to the following areas:

- Layout consideration for optimal performance
- Power dissipation within the line-side circuits
- Power supply considerations
- Connections to Tip and Ring (PSTN)
- Ring Detect and Caller ID path connections
- Pulse transformer considerations
- Reference schematics and layout examples
- Power dissipation and other considerations for the line-side circuits
- Special layout considerations for the 73M1822
- Exposed bottom pad on 73M1x22 QFN packages
- High voltage layout, with particular references to creepage and clearances
- EMI and EMC considerations
- Considerations for high-frequency signals
- Cost reducing the design

The 73M1922 is a chipset consisting of two devices, as shown in Figure 1. The 73M1902 is predominately digital in nature and is referred to as the Host-Side Device. The 73M1912 is located on the telephone network side (PSTN) of the isolation barrier and is referred to as the Line-Side Device. These terms are used throughout this document. The majority of recommendations discussed will be with reference to the 73M1912 Line-Side Device.

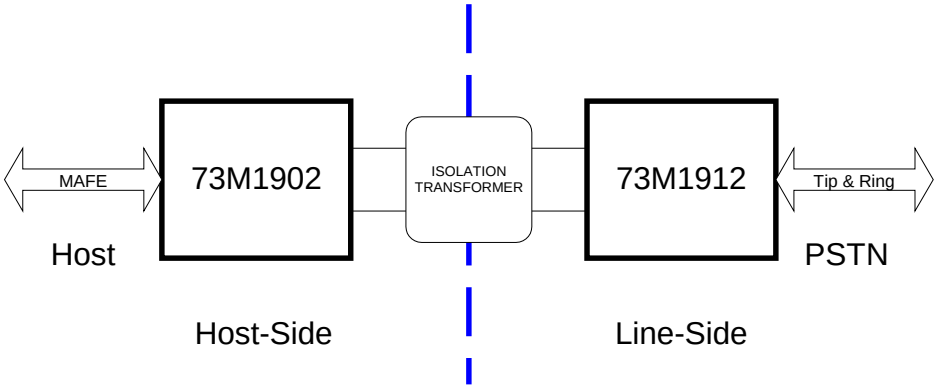

Figure 1: 73M1922 System Architecture

The 73M1822 combines these two devices in a single package to reduce the PCB space requirements. The layout guidelines for the devices are generally the same for both the 73M1922 and 73M1822 since electrically they are identical. The voltage isolation performance is the only significant difference between the two products.

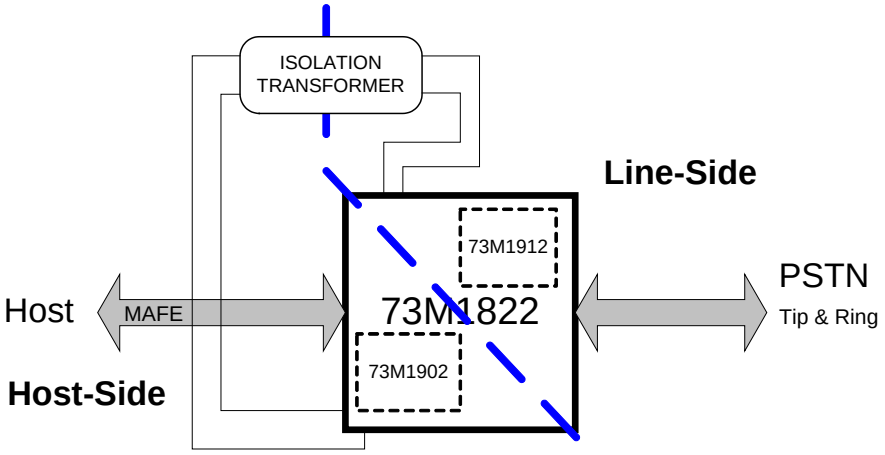

Figure 2: 73M1822 System Architecture

It is important to note that the following layout guidelines are applicable to both the 73M1822 and 73M1922. There is however a section later in the document that adds specific considerations for the 73M1822.

Layout Considerations for Optimal Performance of the MicroDAA

The following layout guidelines should be addressed **before** other signals are routed for the Line-Side circuits. The circuit traces connecting the bridge rectifier (BR1 in Figure 4 and Figure 5), the circuit connecting to the VNS pin, R5, and those that connect to the collector of Q6, should be 1 mm or larger. These traces must carry the DC loop current and transmit signals from the line-side device, and should be made wider to minimize the impedance. It is best to use a "star" grounding technique to ensure circuit stability, with each of the current paths from the AC (Q5), DC, and reference circuits connecting only to a single point near the rectifier bridge. The bypass components should also connect at this point. Any vias in these traces need to be as low impedance as possible. Multiple vias are recommended for all high current paths (or avoid vias altogether), for example, traces connecting Q6 and R5. Also keep these traces as short as possible. **Only after these circuits have been placed should the other line side circuits be routed.**

Power Dissipation for the Line-Side Circuits

Resistor R5 should be a 0805 to allow for worst-case conditions. This resistor carries the DC loop current and can dissipate nearly 100 mW. Provide adequate heat dissipation for Q6 (BCP-56). Q6 carries the DC loop current and may dissipate 600 mW under worst-case conditions. Additional metal on the collector tab PCB connection should be provided with copper on the top and bottom connected with PCB vias to stitch the two layers together.

An example of a 73M1922 board layout is illustrated in Figure 6 with the corresponding top and bottom layer routing shown in Figure 7 and Figure 8. A minimum of 0.5 square inch of copper should be used on both the top and bottom layers. In current-limit mode under worst-case conditions, over 2.4 W will be dissipated by Q6 (60 mA @ >40 V). If the current-limit mode is used, a higher-power transistor with heat sinking will be necessary. SOT223 power transistor packages cannot be used at these power levels, so an NPN transistor with a package able to dissipate at least 2.4 W and with a minimum beta of 60 (for example, the Fairchild KSD1273) must be used for Q6.

Power Supply Considerations

It is recommended that ground and power planes be used on the host-side to help minimize EMI and noise. To improve Electromagnetic Compatibility (EMC), we do not recommend the use of ground and power planes on the line-side. Line-side circuits are predominately analog, not high-speed digital, and generally do not benefit from the use of power and ground planes.

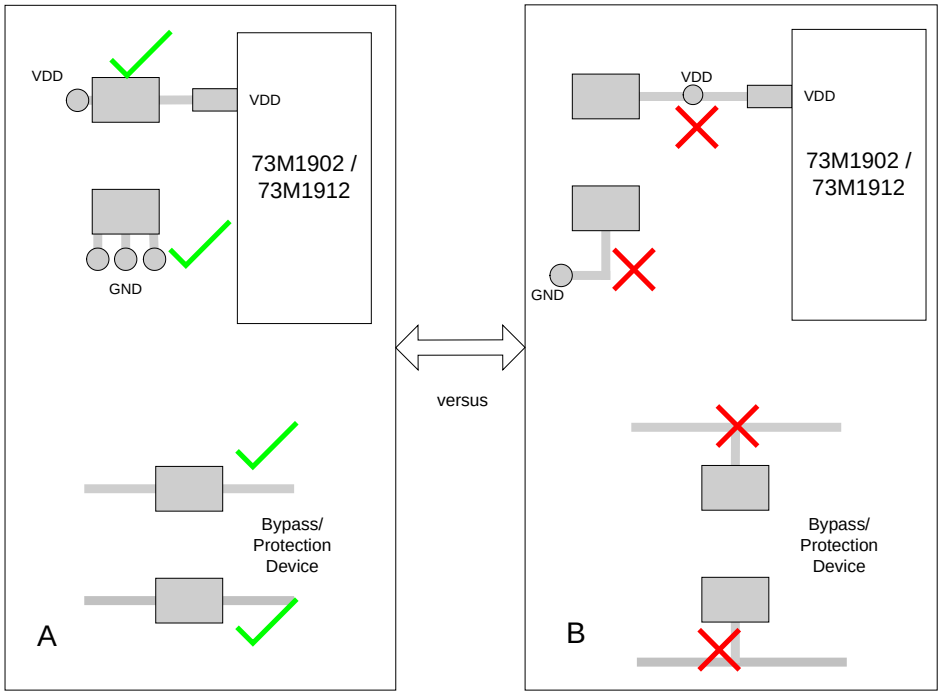

Figure 3: Layout and Routing of Power/Bypass Capacitors

Power supply considerations include the following:

- Do not use power and ground planes on the line-side circuit.
- Use power and ground planes on the host-side circuit.
- Pay special attention to the way the power and bypass capacitors are connected to the 73M1822/73M1922, as in Figure 3 A. PCB traces from the bypass capacitors to the VDD positive supply should be kept as short as possible.
- Keep all bypass capacitors close to the VDD power pins of the device. Ensure that the VDD supply is routed through the bypass capacitor pad and that the GND connection is direct to GND using several vias.
- The power and ground traces should be at least 0.5 mm.
- Power and ground traces for analog and digital supplies should be separated for best low-level receive performance. Power to digital pins and associated bypass capacitors should be kept separate from analog power and bandgap reference (VBG) bypass pins, by using separate traces.
- Use 1000 pF capacitors on power supply pins to minimize EMI and place them near the connecting pins.
- To minimize unwanted series inductance, do not use PCB vias between the 1000 pF bypass capacitors and device pins.

Connections to Tip and Ring

A current limiting device (F1 as shown in Figure 4) is a highly recommended protection component to limit turn-on transient voltage and current for GR-1089-CORE 2500 V and FCC part 68 1500 V impulse tests (this device is bypassed for some power cross tests). Some, but not all, thyristor devices (E1 as shown in Figure 4) must have an additional minimum series resistance to survive the more stringent certification tests. The higher on resistance of Plastic Positive Temperature Coefficient (PPTC) fuse devices (F1) can serve this purpose and improve product reliability compared to other current-limiting components because they automatically reset after a fault condition is removed. The cost of PPTC devices is comparable to single event slow-blow fuses designed for telecom applications. It is possible to avoid fuses altogether if the product is in a fire enclosure and is supplied with a 26 AWG or larger RJ-11 telephone cable. But if this route is chosen, the reliability, potential fire and damage to the other circuits in the enclosure should also be considered.

The ratings for the protection devices depend on a country's requirements for safety testing as well as the ringing voltage and DC source voltage. For the U.S., the requirements are more stringent that for most other countries. The UL over voltage tests require passing 600 V, 60 A tests, so the PPTC fuse must have a 600 V rating. For most other countries' applications this only needs to be 250 V. The U.S. tests require testing with a CO battery voltage of 56 V and 150 Vrms ringing, so the peak voltage is 268.8 V. This means the thyristor must not trigger on these ringing voltages, so minimum voltage the voltage protection can trigger at must be at least that voltage, meaning a 270 V or 275 V thyristor must be used since that is the next larger standard minimum breakdown voltage that is made. In countries where the DC loop and ring voltages are lower than this, a lower voltage thyristor can be used instead.

Ring Detect and Caller ID Path

The components in the input circuit to the Ring Detect and Caller ID (RGN and RGP) pins of the line-side device are used to provide attenuation to this function. The attenuation required means the RGN/RGP inputs will have a high impedance and are sensitive to noise pick-up. The high impedance-side traces to the components must be kept short. Resistors used in the ring detection circuit (R66 and R67 in Figure 4) must be a minimum of 0805 size to meet the voltage rating requirements of the line-side connections to the network. Similarly the capacitors (e.g. C1 and C3) require a voltage rating of at least 200 V to withstand the ringing and battery voltages. Any capacitors that bridge Tip and Ring need to be rated at least 275 VAC. Locate these resistors and capacitors as close as possible to the 73M1912 Line-Side Device (or the Line-Side of the 73M1822) to reduce noise pick-up and achieve the best possible performance.

As previously stated, keep all analog signal traces separate from high-speed digital circuitry and traces. The barrier interface has relatively large, high-current signals when the 73M1912 Line-Side Device is in an operational mode. Signal traces to the RGN and RGP pins need to be kept physically separated from the barrier.

Pulse Transformer Considerations

Table 1 provides a list of pulse transformers that have been tested and proven to work with the 73M1x22 device.

Table 1: Validated Transformers for Use with the 73M1x22

Company	Number	Rated Isolation	Typ. Inductance	Typ. Interwinding Capacitance
Sumida	ESMIT 4180 ESMIT 4181	6 kV peak (Dielectric 3750 Vrms min)	120 µH min 60 µH min	5 pF max.
Wurth Electronics Midcom Inc.	750110001	6 kV peak (Dielectric 3750 Vrms min)	150 µH min	Not specified
UMEC	TG-UTB01543S	6 kV peak (Dielectric 3750 Vrms min)	150 µH min	Not specified
Datatronics	PT79280	6 kV peak (Dielectric 3750 Vrms min)	60 µH min	2.5-5 pF
AAsupreme	P950003	Dielectric 2 kVrms min	60 µH min	6pF max

The best choice for a particular transformer depends upon customer needs. The customer may only be interested in cost and or required isolation. Overall performance of a pulse transformer will depend upon a few parameters. The *73M1x22 Data Sheet* specifies some limits in order to guarantee performance. These parameters include the inductance and interwinding capacitance of the transformer. Also the rated isolation of the transformer may be important.

Reference Schematics and Layout Examples

The following figures contain the reference schematics and layouts that are used with the 73M1922 and 73M1822 Demo Boards. Some components are optional and may or may not be needed for a particular application.

- C24 can be used to improve the radiated EMI, but is not needed in most applications. Generally the normal product shielding for other circuitry will be adequate for the DAA circuits as well. The power supply bypassing can also be adjusted to optimize the EMI performance verses parts count. This is highly dependent on the overall circuit layout, the use of power planes and circuit routing.
- R69 can be used if it is necessary to speed up the discharge of the internal circuitry after going on hook. In some applications it may be desirable to be able read the battery open circuit voltage soon after the 73M1x22 has gone on hook, so the value of R69 can be chosen to get the best settling time with the least impact on the overall operation of the circuits. Approximately 100 K is a good starting value and speeds up settling by 5X.
- For conditions where a highly inductive network connection is present, Zener diode D1 may be needed to limit the inductive kick-back that can lead to excessive voltages on the DAA circuit. This diode prevents voltages across the internal DAA circuits from exceeding 25 V. If current limiting is enabled, the Zener voltage rating should be increased to allow for the open circuit battery voltage.

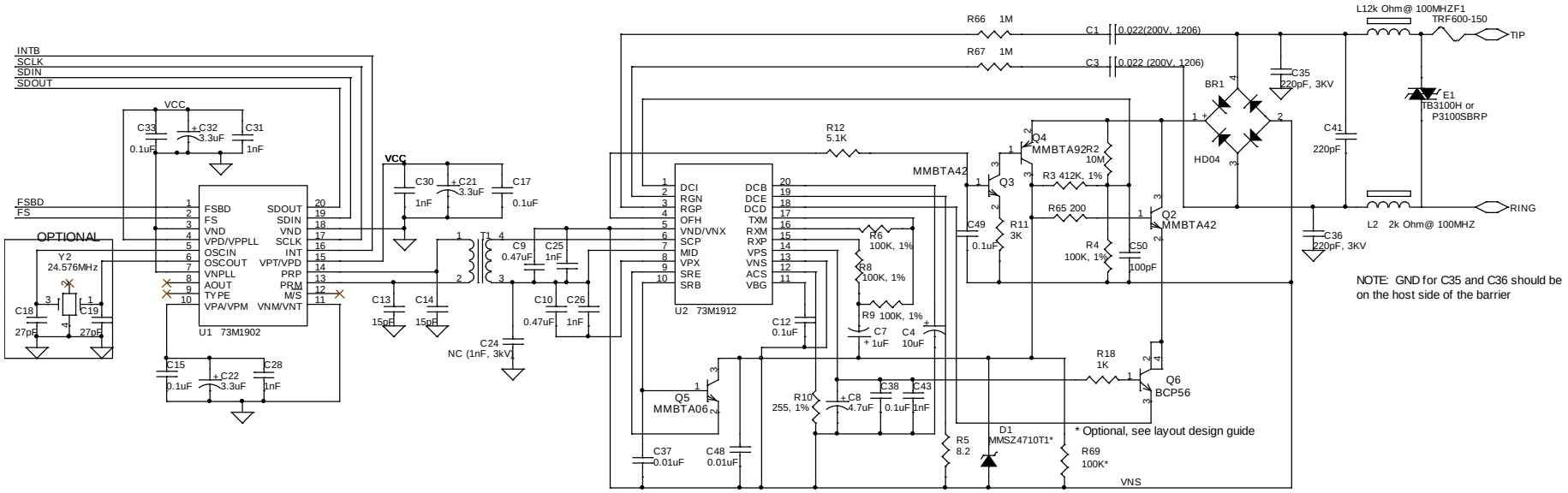

Figure 4: 73M1922 Reference Schematic

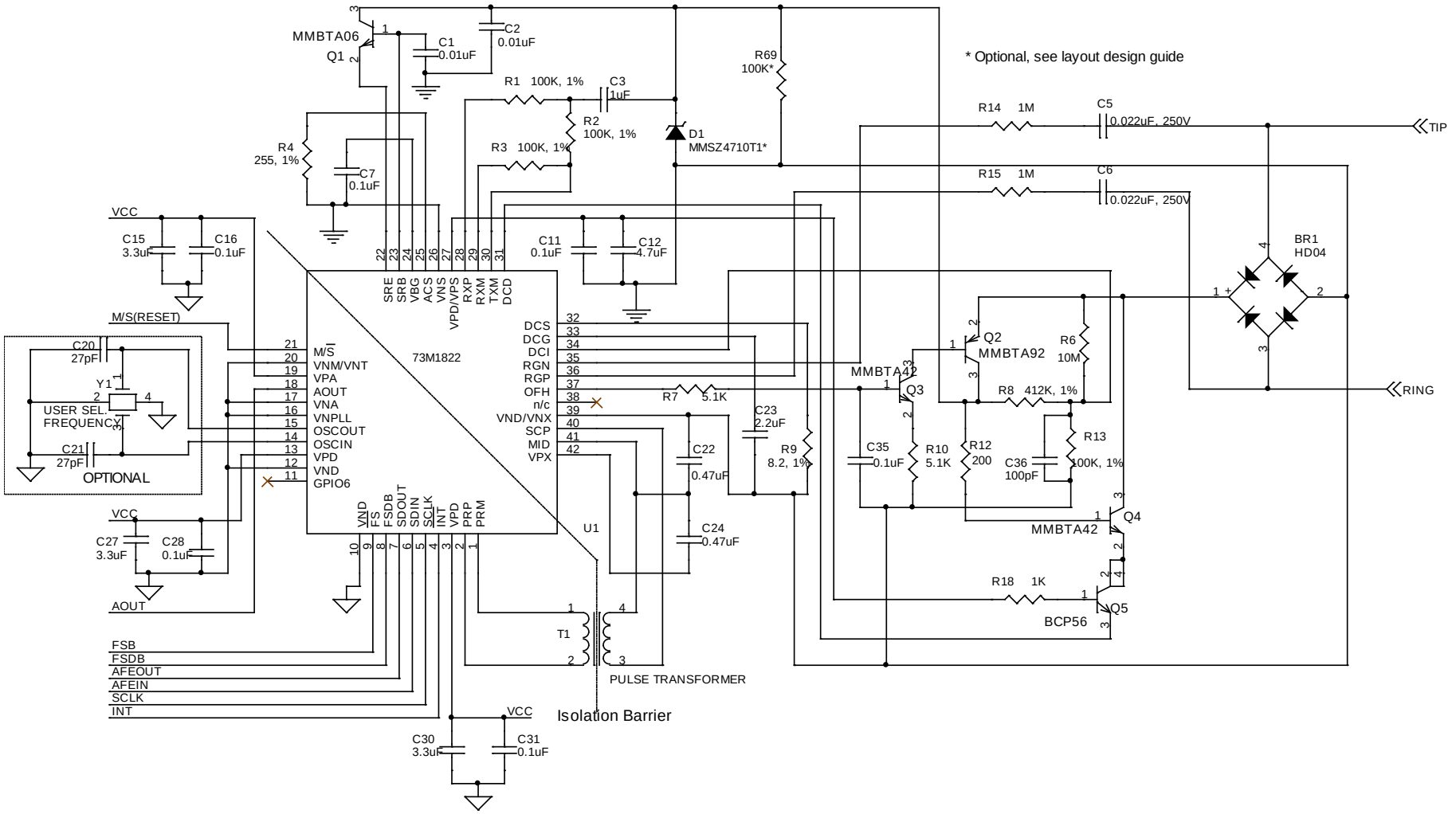

Figure 5: 73M1822 Reference Schematic

The reference schematics shown in Figure 4 and 5 are examples and are subject to change. For the latest schematic information, contact any sales office of Teridian Semiconductor Corporation.

Protection Circuitry

A thyristor (E1) across Tip and Ring rated at 275 V and 100 A (for the US) should follow the fuse. Besides protecting the DAA circuitry from power cross faults, the thyristor is necessary to pass safety testing that will be performed during certification. Many of the components in the DAA cannot tolerate the voltages and currents that the DAA will be subjected to without this protection.

It is very important to provide adequate heat dissipation for the line voltage protection device E1. Some PTT certification tests can be severe and require the voltage protection to operate for extended periods with a large current (>2 A) without failure in order to pass power cross safety testing (refer to UL60950 NAC Fig. 2, Test M-3). In this case, heat dissipation for the line voltage protection device (E1) should be provided by using 5 A-rated (2.5mm) circuit traces from the line connector to the thyristor.

Ring Detect and Caller ID Path

The components in the input circuit to the Ring Detect and Caller ID (RGN and RGP) pins of the Line-Side Device are used to provide necessary attenuation for this function. The attenuation means the RGN/RGP inputs will have a high impedance and will be sensitive to noise pick-up. The high-impedance side traces to the components must be kept short. Resistors used in the ring detection circuit (R66 and R67 in Figure 4) must be a 0805 size or larger to meet the voltage rating requirements of the line-side connections to the network. Similarly the capacitors (e.g. C1 and C3) require a voltage rating of at least 200 V to withstand the ringing and battery voltages. Any capacitors that bridge Tip and Ring need to be rated at least 275 VAC. Position these resistors and capacitors as close as possible to the 73M1912 network-side device to reduce noise pick-up and achieve the best possible performance.

Keep all analog signal traces separate from high-speed digital circuitry and traces. The barrier interface has relatively large, high-current signals when the 73M1912 Line-Side Device is in an operational mode. Signal traces to the RGN and RGP pins need to be kept physically separated from the barrier.

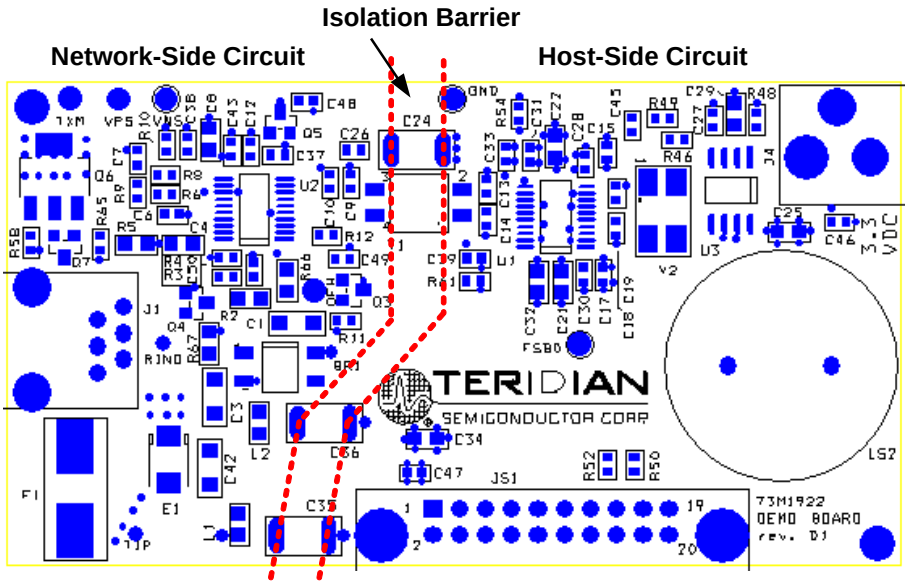

Figure 6: PCB Top View

Power Dissipation and Other Considerations for the Line-Side Circuits

Resistor R5 should be a 0805 to allow for worst-case conditions. This resistor carries the DC loop current and can dissipate in the order of 100 mW.

It is necessary to consider providing adequate heat dissipation for transistor Q6 (see Figure 3). Under normal operation, Q6 carries the DC loop current and may dissipate 600 mW under worst-case conditions. Additional metal on the collector tab PCB connection should be provided with copper on the top and bottom connected with PCB vias to join the two layers together. The 73M1922 board layout is illustrated in Figure 6 with corresponding top and bottom layer routing shown in Figure 7 and Figure 8. A minimum of 0.5 square inch of copper plane should be used on both the top and bottom layers.

In current-limit mode under worst-case conditions, over 2.4 W may be dissipated by Q6 (60 mA @ >40 V). If the 73M1922 current-limit mode is used, a higher-power transistor with a greater heat sinking capacitor may be necessary. SOT223 power transistor packages should not be used at these power levels. An NPN transistor with a package capable to dissipate at least 2.4 W and with a minimum beta of 60 (for example, the Fairchild KSD1273) is recommended to be used for Q6.

The circuit traces connecting the bridge rectifier (BR1 in Figure 4), the circuit connecting to the VNS pin and those that connect to the collector of Q5, should be 0.5 mm minimum width. These traces carry the DC loop current and transmit signals from the line-side device, and it is recommended that they be made larger to minimize the impedance.

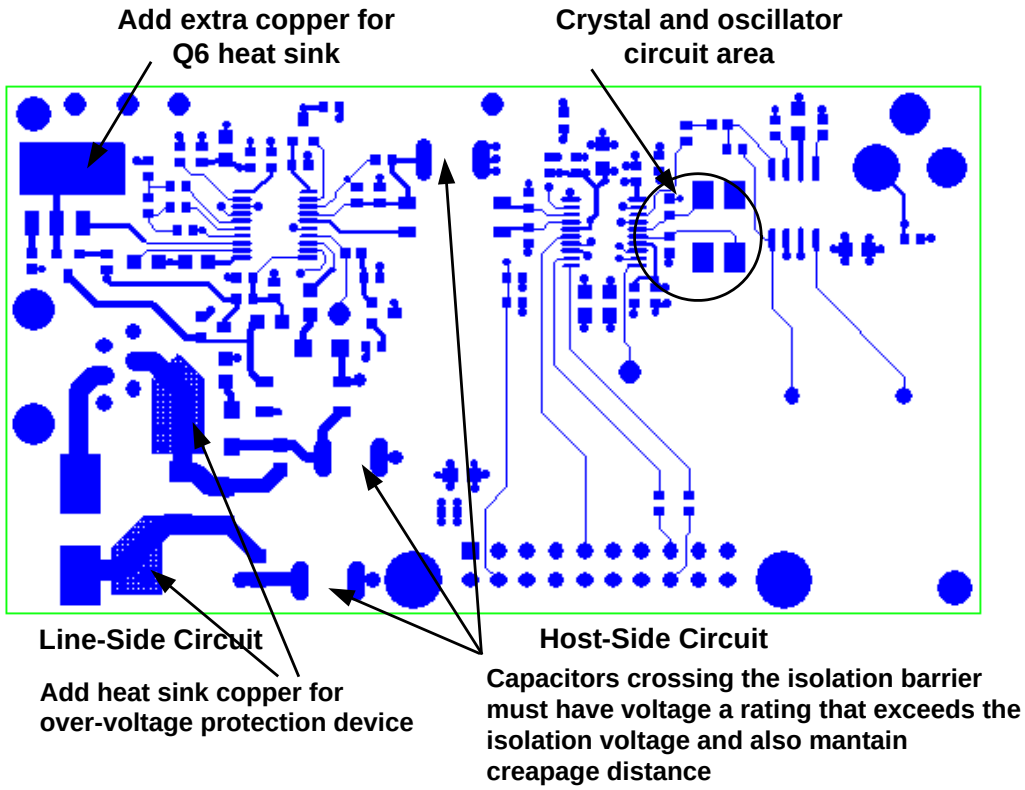

Figure 7: PCB Top Copper Layer

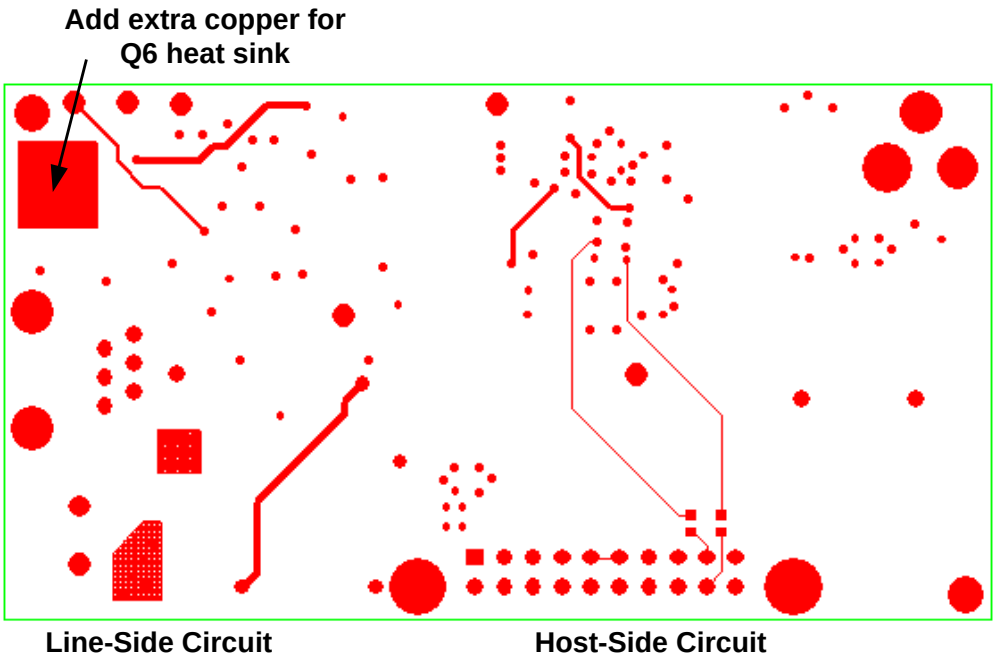

Figure 8: PCB Bottom Copper Layer

Special Layout Considerations for the 73M1822

The 73M1822 is intended for use in applications that require the smallest possible footprint at the expense of the greatest possible high voltage isolation. If isolation over 4.5 kV is required, the 73M1922 should be used instead. The minimum separation between the circuits on the line side and host side are on the bottom of the package. This minimum 73M1822 contact spacing is more than 2.5 mm; therefore it exceeds the IEC 60950 requirements for clearance and creepage. It is important that the PCB connections do not compromise the clearance by having less than 2.5 mm between the PCB mounting pads nearest the barrier separation. This also applies to the backside contact pads on the bottom of the 73M1822 package. It is also important that the assembly and attachment of the parts do not compromise the separation as well. The soldering process often leaves debris under the package, such as solder and flux, and this can degrade the isolation performance of the device even though the PCB layout provides adequate separation. Because the device package lies flat against the circuit board, it can be difficult to thoroughly clean in between them. Excessive solder is particularly difficult to remove after assembly, so great care needs to be taken during the soldering process. Many solder fluxes can be conductive to some degree, so washing needs to be thorough to get the best isolation voltage performance. Needles to say, the components on the Host-Side and Line-Side also need to maintain the same 2.5 mm clearance as the 73M1822 package in order to not violate the IEC 60950 requirement.

It should be noted that the 73M1822 package is not symmetrical where the corners separations for isolation are located. Do not infringe on the gap between the host and line-side connections when laying out the circuit traces. This can reduce the separations to less than the minimum 2.5 mm that is required by IEC 60950. Because of the asymmetry it may appear to be maintaining the spacing when it is not.

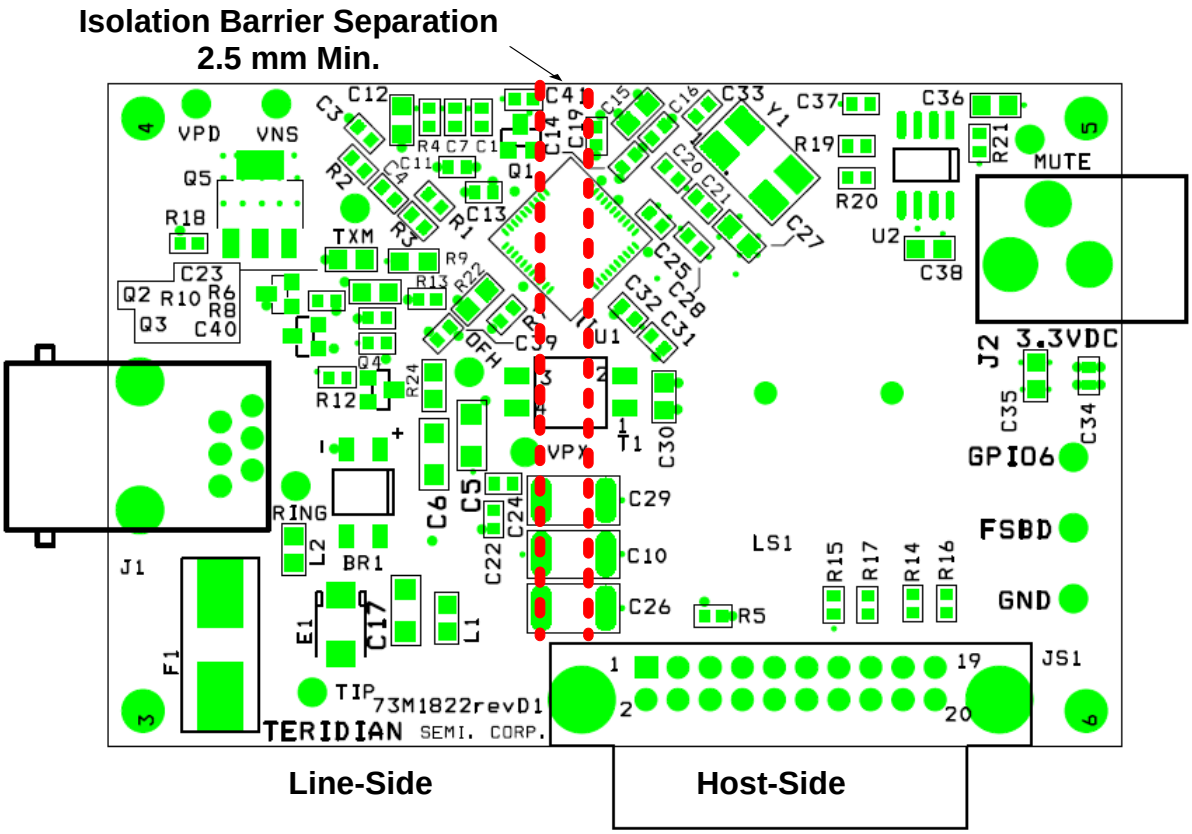

Figure 9: 73M1822 Reference PCB Top View

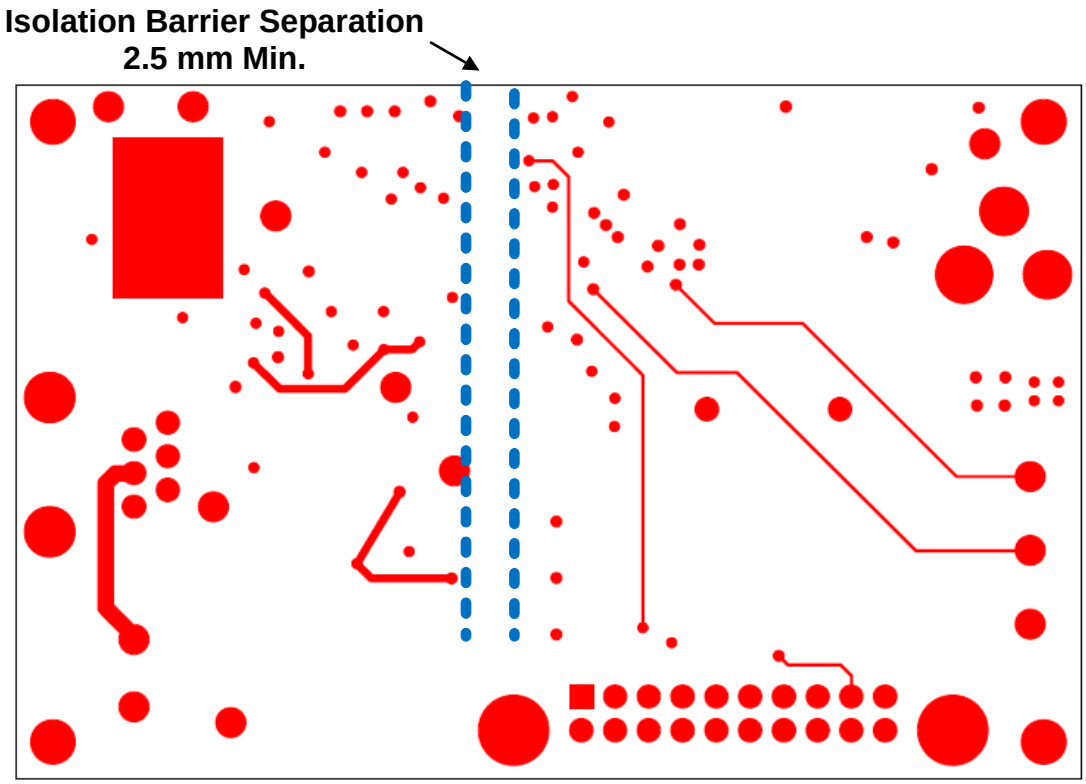

Figure 10: 73M1822 Reference PCB Bottom View

Exposed Bottom Pad on 73M1x22 QFN Packages

The 73M1822 and 73M1922 QFN packages have exposed pads on the underside that are intended for device manufacturing purposes. These exposed pads are not intended for thermal relief (heat dissipation) and should not be soldered to the PCB. Soldering of the exposed pad could also compromise electrical isolation/insulation requirements for proper voltage isolation. Avoid any PCB traces or through-hole vias on the PCB beneath the exposed pad area.

High Voltage Isolation Layout Considerations

The necessary isolation requirements between the host-side and line-side circuitry must be suitable for the specific design. Maintain at least ~1/8 inch (2.5 mm) separation between the 73M1x22 PSTN line-side and host-side routing and components to meet UL 60950-1, CSA 60950-1-03 and IEC60950 creepage distance requirements. Creepage is defined as the distance along a surface between two isolated conductors. All components crossing the isolation barrier must have a voltage rating at least as high as the desired isolation withstand voltage, including any capacitors for EMI and EMC control. If protection beyond the minimum is required, the creepage and clearance can be increased to 3.5 mm for 3 kV isolation. The power plane should also observe the same isolation boundaries as the other circuitry.

Note that Norway, Sweden, Denmark, and Finland typically have more stringent requirements for creepage. For these countries the creepage requirement is 4 mm instead of 2.5 mm. The 73M1922 can be used since it can easily be arranged to meet the 4 mm creepage requirement. Any transformers or capacitors that bridge the barrier also need to meet the 4 mm requirement.

Should it be necessary to place capacitors across the isolation barrier, these must have voltage ratings at least as high as the isolation that is required. These include C24, C35 and C36 in the schematic shown in Figure 4.

EMI and EMC Susceptibility

Equipment with clock rates greater than 100 kHz must be tested for EMI (high frequency energy radiated by the product) and EMC (operation in the presence of high levels of EMI). The amount of additional protection needed is dependent on the layout and adherence to the following good layout practices:

- The layout must limit the area of any current loops to a minimum, maintaining close routing between source and return current paths.
- Route power supply traces such that the source and return current paths are on opposite sides of the PCB and directly beneath each other. This keeps the loop area to a minimum.
- Use ground and power planes on the 73M1x22 Host-Side, but avoid these on the 73M1x22 line-side circuitry.
- A shielded enclosure will reduce most of the EMI/EMC; so minimal additional EMI filtering may only be needed.

The 73M1x22 Demo Boards include provisions for EMI/EMC suppression on the board. These are used when testing the bare board for EMI/EMC, but are not necessary if the modem is mounted in an EMI/EMC shielded case. Attention to high-frequency and low-frequency bypassing can minimize EMI at the source.

- EMI/EMC components at the entry/exit point for the analog signals (Tip and Ring) will usually be sufficient to maintain conducted emissions at acceptable levels and reduce susceptibility.
- Use only UL, CSA or TUV approved components when they cross the isolation barrier or for network protection to assure compliant performance for the DAA.
- Bypassing with X7R ceramic capacitors will yield the best results.
- For the best high frequency results, use 1000 pF capacitors in parallel with a 0.1 µF and 3.3 µF for power supply bypassing.
- Shielding by the product enclosure will minimize the requirements for added protection directly on the 73M1822/73M1922 circuits.

Considerations for High-Frequency Signals

Appropriate consideration needs to be made for the following:

- Crystal oscillator and clock layout.
- Barrier interface layout.
- MAFE interface layout.

This section provides guidelines for these areas.

Crystal Oscillator and Clock Layout

The 73M1x22 requires a clock source either from an external device or a crystal oscillator circuit. When the external system clock is fed to the OSCIN pin, the routing should be kept as short as possible and without any sharp turns in the trace. Running a ground trace in parallel with this trace would be helpful. Make sure this trace does not cross a broken ground plane or power plane to avoid unwanted radiation. When using a local oscillator similar considerations are required. If using a crystal oscillator, make sure the traces are kept as short as possible and both the OSCIN and OSCOUT signal traces are symmetric with the capacitor layout.

Barrier Interface Layout

The 73M1x22 line interface circuitry is powered from the host interface circuitry over the transformer barrier. Digitized analog signal samples, control and status data are transferred across this barrier between the two circuits. The barrier carries high-energy, high-frequency pulses that can go up to 4-5 MHz. This can be a potential noise source. To avoid any such undesirable radiation, make sure the PRP, PRM to transformer traces are straight and as short as possible and that both traces are symmetric along with the provisional capacitor layout. Smoothing capacitors from each driver pin to GND can be useful for EMI/EMC performance.

MAFE Interface Layout

The SCLK, SDIN, SDOUT, $\overline{FS}$ and $\overline{FSD}$ signals can be sources of noise. These signal traces should be carefully laid out with the shortest possible distances. Make sure these traces do not cross a broken ground plane or power plane to avoid unwanted radiation.

Cost Reducing the Design

The overall cost of the design can be reduced in many ways:

- Some of the high-voltage capacitors can be “built” using lower voltage capacitors in series. Lower voltage capacitors are generally less expensive than high-voltage parts, even though they have a higher capacitance value. For example, two 0.047 µF 100 V capacitors in series may be less expensive than a 0.022 µF 200V part. If a lower isolation voltage can be tolerated, 2 kV capacitors can be used in place of the 3 kV parts that are specified.
- The bridge diode can also be built from two lower cost dual diodes in a smaller SOT-23 type package. The overall footprint and placement can be made smaller and more flexible as well. The MMBD2004S is an example of a part that could be used.
- The reference design was intended to meet worldwide certification with a single design. Some countries have less stringent requirements for the fuses and thyristors than those used in this design. If the design will only be used in countries where less stringent standards are required, lower cost versions of these parts can be used. It is possible to avoid fuses altogether if the product is in a fire enclosure and is supplied with a 26 AWG or larger RJ-11 telephone cable. But if this route is chosen, the reliability, potential fire and damage to the other circuits in the enclosure should also be considered.

Revision History

Revision	Date	Description
1.0	8/20/2007	First publication initial draft.
1.1	9/17/2007	Replaced the schematic in Figure 3. Removed “C24” from page 6, paragraph 3.
2.0	10/17/2008	Added layout guidelines and information specific to the 73M1822. Renamed document to *73M1822/73M1922 Layout Guidelines* from *73M1922 Layout Guidelines*. Renumbered the document to AN_1x22_018 from AN_1922_003.
2.1	8/10/2009	Added revised schematics with new information about optional components. Added the Cost Reducing the Design section.
2.2	10/9/2009	Added explanation about protection devices to the Connections to Tip and Ring section. Updated the schematics in Figure 4 and Figure 5. In the Reference Schematics and Layout Examples section, added the second and third bullet. Added the Pulse Transformer Considerations section.