



Maxim > Design Support > Technical Documents > Reference Designs > A/D and D/A Conversion/Sampling Circuits > APP 4655
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REFERENCE DESIGN 4655 INCLUDES: ✓Tested Circuit ✓Schematic ✓Description ✓Test Data ✓Software

Signal Conditioning for a Sigma-Delta ADC in Industrial Multichannel Data Acquisition Systems

By: Joseph Shtargot, Strategic Applications Engineer

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Abstract: This application note will help the designer of a high-performance, multichannel data acquisition system (DAS) configure the proper interface between industrial sensors and high-performance ADCs. The example used is a power-grid monitoring system. The article explains advantages of the MAX11040K ADC's sigma-delta architecture, and how to select the proper schematic and components to achieve optimum system performance.

Introduction

Many new advanced industrial applications require an interface between a high-performance data-acquisition system (DAS) and multiple sensors. When this interface requires multichannel highly accurate amplitude and phase information, these industrial applications can take advantage of very high-dynamic-range, simultaneous-sampling, multichannel ADCs like the [MAX11040K](#). This application note explains the MAX11040K's sigma-delta architecture and how to select the proper schematic and components to achieve optimal system performance.

The Benefits of a High-Speed, Sigma-Delta Architecture

Consider as an example an advanced 3-phase power-line monitoring/measurement system shown in **Figure 1**. These industrial applications require accurate simultaneous, multichannel measurement over a wide dynamic range up to 117dB at a sample rate up to 64ksps. To optimize system precision, signals from the sensors (e.g., the CT and PT transformers in Figure 1) should be properly "conditioned" to meet the ADCs input ranges and ensure that the DAS characteristics will enable measurements in compliance with international standards.

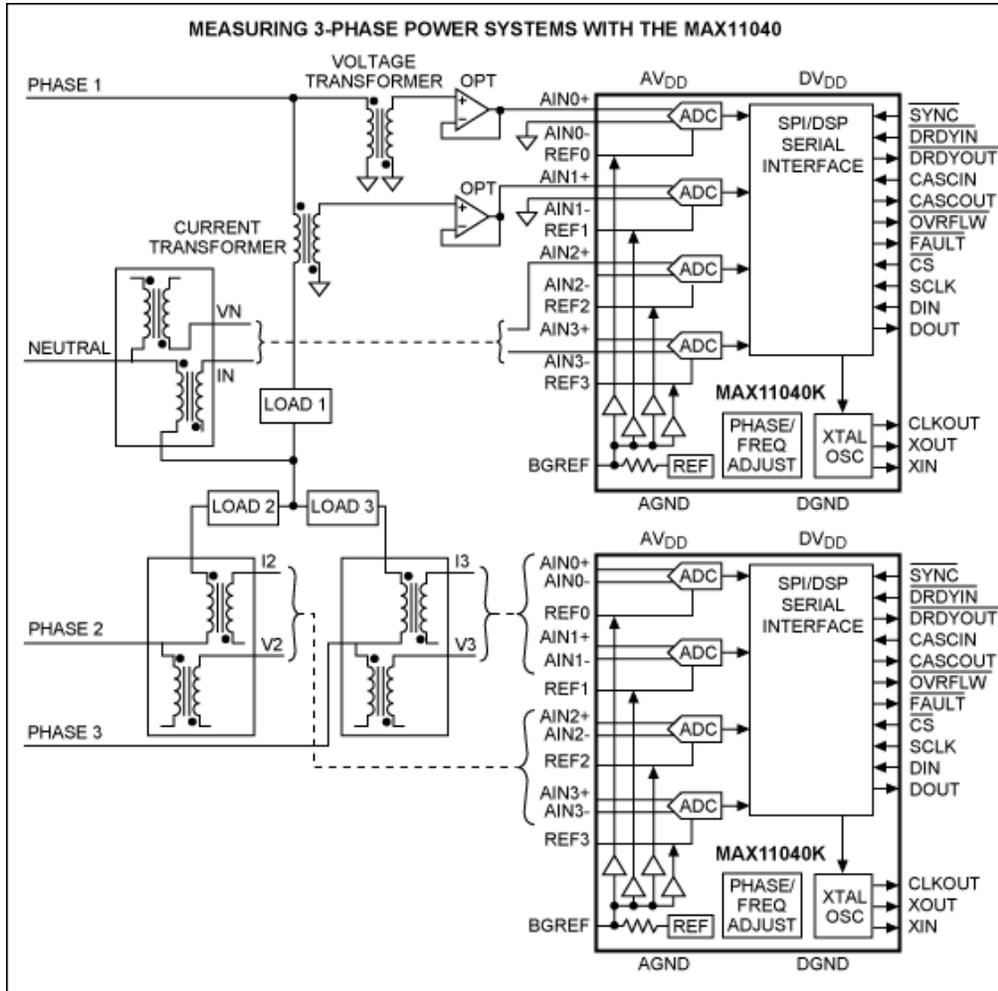


Figure 1. A power-grid monitoring application for a MAX11040K-based DAS.

Figure 1 illustrates that two MAX11040K ADCs can simultaneously measure the three phases and a neutral voltages plus the currents. The ADCs are based on the sigma-delta architecture, which uses an oversampling/averaging process to achieve high resolution. Each ADC channel performs analog-to-digital conversion on its input using a dedicated switched-capacitor sigma-delta modulator. The modulator converts the input signal into low-resolution digital data for which the average value represents the digitized signal information at 3.072MSPS for a 24.576MHz clock. This data stream is then presented to an internal digital filter for processing to remove any high-frequency noise. The result of these operations is a high-resolution, 24-bit output data stream.

The MAX11040K is also a 4-channel simultaneous-sampling ADC where output data represent processed and averaged values. These values cannot be considered "instantaneous" like in the successive-approximation-register (SAR) ADCs.^{1,2}

The MAX11040K provides designers with many capabilities that are not achievable in a SAR-based architecture: a very high dynamic range of 117dB SNR at 1ksps; integral and differential nonlinearity (INL and DNL) on the order of magnitude better than in a SAR-based ADC; and a unique, adjustable sampling phase (sampling point) that enables internal compensation for phase shift due to external circuitry such as dividers, transformers, or filters at the inputs.

Additionally, the MAX11040K integrates an on-chip digital lowpass filter that processes the data stream from each modulator and generates noise-free high-resolution output data. The lowpass filter has a complex frequency-response function determined by the programmable output data rate. The combination of the input resistor/capacitor (RC) filter and the digital lowpass MAX11040K filter can be used to reduce, or eliminate completely, the complexity of

the anti-aliasing filter design required on the input signal path to the MAX11040K. Some characteristics of the MAX11040K are shown in **Table 1**. For more detailed information about the MAX11040K's digital lowpass filter or the characteristics shown in the table, see the device's data sheet.

Table 1. Important typical characteristics of the MAX11040K ADC.

Part	Channels	Input range (V _{P-P})	Resolution (bits)	Speed (ksps, max)	SINAD (1ksps) (dB)	Input impedance
MAX11040K	4	±2.2	24	64	117	High, (130kΩ, approx)

ADC Performance Requirements in the Powerline Application

The outputs of the CT (current) and PT (voltage) sensor transformers in this application are typically ±10V or ±5V peak to peak (V_{P-P}). The MAX11040K's ±2.2V_{P-P} input range is below these typical outputs from the CT and PT transformers. There is, however, a simple and cost-effective approach to accommodate the transformers' ±5V or ±10V ranges with the MAX11040K's lower input range. This is shown in **Figure 2**.

The circuit connected to channel 1 represents a single-ended design. In this configuration, one side of the transformer is tied to ground and signal conditioning is achieved by one simple resistive-divider and capacitor.

If common-mode noise (noise which is the same to both ADC inputs) represents a serious concern, then a differential design is recommended as shown in the circuit connected to channel 4. By taking advantage of the MAX11040K's truly differential inputs in this design, noise effects are reduced.

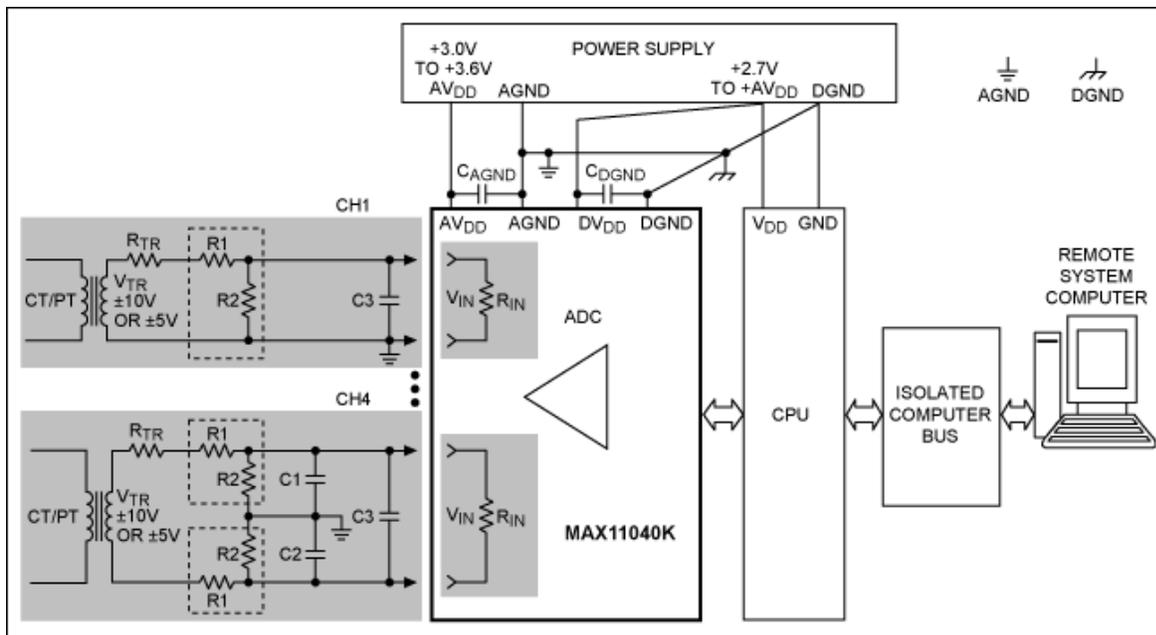


Figure 2. Board-level block diagram of a typical power-line monitoring application using the MAX11040K. Drawing shows a ±10V or ±5V transformer interface. The CH4 interface represents a differential design, while the CH1 interface is a single-ended design.

PT and CT measurement transformers represent relatively low-impedance sensors. (Effective impedance, R_{TR} , is in the order of 10Ω to 100Ω). Two assumptions are made for the calculation examples and experiments below: the transformers represent voltage sources with an effective output resistive impedance $R_{TR} = 50\Omega$; and for the purpose of demonstration, the transformers could be replaced by low-distortion function generators with an output impedance of 50Ω, as shown in **Figure 3**. The input impedance of the MAX11040K is set by the clock rate and ADC input capacitor value. With a proper bypass capacitor, C3, and with XIN clock frequency = 24.576MHz, then the input impedance, R_{IN} , is equivalent to 130kΩ ±15%. The tolerance limits are set by variations in the internal input

capacitor.

The resistor-divider networks of R1 and R2 need to scale the input signal $\pm 10V$ or $\pm 5V$ to the full-scale range (FSR) of the ADC equaling $\pm 2.2V$. For this circuit to work properly, optimal values for the resistors R1 and R2 and capacitors C1, C2, and C3 are selected to accommodate the $\pm 10V$ or $\pm 5V$ input values. The resistors R1 and R2 must have a high enough impedance to avoid substantial loading on the CT and PT transformers' outputs. The value of R2 should also be low enough not to be "loaded" itself by the input impedance of the ADC ($R2 \ll R_{IN}$).

For single-ended designs, the MAX11040K's input voltage, $V_{IN}(f)$, for channel 1 in Figure 2 can be calculated using Equation 1:

$$V_{IN}(f) = \frac{(R2 \parallel R_{IN})}{\sqrt{(R_{TR} + R1 + R2 \parallel R_{IN})^2 + (2\pi \times f \times R2 \parallel R_{IN} \times C3)^2}} \times V_{TR} \quad (\text{Eq. 1})$$

Where:

V_{TR} is the output voltage of the CT and PT transformers.

R_{TR} is the transformers' effective impedance.

R1, R2 are the resistive-divider networks.

R_{IN} is the input impedance of the MAX11040K.

$R2 \parallel R_{IN}$ is the parallel impedance of R2 and R_{IN} .

C3 is the input bypass capacitor.

f is the input signal frequency.

$V_{IN}(f)$ is the MAX11040K's input voltage.

A very similar approach can be used for a differential design.

To maintain a precision resistance ratio and proper bypass characteristics, resistors should be metal-film type with tolerances of 1% or better and with a low temperature coefficient. Capacitors should be precision ceramic or film capacitors. It is preferable to acquire components from reputable sources like Panasonic®, Rohm®, Vishay®, Kemet®, and AVX® products.

The [MAX11040EVKIT](#) offers a fully functional 8-channel DAS. The EV kit can help a design engineer to expedite real-life developments such as verification of the schematic solution suggested in Figure 2.

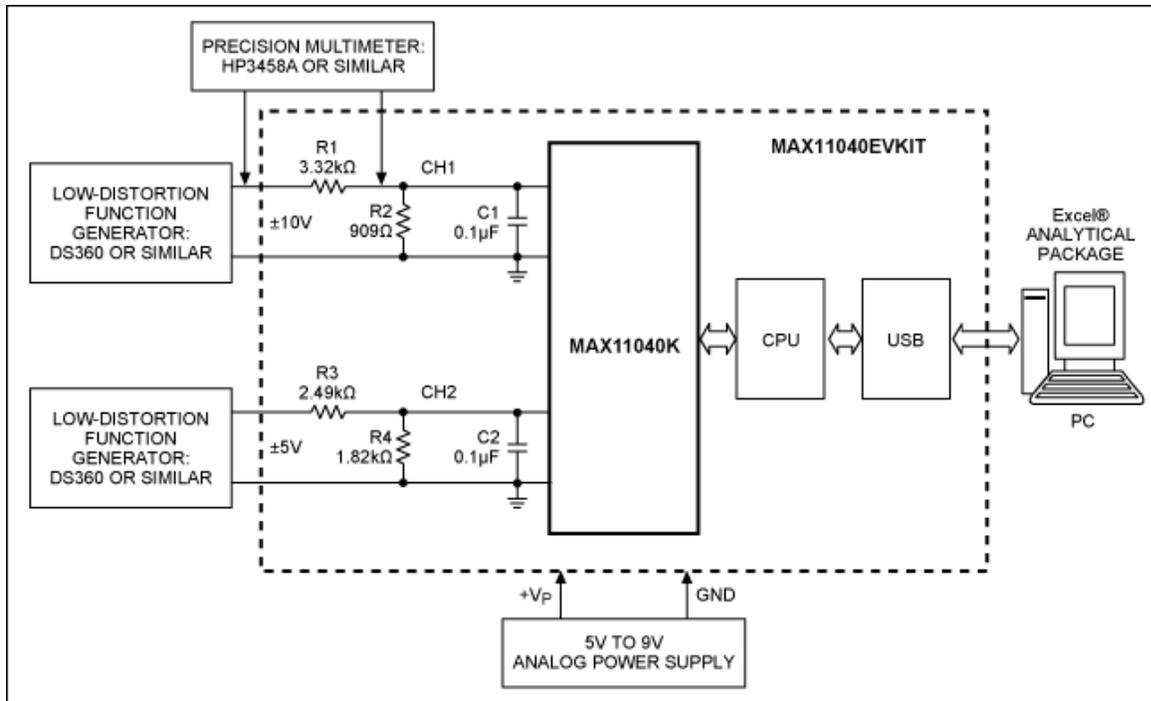


Figure 3. Block diagram of a MAX11040EVKIT-based development system. Two precision instruments are needed to accomplish proper calibration of the measurement channels. Measurement results could be transferred through the USB port to a PC and then converted to Excel® files for further processing.

±5V signals from a function generator are connected to the MAX11040K's channel 2, while ±10V signals from a function generator are connected to the MAX11040K's input, channel 1. The resistor-dividers networks, R1/R2 and R3/R4 will scale the input signal ±5V or ±10V, respectively, to the approximate full-scale range (FSR = ±2.2V_{P-P}) of the ADC.

Resistor-divider values R1 and R2, as well as the bypass capacitors C1 and C2 shown in **Table 2** were selected using equation 1 to achieve a near-optimal input dynamic range (around ±2.10V_{P-P}). This dynamic range is within the limits of the high relative accuracy on the order 0.05%, or better, for the MAX11040K. For more detailed information regarding this accuracy specification, see the MAX11040K data sheet.

Table 2. Calculation for resistors and bypass capacitors in Figure 3.

V _{TR} ±V _{P-P}	R _{TR} (Ω)	R1 (Ω)	R2 (Ω)	R _{IN} (Ω)	C3 (μF)	f (Hz)	V _{IN} ±V _{P-P}	V _{ADC} (VRMS)	Calibration factor-K _{CAL}	Calibration factor error (%)
Calculations for nominal V_{TR} and standard components (nominal) values										
10	50	3320	909	130000	0.1	50	2.11268	1.4939	4.73301	0.70
5	50	2490	1820	130000	0.1	50	2.07026	1.46395	2.41516	0.99
Measured values for V_{TR}, V_{IN}, V_{INRMS} with real components values and tolerances used in the experiment										
9.863	50 ± 10%	3320 ± 1%	909 ± 1%	130000 ± 15%	0.1 ± 10%	50	2.09872	1.483899	4.699912	0
4.932	50 ± 10%	2490 ± 1%	1820 ± 1%	130000 ± 15%	0.1 ± 10%	50	2.06151	1.45833	2.3914	0
0	50 ± 10%	2490 ± 1%	1820 ± 1%	130000 ± 15%	0.1 ± 10%	50	0	0.00048	NA	NA

The calculations in Table 2 were made with equation 1 and the precision measurements defined for Figure 3. The top portion of the table shows both the theoretical calculations from Equation 1 for nominal input voltages, and the

nominal selected standard values for discrete components. The lower portion of Table 2 demonstrates the real component values and tolerances used in the experiment, as well as the measured values used for the FSR calibration and K_{CAL} factor calculations below:

The calibration factor, K_{CAL} , is calculated using Equation 2:

$$K_{CAL} = V_{TRMAX}/(V_{ADCMAX} - V_{ADC0}) \quad (\text{Eq. 2})$$

Where:

V_{TRMAX} is the **maximum** values of inputs representing signals $\pm 5V$ or $\pm 10V$, respectively.

V_{ADCMAX} is the measured and processed ADC values with the MAX11040EVKIT settings similar to Figure 3 and the input signal set to V_{TRMAX} .

V_{ADC0} is the measured and processed ADC values with the MAX11040EVKIT settings similar to the Figure 3 input signal which is set to $V_{IN} = 0$ (system zero offset measurements).

K_{CAL} (in this experiment) is the calibration factor for the particular channel that will be used for calculation of the input signal V_{TR} using V_{ADC} .

The K_{CAL} error calculation shows that the "theoretical" K_{CAL} based on the nominal values *only* could produce errors in the order of 1% versus a calculation for K_{CAL} based on the real measured values.

These results mean that that a theoretical calculation alone is not sufficient for practical measurement; full-scale calibration (FSR) is needed for each measurement channel if the design is to exceed the required 0.2% precision for energy metering equipment as mandated by the popular EU IEC 62053 standard.

Table 3 shows the results that verify the measurements of the $\frac{1}{2}$ FSR input signals. Data were gathered using a precision HP3458A multimeter; ADC measurements and calculations were made with the calibration factor, K_{CAL} , of Equation 2.

Table 3. Verified measurements for $\frac{1}{2}$ FSR input signals.

Generator	Generator	MAX11040K	Calculation	Verr	Requirements
Nominal signal ($\frac{1}{2}$ FSR)	V_{TR_m} - signal measured by HP3458A	V_{IN} measured by ADC	$V_{TR_C} = V_{IN} \times$ K_{CAL}	$(V_{TR_M} - V_{TR_C}) \times$ $(100/V_{TR_C})$	IEC 62053
(V_{P-P})	(V_{RMS})	(V_{RMS})	(V_{RMS})	(%)	(%)
Channel 1: ± 5.000	3.4892	0.74259	3.490126	-0.026544	0.2
Channel 2: ± 2.500	1.7471	0.7307	1.747384	-0.016265	0.2

In Table 3 V_{TR_M} represents the measured value of the input $\frac{1}{2}$ FSR signal while V_{TR_C} represents the processed and calculated value of the input signal using the MAX11040K's measurements and K_{CAL} .

Results confirm that the measured error, V_{ERR} , of the conditioned circuits is below 0.03% which comfortably meets the 0.2% precision requirement mandated by the EU standard IEC 62053.

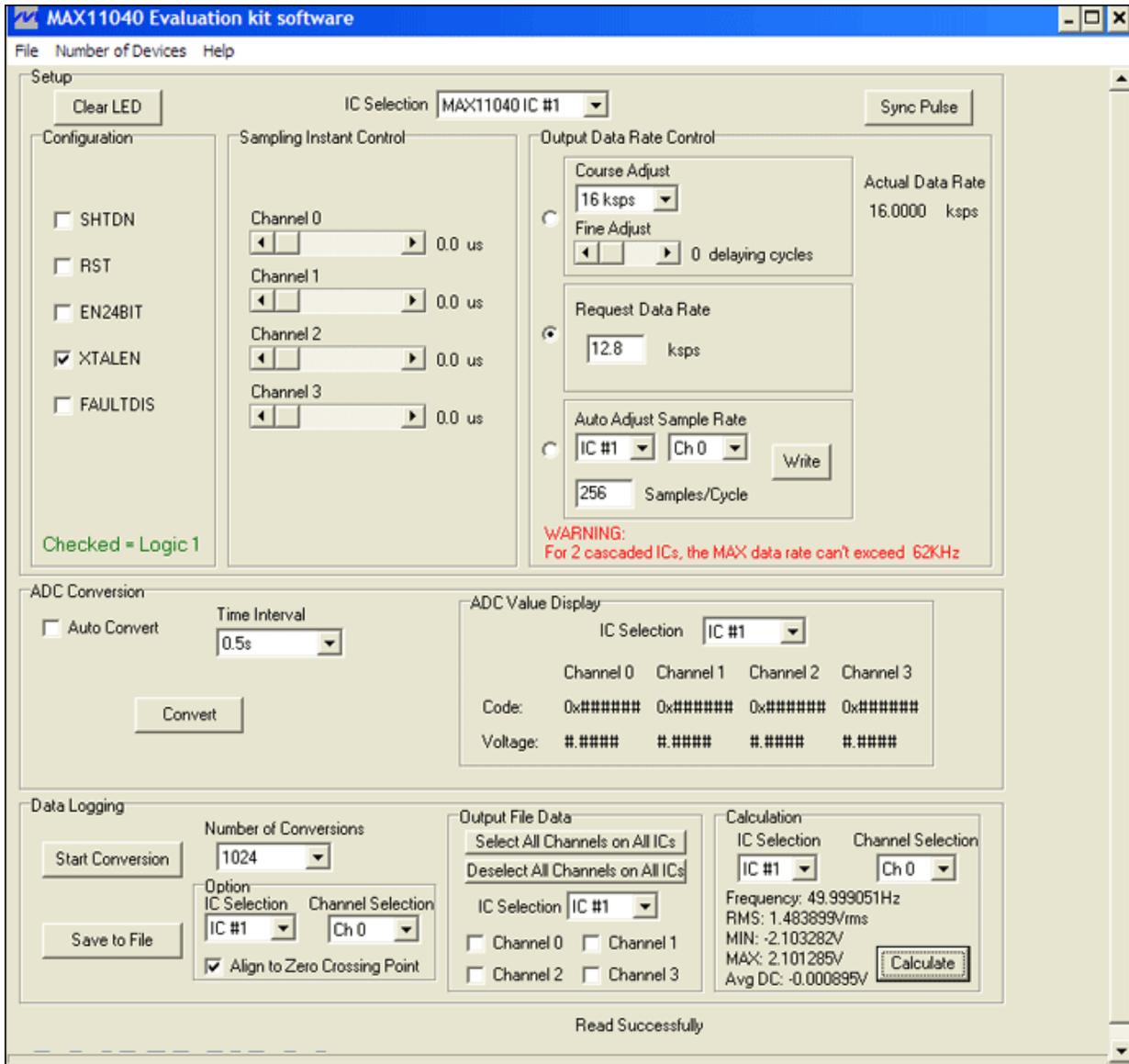


Figure 4. The MAX11040EVKIT GUI allows a user to conveniently set various measurement conditions: 12.8ksp/s, 256 samples/cycle, and 1024 as the number of conversions. Additionally, the calculation section of the GUI provides a convenient tool for engineering fast evaluations.

For more detailed analyses, measurement results can be transferred through a USB port to a PC and then the powerful (and free) complementary Excel analytical package can be used.

Conclusion

High-performance simultaneous-sampling, multichannel, sigma-delta ADCs like the MAX11040K are especially useful in a new DAS for industrial applications. These new ADCs provide a very high dynamic range up to 117dB, improved integral and differential nonlinearity, and a sample rate up to 64ksp/s. With a properly selected signal-conditioning circuit, the MAX11040K can meet and exceed the requirements of advanced specifications for "smart" power-grid monitoring systems.¹

References

1. See Maxim's application note 4595, "[Reduce system cost for advanced powerline monitoring by leveraging high-performance, simultaneous-sampling ADCs.](#)"
2. See Maxim's application note 4639, "[Use high-performance simultaneous-sampling ADCs for sensor signal conditioning in industrial multichannel data acquisition systems \(DASs\).](#)"
3. See Maxim's application note 4272, "[Overview of the MAX11040K 24-bit simultaneous-sampling, sigma-delta ADC.](#)"

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Related Parts

MAX11040K	24-/16-Bit, 4-Channel, Simultaneous-Sampling, Cascadable, Sigma-Delta ADCs	Free Samples
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REFERENCE DESIGN 4655, AN4655, AN 4655, APP4655, Appnote4655, Appnote 4655

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