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APPLICATION NOTE 4613

A Proposed Framework for Measuring, Identifying, and Eliminating Clock and Data Jitter on High-Speed Serial Communication Links

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Abstract: As the new and successful serial-data standards go from fast to very fast, designers must devote a greater amount of time to the analog aspect of those high-speed signals. It is no longer enough to remain in the digital domain with ones and zeros. To find and correct conditions that lead to potential problems, and thereby prevent those problems from showing up in the field, designers must also check the parametric realm of their designs. Signal integrity (SI) engineers must mitigate or eliminate the effects of timing jitter on system performance. The following discussion offers a simple and practical procedure for characterizing high-speed serial data links at 1Gbps and beyond.

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Introduction

The characterization of a high-speed serial link depends on the ability of the SI engineer to find, understand, and solve serious jitter problems. In this discussion, we assume that the clock and data recovery (CDR) block of the PHY (physical layer) or SerDes (serializer-deserializer) device complies with the standards applicable to that device. In a serial-communication system, the CDR recovers the clock signal from the data stream. Thus, a key operation is to extract data from the serial data stream and synchronize it with the data-transmitter clock.

The transmitter always contributes some jitter to the recovered clock, but we assume that contribution to be minimal. For simplification, therefore, we assume that any jitter seen on the recovered clock was coupled either onto the link in the cable (as EMI) or within the PCB (as crosstalk).

"Jitter transfer," "jitter tolerance," and "jitter generation" are important measures, but they apply more to PHY and SerDes devices than to the testing of system channels. We assume that the devices used in our design meet all device-level compliance testing. We therefore focus on the complete system, as we find a way to reliably capture serial data at the receiver. We look at system-channel characterization rather than device characterization. Such a channel (**Figure 1**) consists of the transmitter PHY, FR4 (PCB material), connector,

shielded cable, connector, FR4, and receiver PHY.

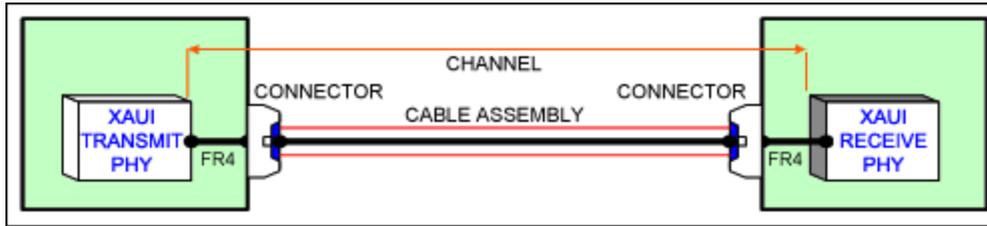


Figure 1. A channel lineup includes FR4 (PCB material), the cable and connectors, and more FR4.

The embedded telecomm card, a mixed-signal board used to collect many of the measurements in this article, is part of a "radio unit." The radio unit connects to the base station with a common public radio interface (CPRI), a new standard for communications between a base station and a radio unit. One physical layer in the CPRI includes the radio data (IQ data) as well as management, control, and synchronization information. For the application described in this article, the CPRI is specified to run on a serial link at 1.2288Gbps. This serial link is then characterized and measured to illustrate the jitter tests described in this article.

Jitter—Understanding its Make Up

The most important steps in achieving the performance specified for a high-speed serial-communications interface include understanding jitter, finding its causes, and eliminating some of its effects. This article is not a tutorial on the topic of jitter *per se*, but it would be difficult to talk about testing a serial-communication link without saying a word or two about jitter. Accordingly, the discussion in this section is directed to those who are new to the subject.

Jitter is defined as the variation of a signal edge from its ideal position in time. More to the point, jitter is the misalignment of the significant edges of a digital signal from their ideal positions in time (**Figure 2**). Jitter can also be viewed as an unwanted phase modulation of the digital signal. It is imperative that an SI engineer understand a basic premise at the outset: a receiver that meets the serial-link data rate while not also meeting its jitter specification may not operate reliably. Jitter characterization is, therefore, essential for guaranteeing an acceptable bit error rate (BER) for the system. Jitter can affect timing margins and synchronization, while causing a long list of other problems.

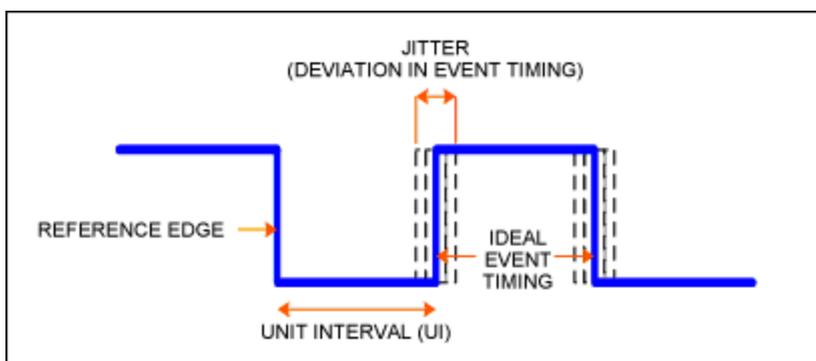


Figure 2. With respect to a single pulse, jitter can be defined as a deviation in edge timing.

Viewed as deviations of output transitions from their ideal positions, jitter is an important performance measure for both the clock and data signals of a serial link. The continuous incremental addition of jitter leads eventually to data errors. Remember that any time-domain measurement taken on a hardware system is only as good as the sampling signal used to acquire it.

Today's serial-communication systems have opted to embed clock information in the data stream rather than using an external trigger signal at the receiver. The clock must, therefore, be recovered from the received bit stream itself. This function, known as CDR, is shown in the block diagram for a typical SerDes receiver (**Figure 3**). If, however, the incoming signal has more than a certain amount of jitter or phase noise, the recovered clock cannot stay accurately aligned with the data. Misalignment causes an inaccurate placement of individual data points in time.

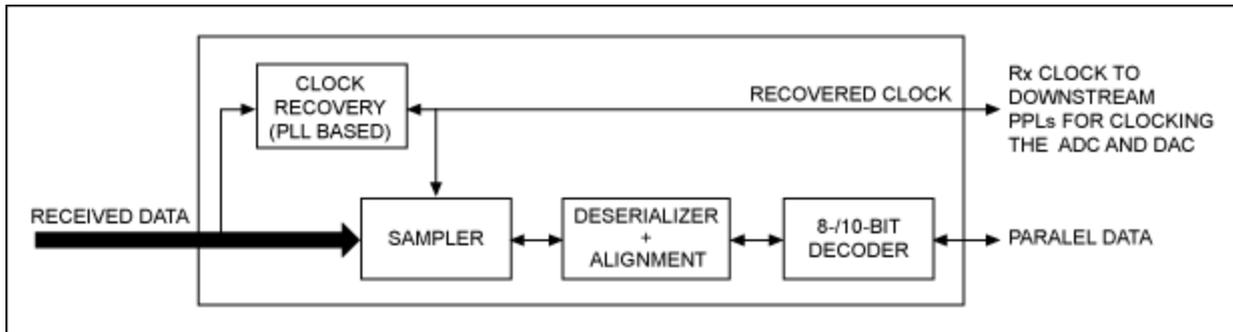


Figure 3. This block diagram depicts a generic SerDes receiver.

To minimize the BER, you must properly time this phase shift with the data stream, and for that reason serial-communication standards now place a greater importance on highly accurate measurement of jitter. Jitter is generally classified as deterministic jitter (DJ) or random jitter (RJ). Because each type of jitter is created differently, they are characterized separately.

Two Fundamental Components of Jitter: DJ and RJ

Random jitter represents timing noise with no discernable pattern. For the purpose of modeling, RJ is assumed to have a Gaussian probability distribution (**Figure 4**). Usually due to the forces of nature, RJ is statistical and unbounded. (It is characterized by its standard deviation value, expressed as an RMS quantity.) Thus, providing an RJ specification without a sample size does not make much sense. Other than measuring the value of RJ in a system, however, most designers do little else with this parameter. (Finding the cause of RJ is a difficult task, and beyond the scope of this article.)

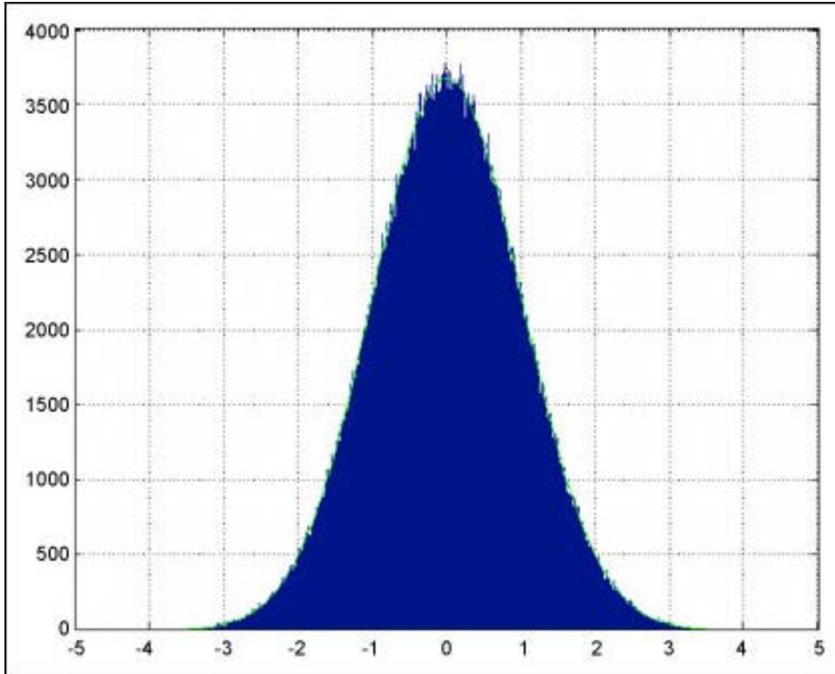


Figure 4. A Gaussian (normal) distribution is symmetrical with respect to the maximum value.

Deterministic jitter is caused by events in the system; it appears as timing noise with "somewhat" discernable patterns. DJ is usually repeatable, persistent, and predictable. In addition, it is usually the result of faulty design in areas such as the circuit, the layout, and the transmission line. It is typically non-Gaussian, as is power-supply noise due to a bad reference plane.

Deterministic jitter is further classified into subcomponents: periodic jitter (PJ in **Figure 5**); data-dependent jitter (DDJ, also known as intersymbol interference, or ISI); duty-cycle-distortion jitter (DCDJ); and any other timing jitter that is uncorrelated and bounded to the data. PJ can be caused by crosstalk from other signals and from semiconductor switching close to the serial-data signals); by electromagnetic interference (EMI); and by other unwanted modulation. DCDJ results from unbalanced transitions in the data (i.e., differences in rise and fall times), and DDJ is jitter correlated with bit sequences in the data stream (also affected by the channel's frequency response).¹

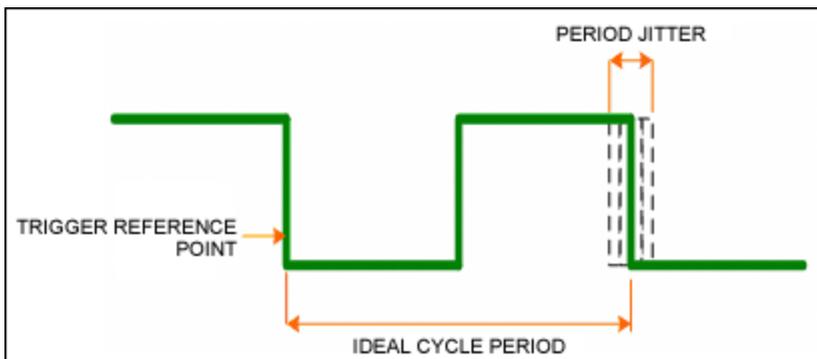


Figure 5. For PJ, the timing deviations have a predictable pattern.

Total Jitter (TJ)

As you might guess, TJ is composed of random and deterministic components (**Figure 6**). There are several techniques for estimating TJ. Some find the TJ by resolving it into the RJ and DJ components, then adding them together using a multiplier in front of the RJ component. Other methods find TJ by extrapolating the histogram of time interval error (TIE) measurements. TJ is usually a peak-to-peak value expressed in picoseconds or fractions of a unit interval (UI). For example, 0.2UI means that jitter is 20% of the data eye.

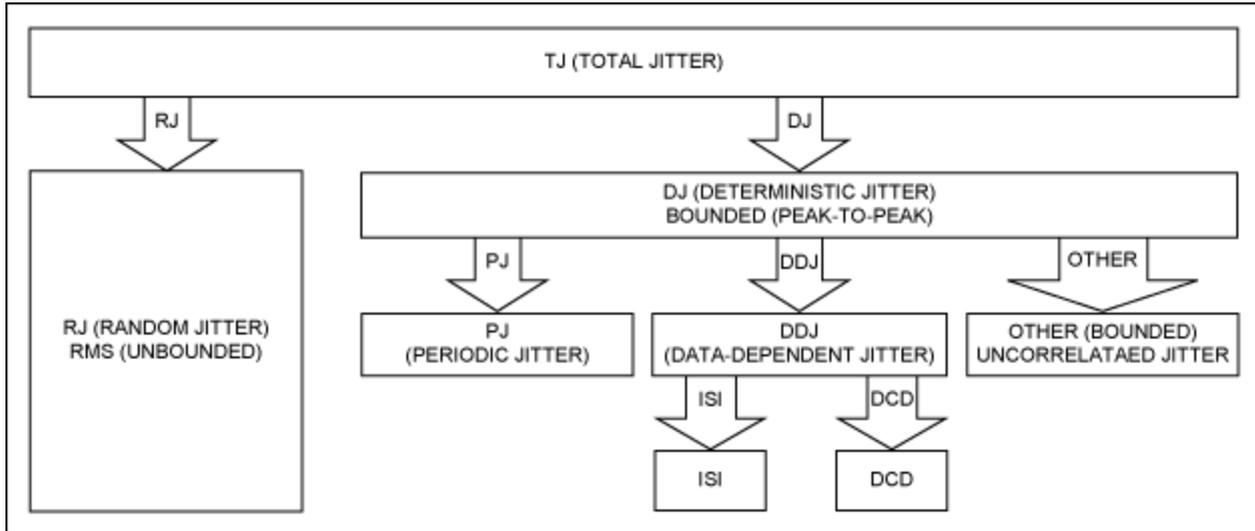


Figure 6. The total jitter in a system can include various types (components) as shown.

To predict the overall performance of a system, you must, therefore, understand the *types* of jitter and their effects. Because jitter causes timing errors, it has become increasingly important to characterize and qualify all jitter components in a system. Before that can be done, however, you must determine the sources of jitter. As mentioned earlier, the two types (random and deterministic) have different sources. A designer has little or no control over the sources of RJ in an existing system of embedded circuit boards,² but good design practices will greatly mitigate or even eliminate the sources of DJ. Each jitter component has a specific cause, as shown in **Table 1**.¹

Table 1. Common Sources of Jitter

Jitter Type	Common Source	Root Cause
Deterministic	EMI	Unwanted radiation of conducted emissions from other devices in the PCB or system, such as a switching power supply.
	Crosstalk	Undesired signals that result from coupling between adjacent conductors.
	Reflections	Impedance mismatch (or mismatches) on the signal lineup (ISI from the receiver's perspective), due to poor stubbing, incorrect or absent terminations, and/or discontinuities in the physical media.
Random	Shot noise	White noise generated when electrons and holes move in a semiconductor (i.e., noise within system components).
	Flicker noise	1/f noise, mostly at lower frequencies.
	Thermal noise	White noise generated by the transfer of energy between free electrons and ions. It is created by the movement and collision of electrons in the conductor.

Six Steps to Achieve a Well-Characterized, High-Speed Serial Link

Link-Characterization Framework

The link-characterization framework presented here helps to identify and measure the sources of clock and data jitter. The technique hinges on the designer's ability to separate jitter sources and to focus on the problem areas revealed by this testing framework. Jitter testing generally requires observation of a repeating test pattern on the channel.

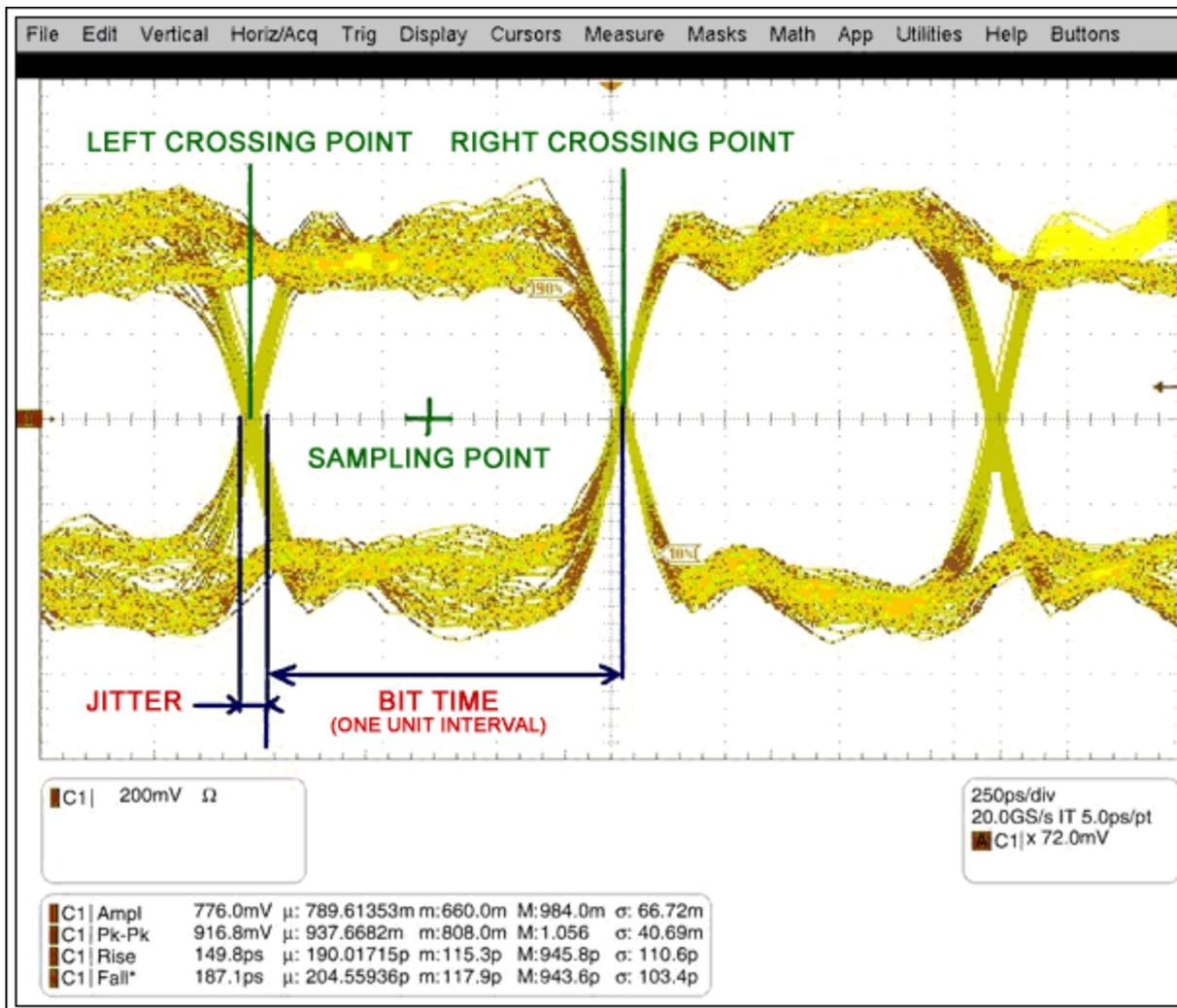
The data pattern to be used is important, because reflection and ISI are both data-dependent sources of noise. The test patterns used to collect the majority of plots in this paper included a mixed-frequency repeating K28.5 sequence (also known as the comma character: K28.5 = 00111110101100000101), and a pseudo-random bit sequence (PRBS-23). PRBS patterns give a good spread of the different bit sequences that might be observed in actual data traffic. Other compliance test patterns for jitter evaluation are available, including the jitter test pattern (JTPAT), compliance random pattern (CRPAT), and compliance JTPAT (CJTPAT), to name a few.

The key to getting accurate measurements lies in selecting the right measurement equipment for your application (oscilloscopes and probes, for instance). For step 1 of this framework (and for the remaining steps as well), the signal is measured after it has propagated through a channel formed by a 50Ω transmission line that also includes the cable, connector, and FR4 PCB. Solder to the PCB trace, as close as possible to the receiver IC, a differential, high-performance probe with high bandwidth and low capacitive loading.

Step 1. Quantify Random and Deterministic Jitter (RJ and DJ)

First, observe the signaling level. Then, collect link measurements and compare them to the standard. (**Table 2** gives an example of measurements versus the XAUI specification, which is a measurement of the PHY's input characteristics.) The SI engineer can create a similar matrix for the standard against which a system is being tested.

An eye diagram is one of the most important measurement tools to assess high-speed signal integrity. It overlays waveforms from multiple unit intervals (UIs), using either the real clock or a reconstructed clock as the timing reference. Because the eye diagram helps you to visualize amplitude behavior as well as the timing behavior of a waveform, it represents one of the most useful presentations of jitter. **Figure 7** shows an eye diagram measurement taken from a XAUI channel.



[More detailed image \(PDF, 1.4MB\)](#)

Figure 7. This eye diagram (XAUI measurement) is displayed at the input of a PHY device.

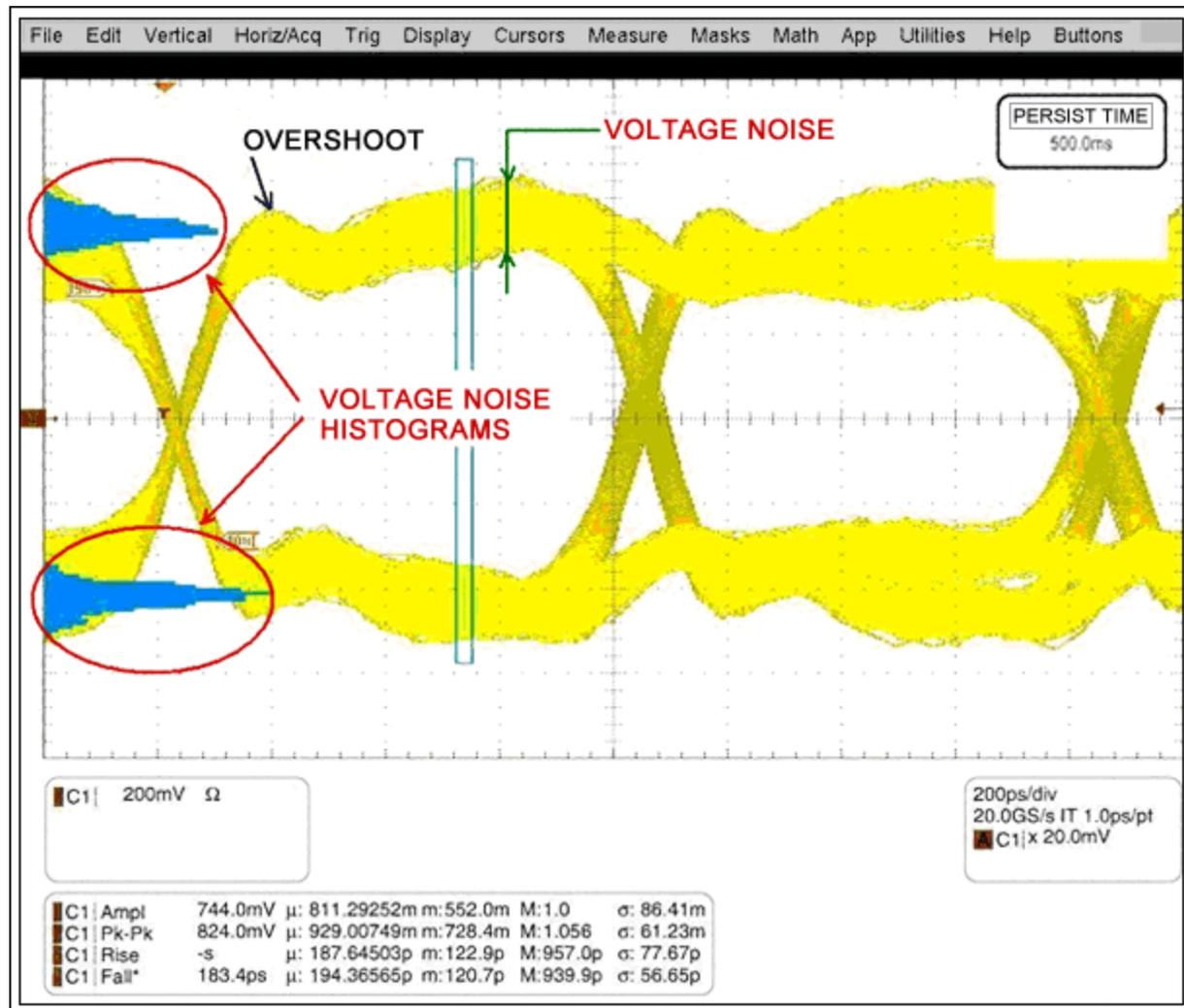
Use timing-analysis software loaded on the scope (e.g., a TDSJIT3 from Tektronix®, for example). With the scope set for "golden PLL," the SI engineer can set the parameters shown in Table 2 and capture an eye diagram of the channel traffic. Then, the matrix shown in Table 2 can be completed for the particular standard being used. (Golden PLL is a method for filtering out jitter on the scope trigger, thereby ensuring that any jitter represented in the measured jitter amplitude and histograms is actually present on the link.³)

Table 2. Measurements against the PHY Input Characteristics (Example)

Input Characteristics	Specification	Measurements
Differential rise and fall times (T_{RF})	?	
DJ tolerance	0.37UI	
TJ tolerance	0.65UI	
Differential amplitude (V_{P-P})	2.2 V_{P-P} (max)	

Step 2. Measure Amplitude Noise or Voltage Error Histograms

This step measures amplitude noise, which can cause error in the design. We are looking to see if the probability density functions (PDFs) for amplitude have a normal distribution for both the 1 and 0 levels. (Figure 8 shows the PDFs for an XAUI link.) The random-amplitude noise shown in blue in the histograms (circled in red) can be considered as normal distributions. The SI engineer can also use this plot as a graphic aid in determining whether other signaling issues are present, such as overshoot and undershoot. If amplitude noise is an issue (if the amplitude histograms are bimodal, for example), then we likely have a power-distribution problem on the board.

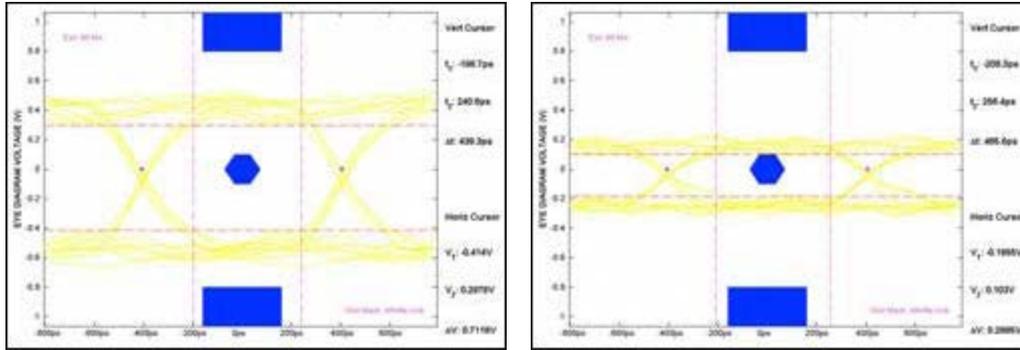


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Figure 8. Voltage noise can be derived from an eye diagram as shown here.

Step 3. Compare Eye Diagram versus "Far-End" Masks

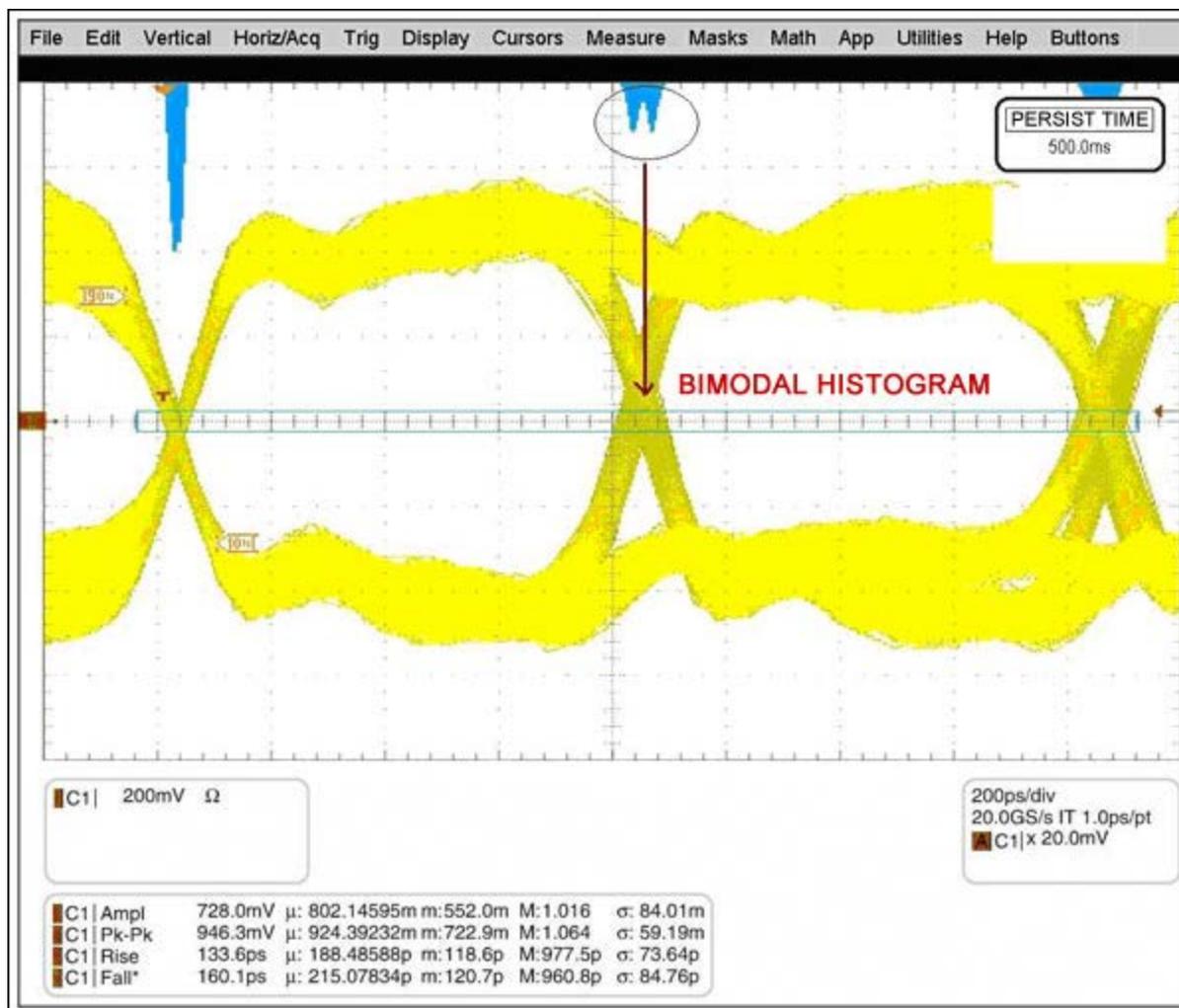
Step 3 lets you to estimate the jitter quality for the received signal over a long sequence of data. Many jitter application packages include standard masks, whose minimum-closure dimension allows you to rate the quality of the measured channel. By comparing the eye diagram to the receive masks, you can view the amount of eye closure in a given configuration. The eye should be clear of the masks (Figures 9a and 9b).



(a). [More detailed image](#) (PDF, 1.19MB) (b). [More detailed image](#) (PDF, 1.31MB)

Figure 9. By applying the XAUI far-end masks to a measured eye diagram, you can discern a bad case (a) and a good case (b).

At this stage, the tester also analyzes the eye plot's rising edges separately from the falling edges. In the example of **Figure 10**, one can clearly observe that the rising and falling edges are not aligned in the middle at the eye crossing point (the bimodal histogram circled at middle top of the figure). This bimodal histogram indicates the presence of cycle-to-cycle jitter or PJ on the channel. The histogram could also represent DCD or ISI jitter.



[More detailed image \(PDF, 1.9MB\)](#)

Figure 10. This data eye shows a bimodal histogram at the edge of the crossing.

Designers often limit their testing to a measurement of TJ and thus only view the histogram, which represents the TJ (DJ and RJ mixed together). However, to understand the root cause of jitter and eliminate its contributing components, it is essential to separate and identify each component. Since the eye diagram is a general tool that gives insight only into the amplitude and timing behavior of the signals, other means are needed to separate the jitter components.

In the next step, we separate TJ into its components by analyzing the jitter histogram and bathtub plots.

Step 4. Separate Jitter Types and Components

To keep jitter out of the system one must be able to separate the RJ and DJ components. The technique described in step 4 lets you distinguish these types of jitter, and helps with debugging and design verification as well as characterization of the system links.

We now analyze some of the histograms collected in the previous sections.

Histogram Plot

The TJ histogram is a good first look at the analysis of jitter. As mentioned above in *Two Fundamental Components of Jitter: DJ and RJ* and Figure 4, RJ is assumed to have a Gaussian (normal) distribution for the purpose of modeling. That means that its probability density function is described by the well-known bell curve. The TIE histograms associated with our PRBS-23 data are shown in **Figures 11a** and **11b**. Note that the TJ histogram can also be multimodal.

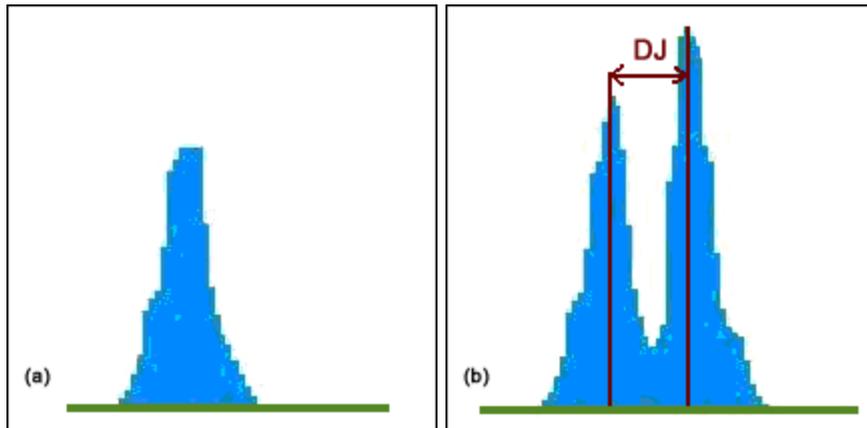


Figure 11. Typical jitter histograms can be almost Gaussian (a) and bimodal (b).

The histogram of Figure 11a is not necessarily ideal, but that of Figure 11b definitely points to issues with a poor design. As shown in Figure 10, a bimodal histogram involves rising and falling edges that are not aligned in the middle. (Some systemic problem is "messing up" the histogram and making it non-Gaussian.) A bimodal histogram usually indicates significant amounts of DJ.

When both DJ and RJ components are present, the jitter histogram is generally broadened and no longer resembles a Gaussian distribution. In that case, the difference between the left and right peak values represents DJ, and results from a crossing point that is a bit higher than it should be. This condition can be associated with DCD jitter due to a crosstalking signal with a given period. Thus, it is important for designers to analyze the histograms as complementary insights to eye diagrams.

Bathtub Plot

Like the histogram, the bathtub plot offers a powerful way to look at jitter and analyze its timing. By plotting BER as a function of sampling position within the bit interval, the bathtub plot represents eye opening versus BER (**Figure 12**). (Operation at an expected maximum error rate of 10^{-12} has become a *de facto* requirement in many serial standards.) As can be observed in Figure 12, DJ forms the almost flat horizontal portion of the bathtub curve (gold region), while the slope portion (blue region) is due to RJ. You can also see that that the following equation applies:

$$\text{Jitter eye opening} + \text{TJ} = 1\text{UI}$$

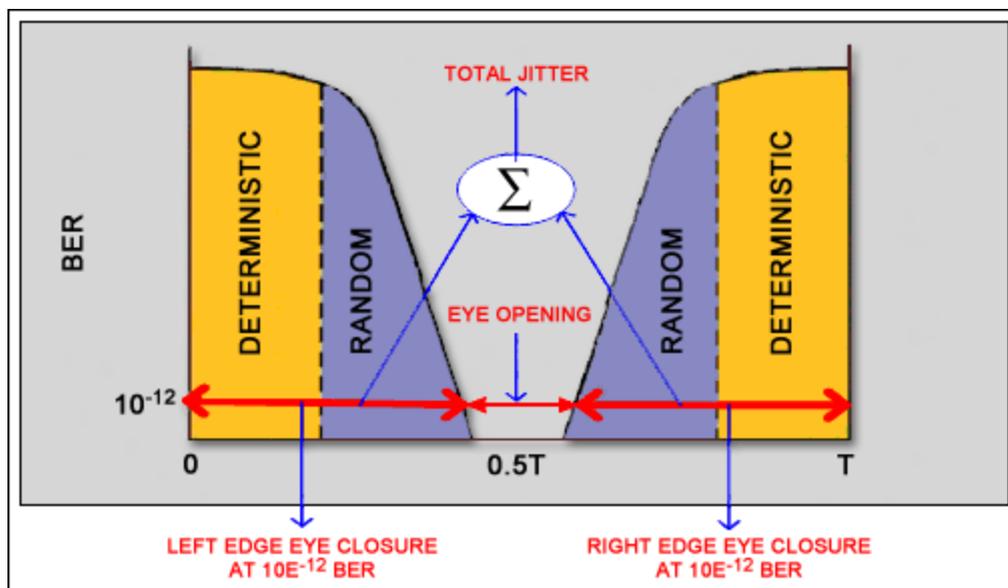


Figure 12. This bathtub plot shows BER vs. decision time.

The measurement of a jitter histogram, or bathtub curve, or both, is a primary step informing the SI engineer of jitter in the system. Neither measurement, however, reveals the individual sources of the jitter components. In the next step, we attempt to identify the root cause(s) of DJ by separating it into its components.

Step 5. Diagnose the Root Cause of Jitter

We now analyze jitter in the frequency domain, which reveals DJ components (i.e., PJ, ISI, DCD, etc.) as distinct single-frequency spurs (line spectra) that can be easily visualized to determine their sources. These frequency domain views can include the phase-noise plot, the jitter spectrum plots, or a fast Fourier transform (FFT) of the jitter trend.

Jitter Spectrum of Data TIE Plot

Several techniques are available for measuring jitter on a single waveform. One technique examines the spectrum of the TIE. TIE is the timing deviations of digital-data transitions from their ideal (jitter-free) locations. (See prior section on *Total jitter*.) In short, the TIE measures how far each active edge of the clock varies from its ideal position. TIE is important because it shows the cumulative effect of even a small amount of jitter³ over time.

We now return to the serial link being characterized. **Figure 13** shows a plot of the jitter spectrum of the TIE taken on the link. In the figure the spurs present a snapshot of the channel at a specific point in time. The spurs have been numbered F1, F2, F3, and F4. The first spur is at F1 = 61.44MHz (the fundamental frequency of the recovered clock). Spurs F2 and F4 are integer multiples (harmonics) of F1. Spur F3 is at 153.18MHz does not seem to fit in because there is no clock source on the board with this frequency. F3 represents an intermodulation of two or more frequencies on the card. It could also be produced when the high-speed signal crosses over a split in the power/ground plane. When high-speed signals pass over a split reference plane, the discontinuity in the return path for current can create emissions.

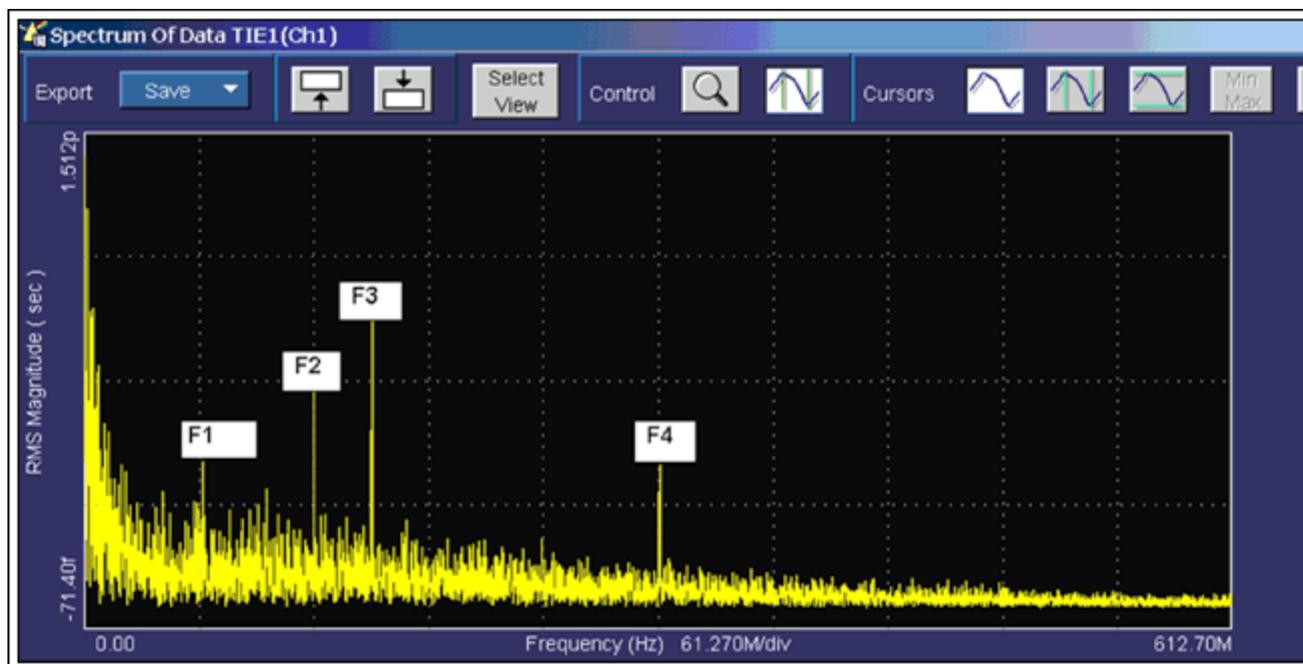


Figure 13. A spectrum of TIE for this data reveals four significant spurs of PJ.

Spectral Analysis

To reveal sources of jitter, the SI engineer must conduct a spectral analysis of the jitter spectrum plot to determine an idea of the modulation frequency of each jitter source. Frequency-domain plots exhibit the unique frequency spurs. You can isolate certain DJ components using the following methods:

Isolating PJ

Occasionally the serial data channel will show a nice looking histogram (a Gaussian distribution), yet the spectrum of TIE on the same link shows some spurs. This means that a small PJ can be buried in the RJ and not be visible on the histogram of TJ. It is, therefore, worthwhile to do the spectral analysis to eliminate all sources of jitter, even when the jitter numbers have not gone out of spec.

In the spectrum plot analysis in Figure 13, F3 was regarded as the result of an unwanted modulation. It is this type of unwanted modulation (due to EMI or crosstalk, for instance) that usually causes PJ. The signature of PJ is that it repeats at a fixed frequency. Such unwanted modulation can also be caused by cross-coupling, such as switching noise from the power-supply module coupling into the data or system clock.

Isolating duty Cycle Distortion (DCD)

DCD points to differences in the rise and fall times of the digital transitions and to variations in switching thresholds for the devices previously mentioned. DCD is caused both by voltage offsets between differential inputs and by differences in the system's rise and fall times. The rise and fall edges in Figure 9, for example, are not aligned in the middle. An SI engineer can attempt to isolate DCD by stimulating the system with a high-frequency pattern such D21.5 (1010101010...). That pattern is effective in showing DCD while eliminating ISI.

Isolating ISI

A common source of DDJ is the frequency response of the signal path through which the serial data is transmitted. ISI is a type of DDJ. It is created in the channel lineup that includes the cable and connectors; it is affected by losses in the FR4 PCB material. Because ISI is usually the result of a bandwidth limitation in either the transmitter or the signal path, limited rise and fall times in the signals can produce varying amplitudes for

the data bits.³ Another primary source of DDJ is impedance mismatch in the channel lineup due to an improper termination of the bus. Reflections caused by a transmission line with mismatched termination impedance can cause delays and/or attenuation of the transmitted signals.

Step 6. Optimizing Tx Preemphasis and Rx Equalization

It is well established that the amount of attenuation caused by lossy FR4 traces on a PCB depends on the signaling speed and the length of the transmission medium. In short, FR4 losses are more severe at the higher switching frequencies. Preemphasis and equalization can mitigate the effects of signal attenuation and degradation, thereby restoring the original signal. This link-optimization step not only applies to designs with PHY devices that support transmitter preemphasis and receiver equalization, but also to discrete ICs for preemphasis and equalization which can be used to compensate for the transmission losses caused by FR4 material. Step 6 applies to designs that include provision for tuning the preemphasis and equalization levels of SerDes/PHY devices. We therefore assume that the system in question includes such provisions.

Optimal Preemphasis

Preemphasis is a signal-improvement technique that opens the eye pattern at the far end of a cable (at the receiver). In general, preemphasis increases the transmitted signal quality by increasing the magnitude of some frequencies with respect to the magnitude of other (usually lower) frequencies. The key is to find the optimal preemphasis setting for the design.

For SerDes and PHY devices that support different levels of preemphasis, the SI engineer can step through the levels and select the one with the best eye or the one that achieves a BER of 10^{-12} or better. Also available are preemphasis driver ICs like the [MAX3982](#) that can be used to optimize performance by manually tuning the transmitter with respect to eye opening and ISI jitter at the receiver.

There is a slight advantage to using a discrete preemphasis IC versus one that is embedded in a SerDes/PHY device: the tester can capture an eye diagram at the receiver input with a scope and quickly see improvements in the signal quality. In simple terms, the wider the eye, the better the quality. The SI engineer should, therefore, look for the best eye opening using the least amount of preemphasis. The rule is: do not preemphasize too much. An optimal setting should provide some improvements in the channel's overall jitter performance.

Optimal Equalization

Besides adding preemphasis, you can also minimize the effects of ISI by optimizing the equalization setting at the receiver. The equalizer removes and/or overcomes the effects of high-frequency attenuation introduced on the waveform while traveling on the PCB and cable. The receiver's equalizer compensates the received signal for dielectric and skin losses in the PCB material, as well as for high-frequency loss in the cable.

In the practical and experimental sense, the effects of received equalization are difficult to evaluate when that function is embedded in a SerDes or PHY device. External receiver-equalizer ICs like the [MAX3784](#) can provide a way to quickly observe the results of receiver equalization on the scope (as opposed to BER testing for a SerDes). **Figure 14** shows the MAX3784 equalizer's input eye diagram before and after equalization at a signaling rate of 5Gbps. These measurements were made on a 40in, 6 mil trace (stripline) on FR4 PCB material.

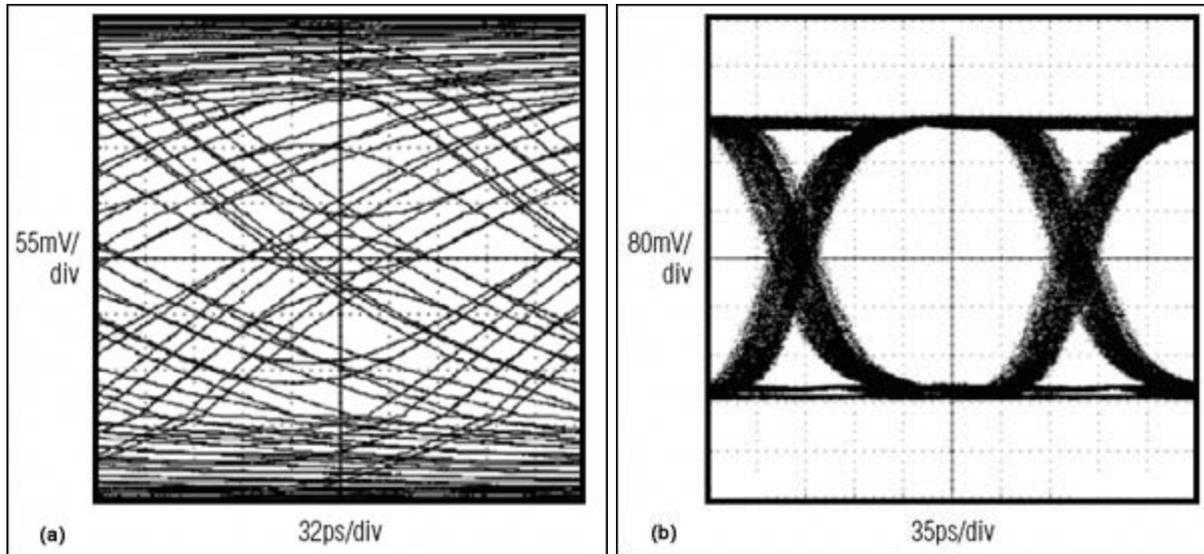


Figure 14. An eye diagram at the equalizer input before equalization (a) shows improvement after equalization (b).

Link Performance

While preemphasis at the transmitter helps to mitigate interference caused by adjacent symbols in the data, equalization at the receiver can also help to achieve a similar result, as shown in Figure 14. Preemphasis and equalization together are the main techniques today for reducing or overcoming transmission losses in serial-transmission mediums.

An important question remains: how much preemphasis and/or equalization is enough? The answer depends on the application and the channel lineup. Blindly setting the system for too much preemphasis or equalization can have negative effects on the system. The SI engineer must take signal-quality measurements to determine the proper amount of preemphasis and equalization for a given application. Maxim has a large portfolio of preemphasis and equalizer ICs for circuit board and cable applications. Devices cover the range from 1Gbps (MAX3803) to 12.5Gbps (MAX3804). For more information, refer to **Figure 15** and to www.maximintegrated.com/equalizerSolutions.

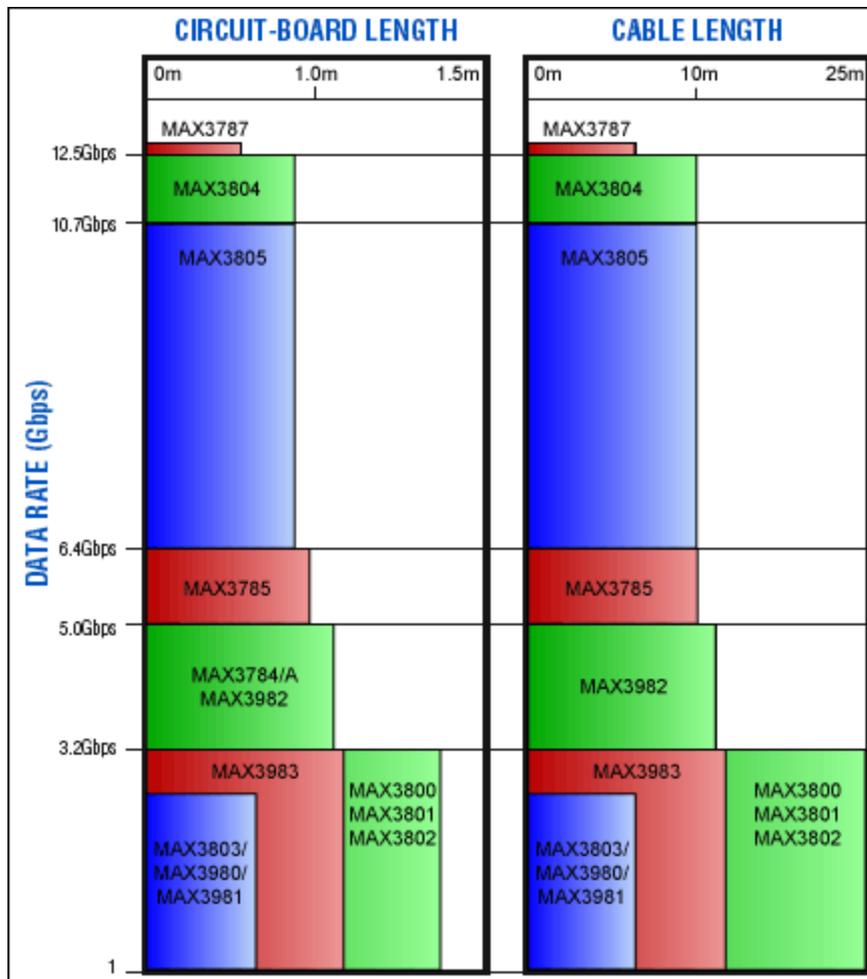


Figure 15. Guide for selecting a preemphasis/equalizer ICs are shown as a function of data rate and signal-path length, for circuit boards and cables.

Conclusion

If you design a high-speed digital system today, chances are that you will have a jitter spec or a jitter budget to meet. Understanding jitter and its causes allows you to create high-performance systems. The accurate separations of TJ into RJ and DJ, and DJ into its subcomponents (PJ, DCD, ISI), are imperative for compliance with the serial standard. Understanding jitter in its complexity is also important in providing diagnostic information for improving the design.

Designers must ensure that their designs work for reasons of competitive advantage, but they must also know the point at which their design stops working. By identifying jitter and its sources, the link-characterization framework proposed in this paper (see **Figure 16**) should help to improve system performance.

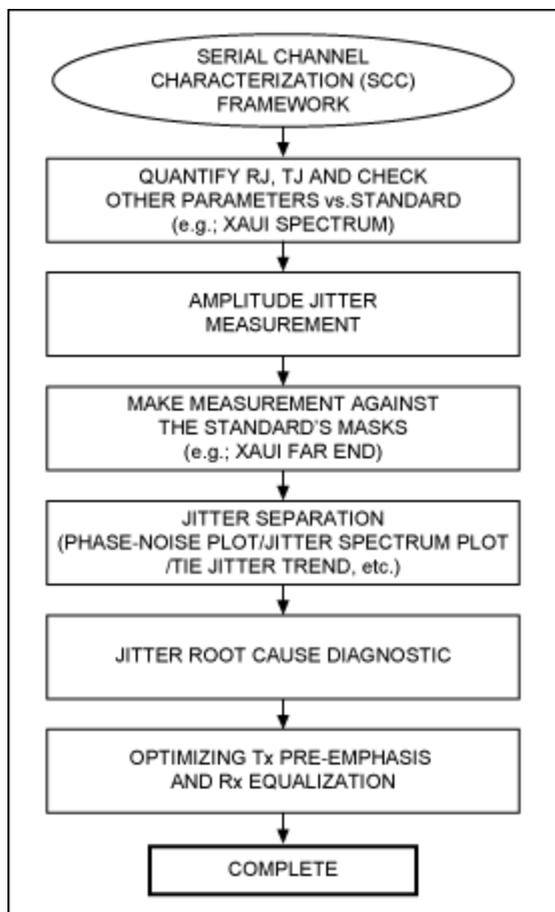


Figure 16. The proposed framework for measuring, identifying, and eliminating clock and data jitter comprises six steps.

References

¹Jitter fundamentals, "Enhance Speed, Throughput and Accuracy with One Powerful Instrument," Wavecrest: A Technologies Company, Eden Prairie, Minnesota, available at www.wavecrest.com.

²The SI engineer can control RJ by a careful selection of the components used. That approach is used to control the effect of RJ on PLL designs.

³A Guide to Understanding and Characterizing Timing Jitter, Tektronix Enabling Innovation Primer, available at www.tektronix.com/jitter.

Tektronix is a registered trademark and registered service mark of Tektronix, Inc.

Related Parts

[MAX3784](#) 5Gbps PCB Equalizer

[Free Samples](#)

[MAX3803](#) DC-Coupled, UCSP 3.125Gbps Equalizer

MAX3804	12.5Gbps Settable Receive Equalizer	Free Samples
MAX3892	+3.3V, 2.5Gbps/2.7Gbps, SDH/SONET 4:1 Serializer with Clock Synthesis	Free Samples

More Information

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APPLICATION NOTE 4613, AN4613, AN 4613, APP4613, Appnote4613, Appnote 4613

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