Add Margining Capability to a DC/DC Converter

By: Brian Vasquez
Nov 03, 2010

Abstract: You can easily add margining capability (digital adjustment of the output voltage) to a DC/DC converter by adding a 2- or 4-channel, I²C-adjustable current DAC (DS4402 or DS4404) at the converter's feedback input. Because each DAC output is 0mA at power up, the extra circuitry is essentially transparent to the system until a command is written via the I²C bus.

A similar version of this article appeared in the September 18, 2008 issue of EDN magazine.

You can easily add margining capability to a DC/DC converter (digital adjustment of the output voltage) by making a single connection to the existing circuit as shown by the dotted line in Figure 1. The extra IC is a 2- or 4-channel, I²C-adjustable current DAC (DS4402 or DS4404). Because each DAC output is 0mA at power up, the extra circuitry is essentially transparent to the system until a command is written via the I²C bus.

As an example, assume \( V_{IN} = 3V \) to 5.5V, \( V_{OUT} = 1.8V \) (the desired nominal output voltage), and \( V_{FB} = 0.6V \) (not to be confused with \( V_{REF} \) of the DS4404). You can obtain the \( V_{FB} \) value from the DC/DC converter datasheet, being sure to verify that it is within the OUTx voltage range specified in the current DAC datasheet (specified as \( V_{OUT:SINK} \) and \( V_{OUT:SOURCE} \) depending on whether you are sinking or sourcing current). It's also important to verify the input impedance of the DC/DC converter's FB pin (the circuit shown assumes a high impedance).

Assume we want to add a ±20% margining capability to the DC/DC converter output (\( V_{OUT} \)):

\[
V_{OUT\text{MAX}} = 2.16V
\]
\[ V_{\text{OUTNOM}} = 1.8V \]
\[ V_{\text{OUTMIN}} = 1.44V \]

First, determine the necessary relationship between \( R_{\text{TOP}} \) and \( R_{\text{BOTTOM}} \) that yields the nominal output (\( V_{\text{OUTNOM}} \)) when \( I_{\text{DS4404}} = 0A \):

\[ V_{\text{FB}} = V_{\text{OUTNOM}} \left( \frac{R_{\text{BOTTOM}}}{R_{\text{BOTTOM}} + R_{\text{TOP}}} \right) \]

Solving for \( R_{\text{TOP}} \),

\[ R_{\text{TOP}} = R_{\text{BOTTOM}} \left( \frac{V_{\text{OUTNOM}}}{V_{\text{FB}}} - 1 \right) \]  \hspace{1cm} (Eq. 1)

For our example,

\[ R_{\text{TOP}} = R_{\text{BOTTOM}} \left( \frac{1.8V}{0.6V} - 1 \right) = 2 \times R_{\text{BOTTOM}} \]

The current (\( I_{\text{DS4404}} \)) required to make \( V_{\text{OUT}} \) increase to \( V_{\text{OUTMAX}} \) is derived by summing currents at the FB node:

\[ I_{\text{RTOP}} = I_{\text{RBOTTOM}} + I_{\text{DS4404}} \]
\[ I_{\text{DS4404}} = I_{\text{RTOP}} - I_{\text{RBOTTOM}} \]

\[ I_{\text{RTOP}} = \left( \frac{V_{\text{OUTMAX}} - V_{\text{FB}}}{R_{\text{TOP}}} \right) \]
\[ I_{\text{RBOTTOM}} = \left( \frac{V_{\text{FB}}}{R_{\text{BOTTOM}}} \right) \]  \hspace{1cm} (Eq. 2)

\[ I_{\text{DS4404}} = \left( \frac{V_{\text{OUTMAX}} - V_{\text{FB}}}{R_{\text{TOP}}} \right) - \left( \frac{V_{\text{FB}}}{R_{\text{BOTTOM}}} \right) \]

This equation can be simplified by solving Equation 1 for \( R_{\text{BOTTOM}} \) and substituting, which yields:

\[ I_{\text{DS4404}} = \frac{V_{\text{OUTMAX}} - V_{\text{OUTNOM}}}{R_{\text{TOP}}} \]

In terms of margin percentage:

\[ I_{\text{DS4404}} = \frac{V_{\text{OUTMAX}} \times \text{MARGIN}}{R_{\text{TOP}}} \]  \hspace{1cm} (Eq. 3)

where margin = 0.2, to implement ±20% margining in this case. Before you can use this relationship to calculate \( R_{\text{TOP}} \) and \( R_{\text{BOTTOM}} \), you must select the full-scale current \( I_{\text{FS}} \).

According to the DS4404 datasheet, the full-scale current (specified as \( I_{\text{OUT:SINK}} \) or \( I_{\text{OUT:SOURCE}} \)) must be between 0.5mA and 2.0mA, to guarantee the specifications for accuracy and linearity. Unfortunately, no formula is available for calculating the ideal full-scale current. That value is influenced by the desired number of steps, the step size, and the values for \( R_{\text{TOP}} \) and \( R_{\text{BOTTOM}} \). Another factor affecting the full-scale current value would be the requirement that a particular register setting correspond to a particular margin percentage.

In any case, your selection of a full-scale current will likely require several iterations, in which you select an arbitrary value (within the range), and then calculate \( R_{\text{TOP}} \), \( R_{\text{BOTTOM}} \), \( R_{\text{FS}} \), and step size. When you've determined an acceptable full-scale current value, you may want to further adjust it (or some of the
resistor values) to ensure that the resistor values finally specified are commonly available.

To calculate $R_{TOP}$ for the original example, we choose $IFS = IDS4404$, which gives us 31 equal increments (steps) from $V_{OUTNOM}$ to $V_{OUTMAX}$, as well as 31 steps from $V_{OUTNOM}$ to $V_{OUTMIN}$. This resolution is more than adequate for our example. We could, for instance, begin by arbitrarily choosing $IFS$ in the center (1.25mA) of the specified range, and then performing all the calculations. Instead, for illustrative purposes we perform calculations for the endpoints of the range (0.5mA, 2.0mA).

So, for $IFS = IDS4404 = 0.5mA$: Using Equation 3 and solving for $R_{TOP}$,

$$R_{TOP} = \frac{V_{OUTNOM} \times MARGIN}{IDS4404} = \frac{1.8 \times 0.2}{0.5 \times 10^{-3}} = 720\Omega$$

$$R_{BOTTOM} = \frac{R_{TOP}}{2} = \frac{720}{2} = 360\Omega$$

To calculate $R_{FS}$, use the formula in the DS4404 datasheet plus the $V_{REF}$ value also found in that datasheet:

$$R_{FS} = \frac{V_{REF}}{IFS} \times \frac{31}{4} = \frac{1.23}{0.5 \times 10^{-3}} \times \frac{31}{4} = 19,065\Omega = 19k\Omega$$

$$\text{STEPSIZE} = \frac{IFS}{\text{NUMBER OF STEPS}} = \frac{0.5 \times 10^{-3}}{31} = 16.1\mu A/\text{STEP}$$

Finally, for completeness we determine the DS4404 output current as a function of register setting: $I_{OUT}(\text{register setting}) = \text{step size} \times \text{register setting}$.

Note that the register setting above does not include the sign bit, which is used to select sink or source. The DS4404 sinks current when the sign bit = 0, making $V_{OUT}$ increase to $V_{OUTMAX}$. It sources current when the sign bit = 1, making $V_{OUT}$ decrease towards $V_{OUTMIN}$.

For $IFS = IDS4404 = 2.0mA$:

$$R_{TOP} = \frac{V_{OUTNOM} \times MARGIN}{IDS4404} = \frac{1.8 \times 0.2}{2.0 \times 10^{-3}} = 180\Omega$$

$$R_{BOTTOM} = \frac{R_{TOP}}{2} = \frac{180}{2} = 90\Omega$$

$$R_{FS} = \frac{V_{REF}}{IFS} \times \frac{31}{4} = \frac{1.23}{2.0 \times 10^{-3}} \times \frac{31}{4} = 4,766\Omega = 4.7k\Omega$$

$$\text{STEPSIZE} = \frac{IFS}{\text{NUMBER OF STEPS}} = \frac{2.0 \times 10^{-3}}{31} = 64.5\mu A/\text{STEP}$$

Comparing $R_{TOP}$ and $R_{BOTTOM}$ for the two cases ($IFS = 0.5mA$ vs. $2.0mA$), you can see that $IFS = 0.5mA$ is more attractive because the resistances are higher.

<table>
<thead>
<tr>
<th>Related Parts</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DS4404</strong></td>
</tr>
</tbody>
</table>

More Information
For Technical Support: [http://www.maximintegrated.com/support](http://www.maximintegrated.com/support)