Abstract: A DS4424 adjustable-current DAC is used to adjust the margin of a DC-DC converter's output voltage. This article describes how to properly select the resistor values of a DC-DC converter's feedback divider network when the DS4424 is employed in the design.

Introduction

The DS4424 adjustable-current DAC is similar to the DS4404 adjustable-current DAC with two major differences. First, the DS4424 has 127 settings each for sink and source mode, while the DS4404 has 31 settings. Second, the DS4424's default I²C address is set to 20h, whereas the DS4404's default I²C address is 90h. Both devices' addresses are determined by the states of the A0 and A1 address pins.

This article focuses on the DS4424, which can be used to adjust the margin of a DC-DC converter's output voltage. The article explains how to properly select resistor values of the DC-DC converter's feedback divider network when the DS4424 is employed in the design.

The Adjustable Power Supply

The DS4424 contains four I²C adjustable current sources capable of sinking and sourcing current. A typical application for these DACs is margining the output voltage of a DC-DC converter (Figure 1).
Figure 1. DC-DC converter circuit with adjustable-current DACs used to margin the converter's output voltage. *VOUT and VFB values are determined by the DC-DC converter, and should not be confused with VOUT and VRFS of the DS4424.

The DS4424 sinks and sources from its OUT pins. Valid full-scale current values range from 50µA to 200µA. The value of the full-scale current, IFS, is determined by the size of the resistor connected to the DAC's FS pin of the corresponding OUT pin. The source/sink current generated by the DS4424 is commonly used to adjust the DC-DC converter's feedback voltage-divider.

Determining the Relationship Between VOUT and IFS

Choosing the right IFS depends on how much margin is desired on the DC-DC converter's VOUT pin. To determine this margin, we must discover the relationship between VOUT and IFS.

Summing currents into the VFB node, we find that:

\[ I_{RA} = I_{FS} + I_{RB} \]  \hspace{1cm} (Eq. 1)

Where:

\[ I_{RB} = \frac{V_{FB}}{R_{B}} \]  \hspace{1cm} (Eq. 2)

And:

\[ I_{RA} = \frac{V_{OUT} - V_{FB}}{R_{A}} \]  \hspace{1cm} (Eq. 3)

However, since RB and VFB are constant, there is no change in IRB. Thus:

\[ \Delta I_{RA} = \Delta I_{FS} \]  \hspace{1cm} (Eq. 4)

We are looking for the relationship between the margin on VOUT, \( \Delta V_{OUT} \), and the selected range of IFS, \( \Delta I_{FS} \). Since we know that the change in the IFS current equals the change in the current across RA, we can subtract one set of VOUT and IRA values from the other to determine the relationship between VOUT and IFS.

First, solving Equation 3 to find VOUT, we determine that:

\[ V_{OUT} = V_{FB} \cdot I_{RA} \cdot R_{A} \]  \hspace{1cm} (Eq. 5)

Use Equation 5 to create two equations. For one equation, we choose the maximum margin on VOUT, VOUTMAX, and the maximum IRA current, IRAMAX. For the other equation, we choose the nominal values for VOUT and IRA, VOUTNOM and IRANOM. Subtracting the two equations, we get:

\[ V_{OUTMAX} = V_{FB} \cdot I_{RAMAX} \cdot R_{A} \]
\[ - (V_{OUTNOM} = V_{FB} \cdot I_{RANOM} \cdot R_{A}) \]
\[ \Delta V_{OUT} = \Delta I_{RA} \cdot R_{A} \]  \hspace{1cm} (Eq. 6)

Using Equation 4, Equation 6 translates into the relationship:
\[ \Delta V_{OUT} = \Delta I_{FS} \times R_A \]  \hspace{1cm} (Eq. 7)

Equation 7 shows that the relationship between the margin on \( V_{OUT} \) and \( I_{FS} \) is determined by the value of the resistor \( R_A \).

**Calculating the Right Resistor Value for the Margin on \( V_{OUT} \)**

Now that we know the relationship between \( V_{OUT} \) and \( I_{FS} \), we can select the correct value of \( R_A \) and, thus, \( R_B \) to generate the desired margin on \( V_{OUT} \). Since the full-scale current sink/source range of the DS4424 is 50\( \mu \)A to 200\( \mu \)A, we select 100\( \mu \)A as the \( I_{FS} \) current for the DAC. To set this value, choose \( R_{FS} \) based on the following equation (also found on page 6 of the DS4424 data sheet):

\[ R_{FS} = \frac{V_{RFS}}{I_{FS}} \times \frac{127}{16} \]  \hspace{1cm} (Eq. 8)

With \( V_{RFS} = 0.976 \)V, we solve Equation 8 and find that \( R_{FS} \) needs to be 80k\( \Omega \) (77.47k\( \Omega \)) to produce a 100\( \mu \)A full-scale current.

With the DS4424 \( I_{FS} \) selected, we must determine the size of \( R_A \) to achieve the desired margin on \( V_{OUT} \). A 2.0V \( V_{OUT} \) with a 20% margin requires \( \pm 0.4 \)V of change. Sinking and sourcing the settings of the DS4424 will manage the sign. The change in \( I_{FS} \) equals the \( I_{FS} \) value of 1mA, and the desired change in \( V_{OUT} \) is 0.4V. After substituting for \( \Delta V_{OUT} \) and \( \Delta I_{FS} \) in Equation 7, we solve for \( R_A \) and get \( R_A = 4.0k\Omega \).

**Determining the Relationship Between \( R_A \) and \( R_B \)**

The feedback network of the circuit in Figure 1 is a voltage-divider with resistors \( R_A \) and \( R_B \). Looking at Figure 1 and assuming \( I_{FS} = 0 \)A, we can create a simple voltage-divider equation:

\[ V_{FB} = \frac{R_B}{R_A + R_B} \times V_{OUT} \]  \hspace{1cm} (Eq. 9)

We assume that the desired nominal value for \( V_{OUT} \) is 2.0V, and that the DC-DC converter has a feedback voltage, \( V_{FB} \), of 0.8V. Substituting the values for \( V_{OUT} \) and \( V_{FB} \), the relationship between \( R_A \) and \( R_B \) is determined to be:

\[ R_A = 1.5 \times R_B \]  \hspace{1cm} (Eq.10)

We use Equation 10 to solve for \( R_B \) and get \( R_B = 2.67k\Omega \).

**Conclusion**

The resistive-feedback-divider network and the current-sinking/sourcing capabilities of the DS4424 DACs control the margin of \( V_{OUT} \) on a DC-DC converter. The relationship between the full-scale current, \( I_{FS} \), to the margin on \( V_{OUT} \) is determined by the value of the resistor \( R_A \). By choosing the correct \( I_{FS} \) value for your application, you can determine the correct resistor values for the feedback divider network, and achieve the desired margin on \( V_{OUT} \).

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