

Keywords: Simultaneous Sampling, Phase delay, 24 bit Sigma Delta, 3 phase power monitoring, cascade 8 devices, up to 32 channels, FAULT, OVERFLOW

## APPLICATION NOTE 4272

# Overview of the MAX11040K 24-Bit Simultaneous-Sampling, Sigma-Delta ADC

By: Sohail Mirza, Application Manager  
 Sep 25, 2008

*Abstract: This application note highlights the key features of the MAX11040K simultaneous-sampling sigma-delta ADC. The article will discuss 4-channel simultaneous sampling; the ability to program phase delays individually for each channel; cascading up to eight devices; and the operation of the active-low FAULT and OVERFLOW signals. Example test data, generated with device's evaluation (EV) kit, will be shown.*

## Four-Channel Simultaneous Sampling

The **MAX11040K** integrates four 24-bit, sigma-delta ADCs to enable 4-channel simultaneous sampling. Unlike multiplexed-channel sigma-delta ADCs that do not maintain phase integrity, the MAX11040K not only records the phase information but also allows the user to program phase on individual channels.

**Figure 1** shows same analog signal applied (zero phase delay) to all four ADC inputs, and the resulting sampled data.

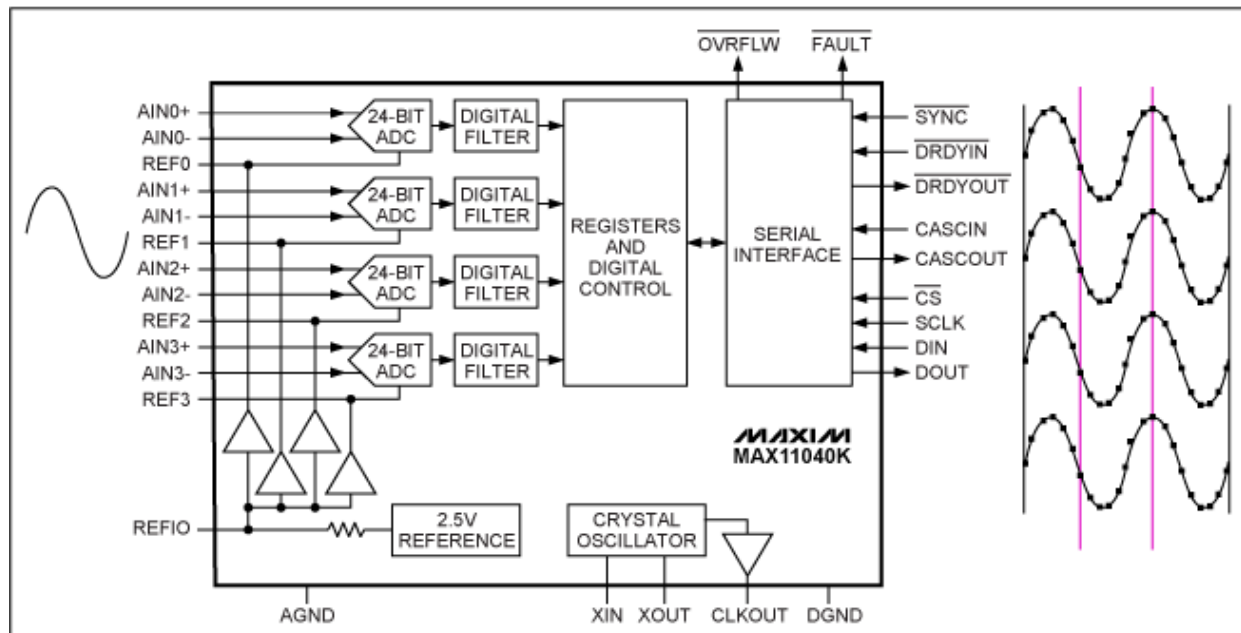


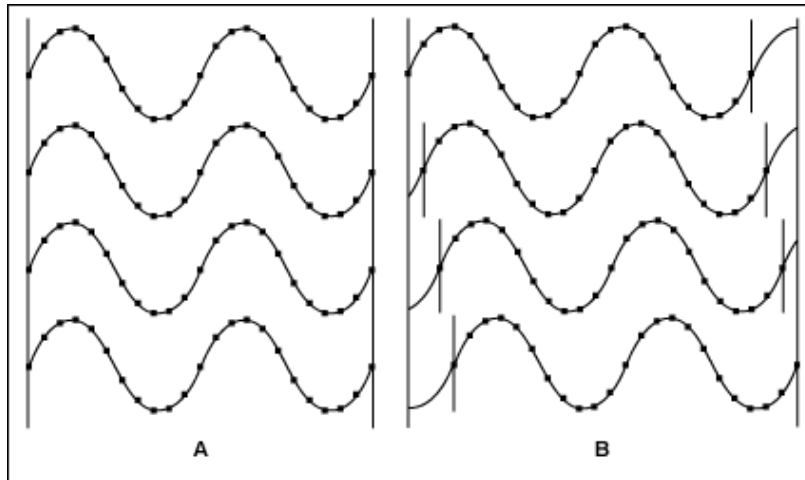
Figure 1. The same sine-wave signal was applied to the four inputs of the MAX11040K. Simultaneous outputs

are shown at right.

## Individual Phase-Delay Programming for Each Channel

Users can independently program phase delay for each ADC channel with a maximum of 333 $\mu$ s delay in 1.33 $\mu$ s steps. By programming phase delays into the ADC channels, the users can null out inherent phase delays caused by filters, delay lines, etc., in their signal path. The delay step size is also smaller than the data rate, thus allowing the user a resolution not available after acquisition.

**Figure 2** shows the sampled output when zero phase delay is programmed and when varying phase delays are programmed. In both cases, all four inputs are tied to the same signal source.



*Figure 2. The same sine-wave signal was applied to the four inputs of the MAX11040K. Figure 2A shows the simultaneous output from the four channels when zero phase delay was programmed. Figure 2B shows the simultaneous output from the four channels when varying phase delays were programmed.*

## Cascade up to 8 Devices

If four channels are not sufficient for an application, one can cascade up to eight MAX11040K devices together to enable 32 channels of simultaneous sampling. This feature is ideal for applications such as EEG that requires multiple simultaneous sampling channels for brain-wave monitoring.

**Figure 3** shows the device setup.

- The active-low CASCOUT signal from the first device is fed into active-low CASCIN of the second device. The setup is similar for the second device to the third and following devices. Finally, active-low DRDYOUT from the last device signals that the data is ready from all devices.
- The CLKOUT signal from the first device is fed into the XIN of all the other devices.
- Active-low FAULT and active-low OVRFLW are in a wired-OR arrangement.

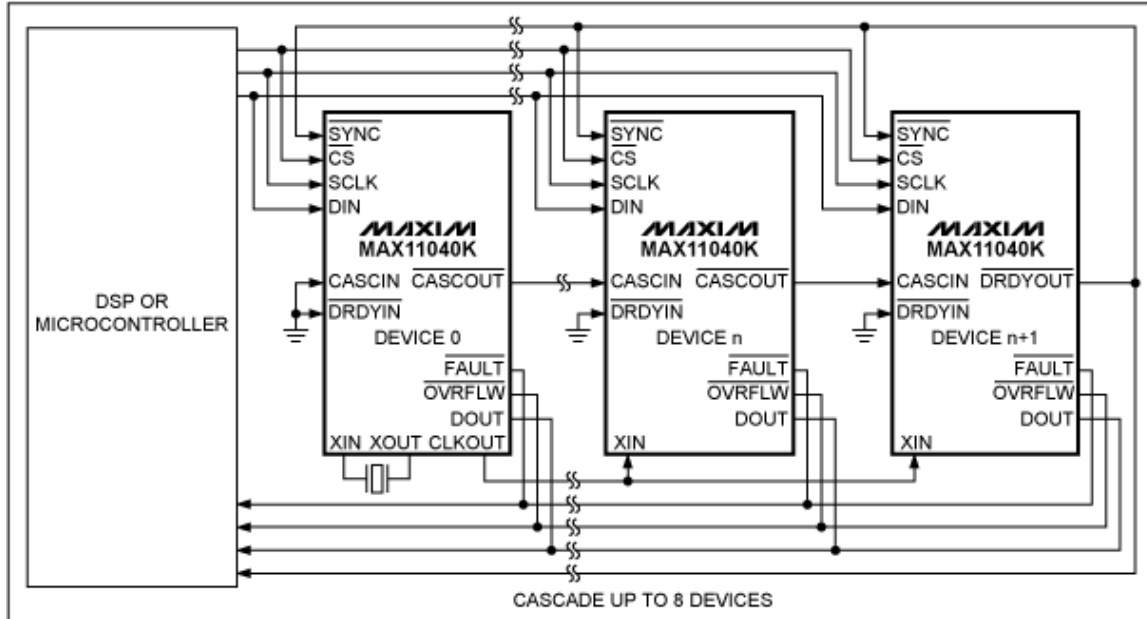


Figure 3. Diagram of the setup for cascading up to 8 MAX11040K devices.

## FAULT and OVERFLOW Signals

The MAX11040K generates active-low OVERFLOW and active-low FAULT signals whenever the input goes above  $\pm 0.88\%$  of  $V_{REF}$  or above 6V, respectively. This feature is important for generating an alarm on saturation or if the application needs overvoltage (OV) protection.

**Figure 4** illustrates the process for a fast-moving input; **Figure 5** illustrates the process for a slow-moving input. For the fast signals, the transition on the active-low OVERFLOW and FAULT signals is almost simultaneous. One should note that there is a latent period from when the signal crosses the threshold and before the active-low OVERFLOW and FAULT signals go low. There is a similar recovery time before the signals return high.

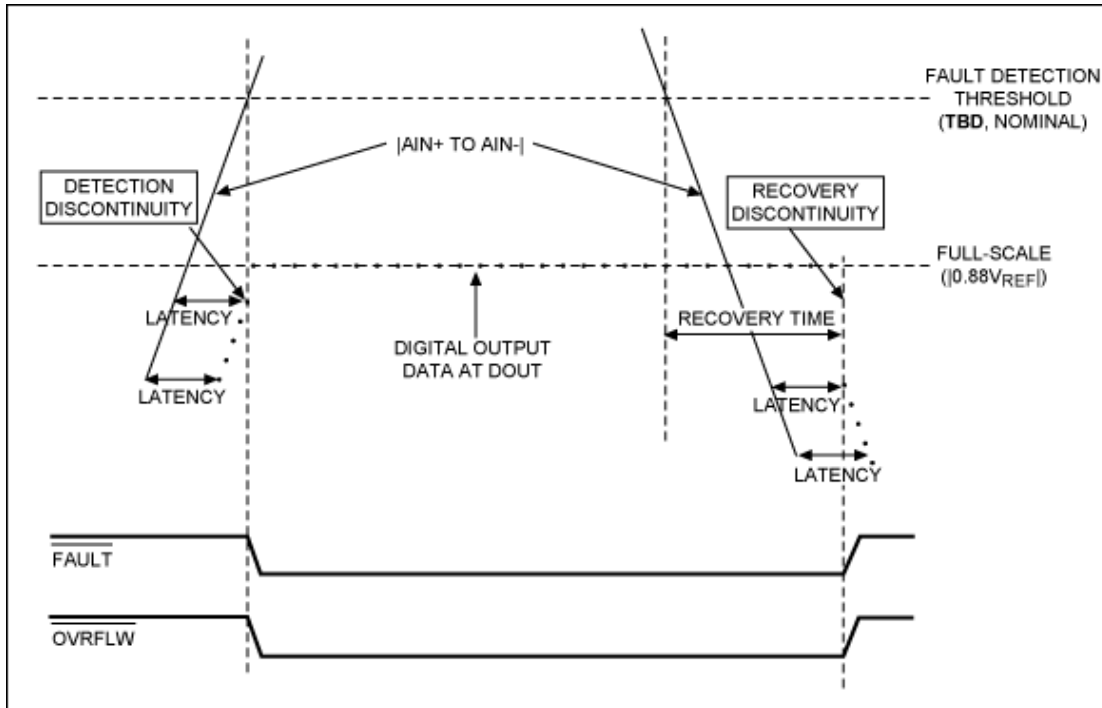


Figure 4. High-frequency analog input OV detection and recovery for a fast-moving input.

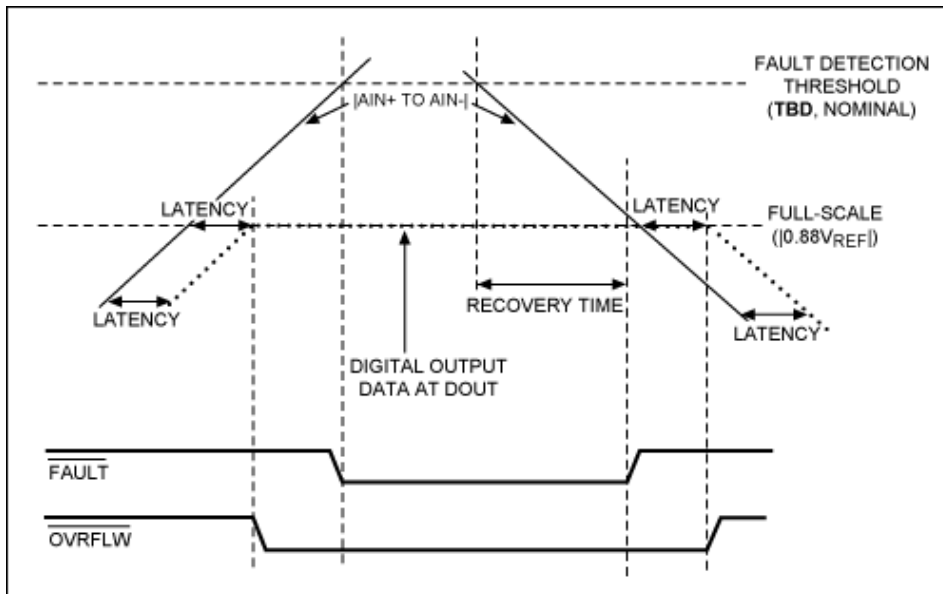


Figure 5. High-frequency analog input OV detection and recovery for a slow-moving input.

## Example Data

The following example data was generated with the MAX11040K EV kit.

### Simultaneous Sampling, Programmable Phase Delay, and Cascadable Device Setup

Figure 6 shows the block diagram of two ADCs. The settings were programmed for various phase delays. An AC signal of  $4V_{p-p}$  running at 120Hz was provided to the 8 inputs (four inputs for each device). The phase

delay for each channel was programmed with the following codes:

CH1	0	0	0 $\mu$ s
CH2	36	36	46.88 $\mu$ s
CH3	2 $\times$ 36	72	93.75 $\mu$ s
CH4	3 $\times$ 36	108	140.62 $\mu$ s
CH1	4 $\times$ 36	144	187.50 $\mu$ s
CH2	5 $\times$ 36	180	234.38 $\mu$ s
CH3	6 $\times$ 36	216	281.25 $\mu$ s
CH4	7 $\times$ 36	252	328.12 $\mu$ s

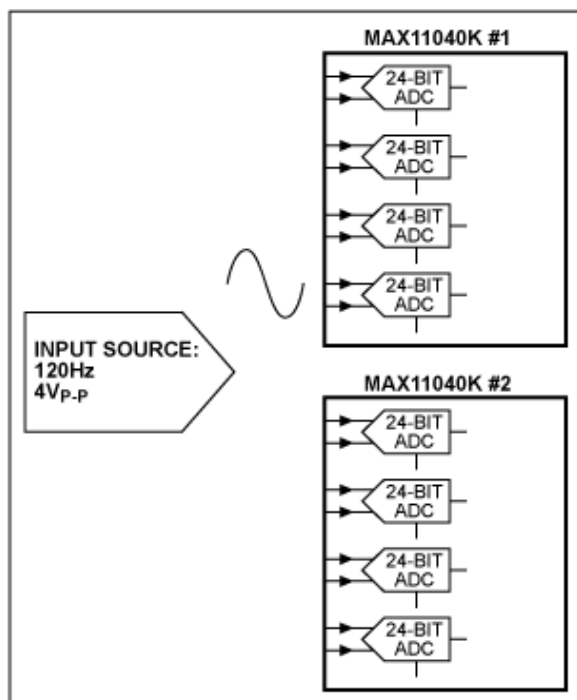
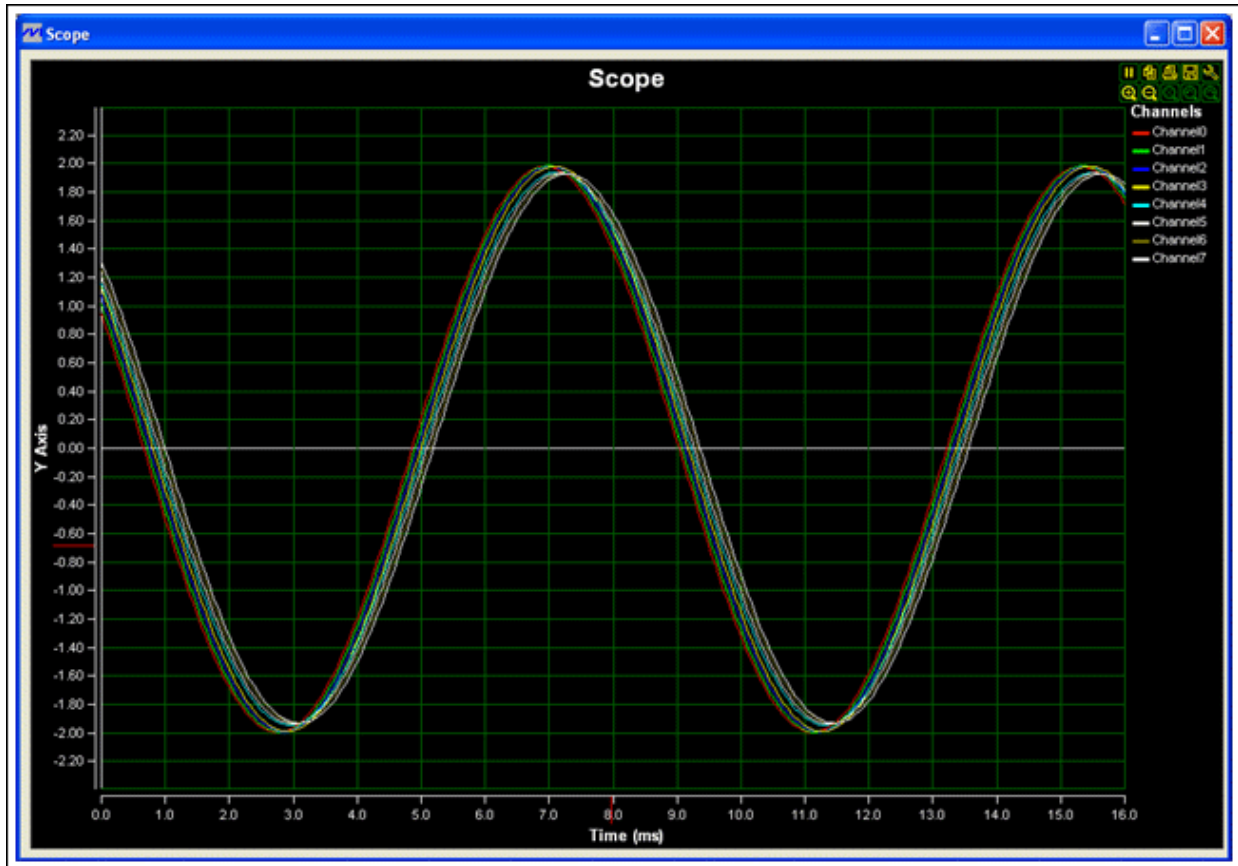


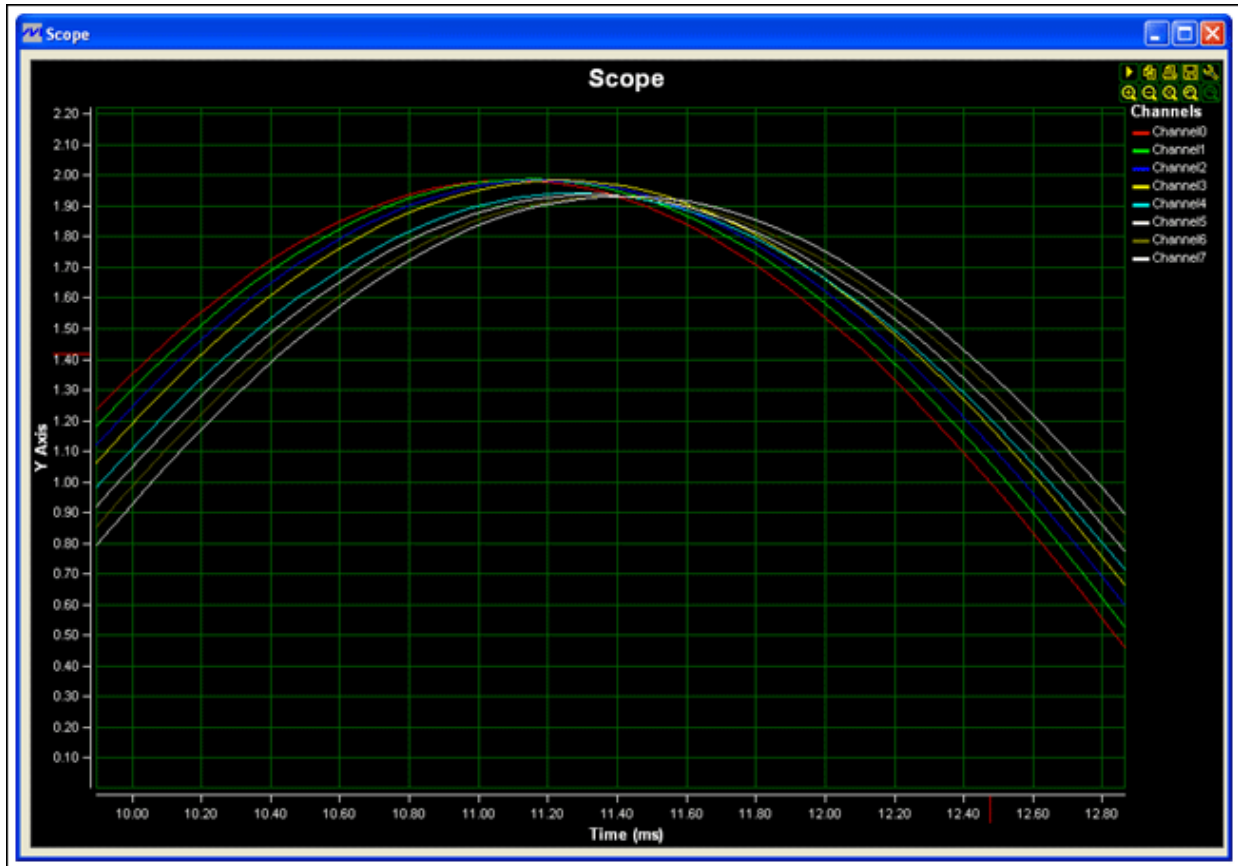
Figure 6. Two MAX11040K ADCs are shown with the various phase delays applied to the signal.

Figures 7 and 8 show the captured data from the two MAX11040K devices in Figure 6. One can see that, although the same signal was applied to all the inputs, the resulting waveform is out of phase due to the programmed phase delay.



[More detailed image \(PDF, 279KB\)](#)

Figure 7. The data that resulted from the dual ADC setup in Figure 6.



[More detailed image \(PDF, 269KB\)](#)

Figure 8. A zoomed-in view of Figure 7.

### Fault and Overflow Detection (Application Assistance)

If a designer wants to use active-low OVERFLOW or active-low FAULT as interrupt signals, then either an external D flip flop or an internal latch is needed in the hardware. The signals will become latched when the active-low OVERFLOW or active-low FAULT goes low on the active-low SD pin. The interrupt controller can reset the signals by driving the active-low RD pin low (Figure 9).

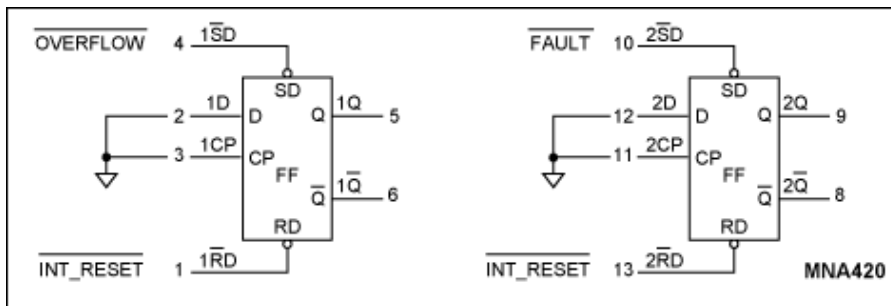
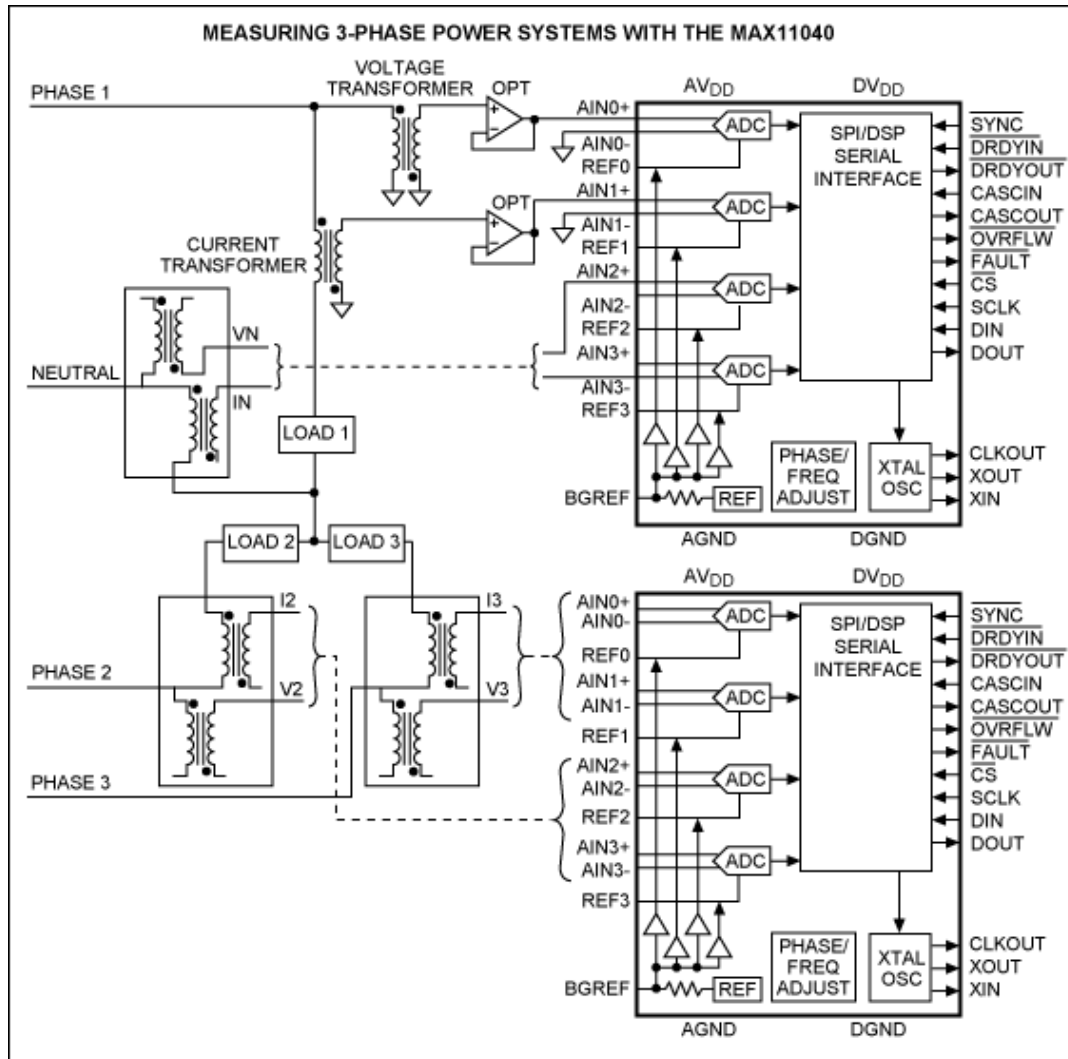


Figure 9. Latching OVERFLOW or FAULT signals.

With all the key features mentioned, MAX11040K is an ideal candidate for:

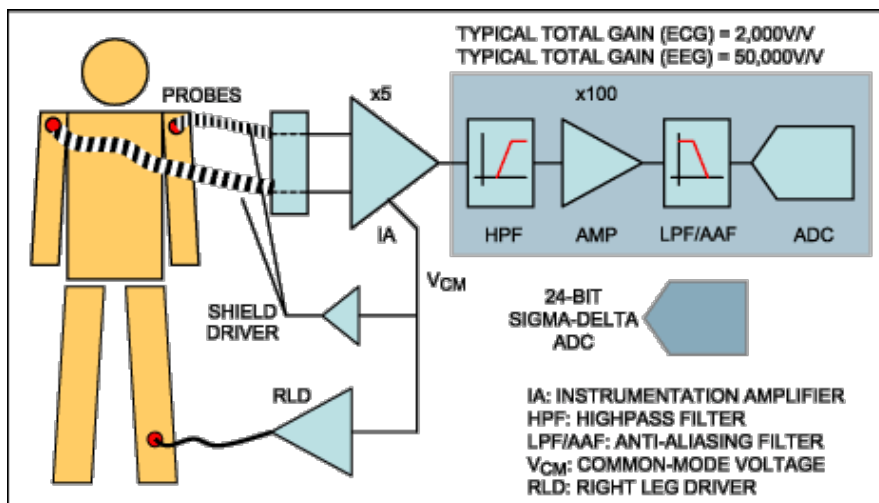
- Three phase plus neutral lines for power measurement and monitoring**  
 By using voltage and current transformers to bring down the voltage to acceptable levels, two MAX11040Ks can be cascaded to monitor three phases plus a neutral voltage and current signals. Although a sigma-delta ADC with 24-bit accuracy, the MAX11040K has sufficient sampling rates to

monitor greater than 24 harmonics (industry standard). With ENOB of nearly 18, electrical noise as well as large transients can be captured to help determine the quality of power. Phase shifts that can create offsets in your power-factor calculations can easily be compensated by programming phase delays. At the same time OVERFLOW and FAULT can be easily detected and captured.



- EEG/EKG signal monitoring





With a high dynamic range, a second gain stage can be eliminated to reduce component count and cost, and improve reliability. Having a sigma-delta architecture with a fifth-order modulator, the MAX11040K provides excellent noise performance compared to SAR and other architectures. It also provides 32 channels with phase adjust to monitor many parts of the brain simultaneously.

#### Related Parts

[MAX11040K](#)

24-/16-Bit, 4-Channel, Simultaneous-Sampling, Cascadable, Sigma-Delta ADCs

[Free Samples](#)

#### More Information

For Technical Support: <http://www.maximintegrated.com/support>

For Samples: <http://www.maximintegrated.com/samples>

Other Questions and Comments: <http://www.maximintegrated.com/contact>

Application Note 4272: <http://www.maximintegrated.com/an4272>

APPLICATION NOTE 4272, AN4272, AN 4272, APP4272, Appnote4272, Appnote 4272

Copyright © by Maxim Integrated Products

Additional Legal Notices: <http://www.maximintegrated.com/legal>