Keywords: transmission line, line impedance, high-speed signal, lossless, lossy, transmission path, source impedance, load, printed circuit board, PCB, micro-strip, coaxial, twisted pair, TDR, Time Domain Reflectometry

APPLICATION NOTE 4168

Interfacing High-Speed Signals

Feb 19, 2008

Abstract: With the world of high-speed signals becoming the norm, there is a greater need to ensure that these signals interface correctly to maintain timing and fidelity. Rise times commonly are in the sub-nanosecond range, and propagation delays are in the nanosecond range. Accurate timing is becoming more critical and cannot be achieved without rigorously analyzing the signal path.

Introduction

The purpose of this article is not to derive the transmission line equations that show why the results of the following case studies occur, but to assume and utilize them where necessary. This article applies transmission-line theories in real cases, shows the results that can occur, and recommends solutions to avoid common pitfalls. A typical high-speed path, in its basic form, is shown in **Figure 1**. The types of problems that can occur in high-speed signal paths are:

- Unwanted oscillations
- Ringing of the waveform
- Overshoot and undershoot
- Unwanted edge effects on the rising and falling edges of a waveform

All of the above effects degrade the signal path by introducing a multitude of timing and, in some cases, DC errors. These errors can be avoided by optimizing the signal path, as will be demonstrated in the following case studies.

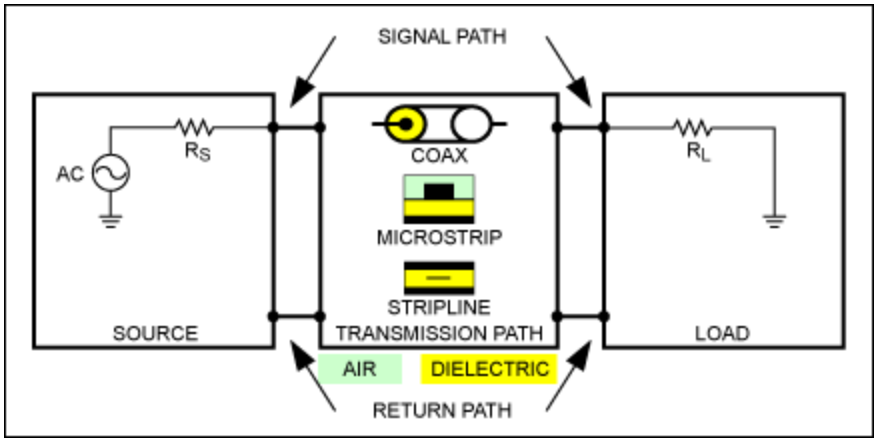

Figure 1. Simple high-speed transmission line.

Figure 1 illustrates a circuit whose source and load impedances are resistive. For the following case studies, we shall keep them resistive in order to keep the analysis simple. The characteristic impedance of the transmission line is normally defined as Z_O. In an ideal world, $R_S = Z_O = R_L$. For these same case studies, we use an impedance of 50Ω. Any impedance can be used in the analysis with similar outcomes.

Basic Transmission-Line Theory

There are two basic simplified circuits for transmission lines.

1. Lossless Transmission Line

   Figure 2 shows a lossless transmission line. It is lossless, because there are no resistive elements that create losses.

   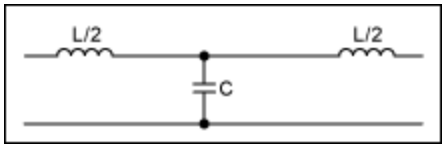

   Figure 2. Lossless transmission line.

   There are four impedances that define lossless and lossy transmission lines.
   - L = characteristic inductance per unit length
   - C = characteristic capacitance per unit length
   - R = characteristic resistance per unit length
   - G = characteristic conductance per unit length

2. Lossy Transmission Line

   If $R << j\omega L$ and $G << j\omega C$, then we can ignore the lossy terms of R and G. This is the assumption that is made in **Figure 3** and, hence, we only need to refer to Figure 2.

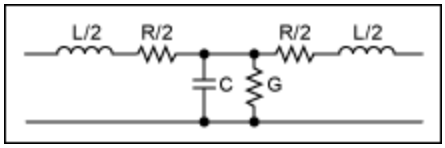

Figure 3. Lossy transmission line.

There are two fundamental characteristics that define the transmission line in Figure 2.

1. Characteristic impedance (Z_O), where:

   $Z_O = \sqrt{\frac{L}{C}}$; Note: This is a real number.

2. Propagation time (τ), where:

   $\tau = \sqrt{L \times C}$

Typical Line Impedances

Table 1 gives some typical impedances and propagation delays for some common wire setups.

Table 1. Typical Characteristics of Line Impedances

Type of Line	Z_O (Ω)	L (nH/in)	C (pF/in)	τ (ns/ft)
Single wire, well above ground	575	50.8	0.152	1.05
Micro-strip on FR4 board 1. W = 1.5mm, T = 0.035mm, H = 0.794mm 2. W = 2.3mm, T = 0.035mm, H = 0.794mm 3. W = 0.7mm, T = 0.035mm, H = 0.794mm	 50.71 36.09 76	 7.17 4.71 10.45	 2.79 4.05 1.81	 1.65 1.65 1.65
Twisted pair	100	7.5	0.75	2.3
Coaxial	50	6.35	2.54	1.52

Transmission Reflections

Now we want to investigate the effects of this signal path on our signal fidelity by looking at three fundamental impedances.

1. **R_S** = Source impedance of our driving source. This can vary depending on the application. R_S can be 50Ω for some applications and 75Ω for others; if it is driven directly from buffers that have feedback paths, it could be in the tens of ohms or lower. They also can be of the order of kilohms when the outputs come from CMOS buffers.
2. **Z_O** = Impedance of the signal path or transmission line. This signal path can also vary, depending on whether we choose a single wire, a coaxial, micro-strip, or strip-line. The signal path also has another parameter that is of great importance, which is the time it takes the signal to travel the full path (τ).
3. **R_L** = Load. This is our load. It is resistive in the following case studies, and it can vary depending on the application.

All three of these impedance parameters affect the signal in different ways. Their effects will be analyzed using the setup shown **Figure 4**. This setup is the basic circuit used for all of the case studies.

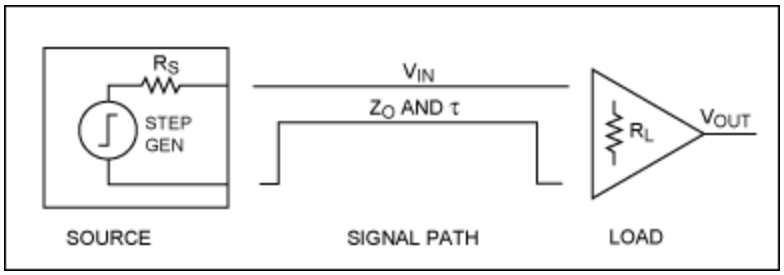

Figure 4. Test schematic.

There are two reflections that can occur in a setup like the one in Figure 4. One of these is the source-reflection coefficient (SRC) or interaction of R_S with Z_O, and the second is the load-reflection coefficient (LRC) or interaction of Z_O with R_L. Each of these reflection coefficients represents the fraction of the voltage that is reflected and is defined as follows:

$$\text{SRC} = \Gamma_S = \frac{R_S - Z_O}{R_S + Z_O}$$

and

$$\text{LRC} = \Gamma_L = \frac{R_L - Z_O}{R_L + Z_O}$$

Case Studies

The following four case studies refer to the setup in Figure 4. The only parameters that change are R_S, Z_O, and R_L.

Case 1 (R_S = 0Ω, R_L = ∞, Z_O = 50Ω, τ = 2.5ns)

A real-life example of a case with specifications close to these is a low-impedance buffer driving an ECL input.

The generator in Figure 4 supplies a stepped pulse of amplitude 1V and a rise time (t_r) of 500ps. The simulated plot of V_{OUT} with the above impedances is shown in **Figure 5**.

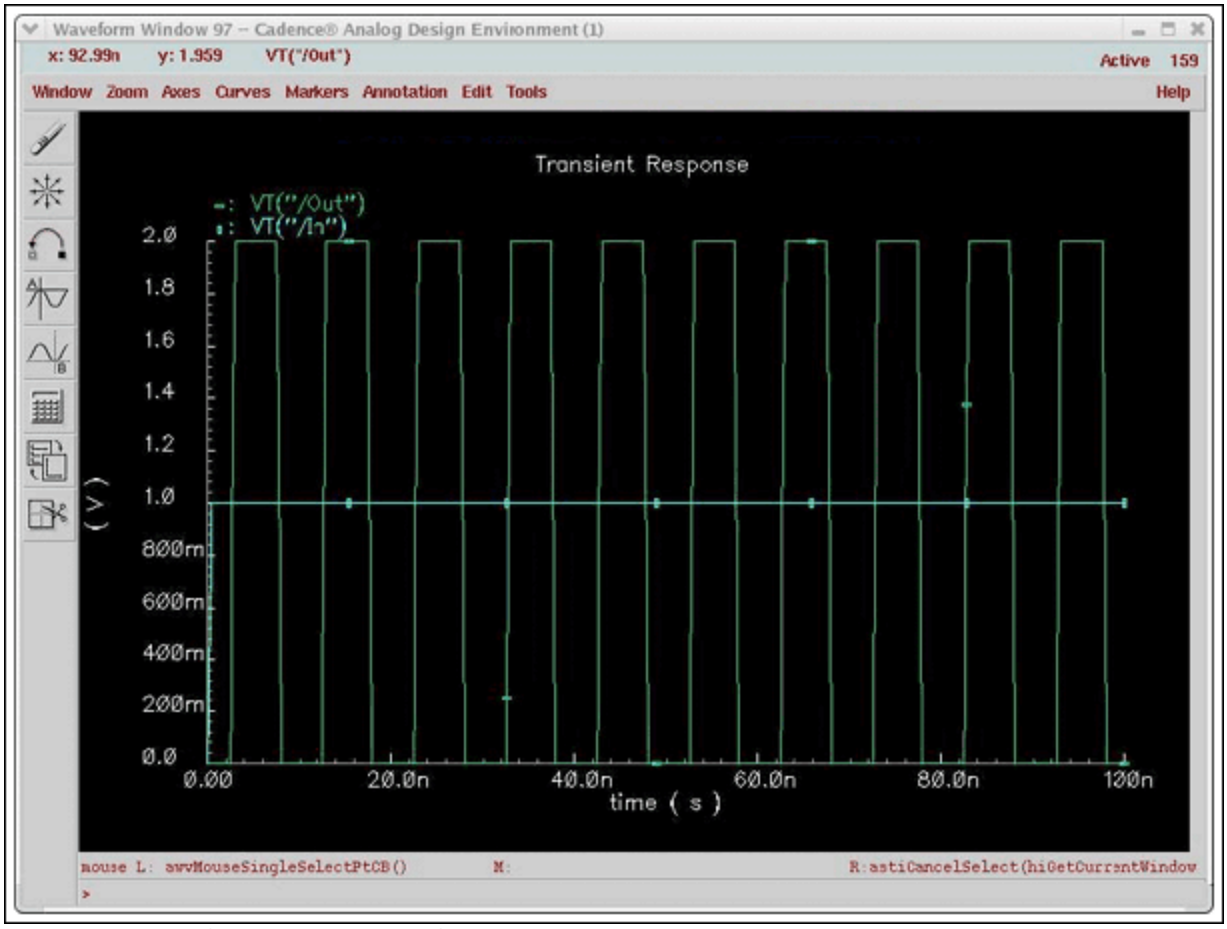

Figure 5. R_S = 0Ω, R_L = ∞, Z_O = 50Ω, τ = 2.5ns.

The problem that occurs with this setup is a full oscillation at the output node V_{OUT}. This case is somewhat unrealistic, as we normally would not drive a transmission line with zero impedance, nor have a load that is infinite. However, it serves the purpose of dramatically showing the problems that will begin to occur if impedances similar to these are being used.

Case 2 (R_S = 10Ω, R_L = 10kΩ, Z_O = 50Ω, τ = 2.5ns)

Case 2 is a little more realistic in that it shows the use of a low-impedance buffer, 10Ω in this case, driving a 50Ω transmission line with a high-impedance load. The results are shown in **Figure 6**. As can be seen in the plot, the well-known problem of ringing is observed on the output node, V_{OUT}; the ringing finally subsides.

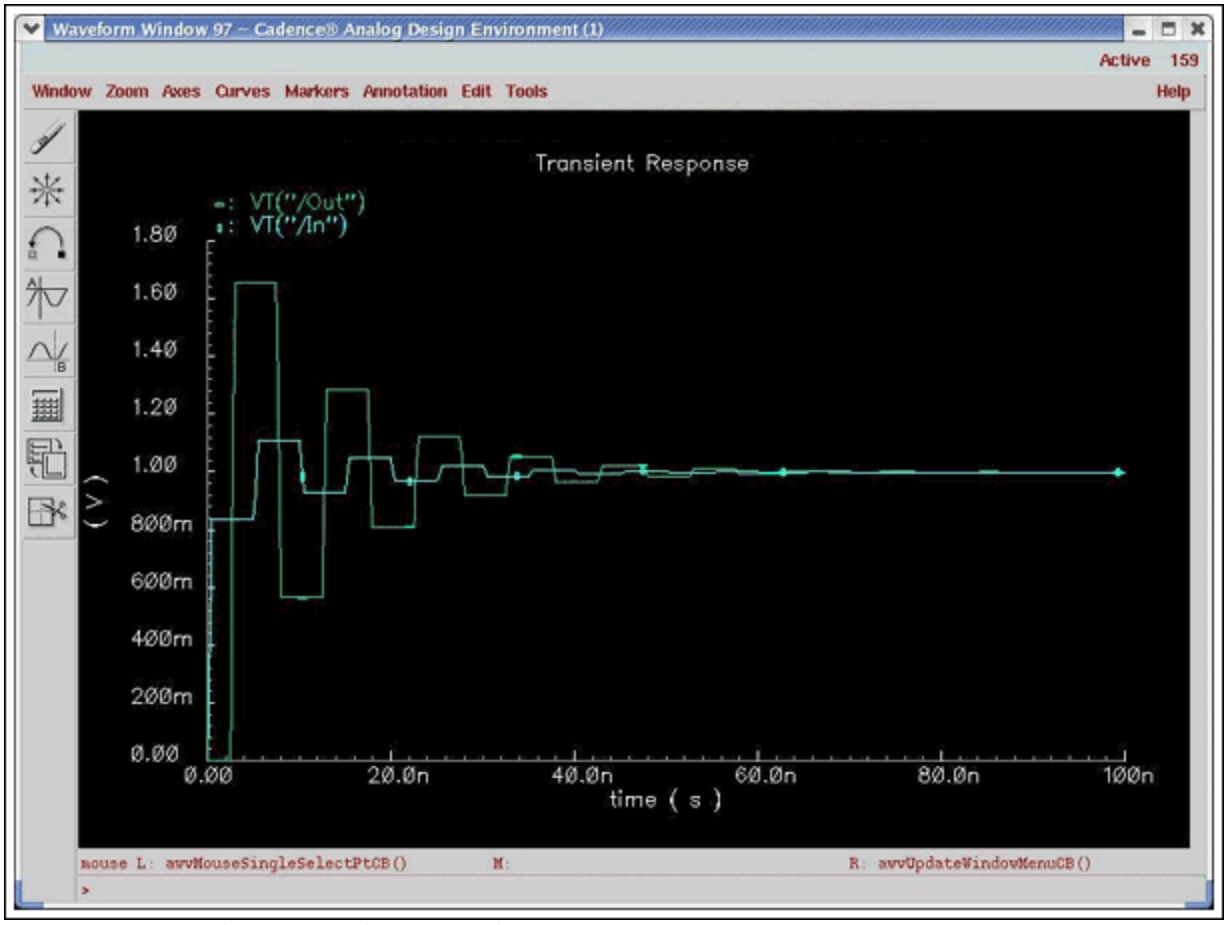

Figure 6. R_S = 10Ω, R_L = 10kΩ, Z_O = 50Ω, τ = 2.5ns.

Case 3 (R_S = 30Ω, R_L = 500Ω, Z_O = 50Ω, τ = 2.5ns)

Case 3 is very similar to some typical setups. Here, the input buffer has an impedance of 30Ω, the transmission line is 50Ω, and the load is 500Ω. It is still the same test setup as in Cases 1 and 2, but the oscillations and/or ringing are dampened considerably. What we see in the **Figure 7** plot is the classic overshoot and undershoot of the output waveform at the V_{OUT} node.

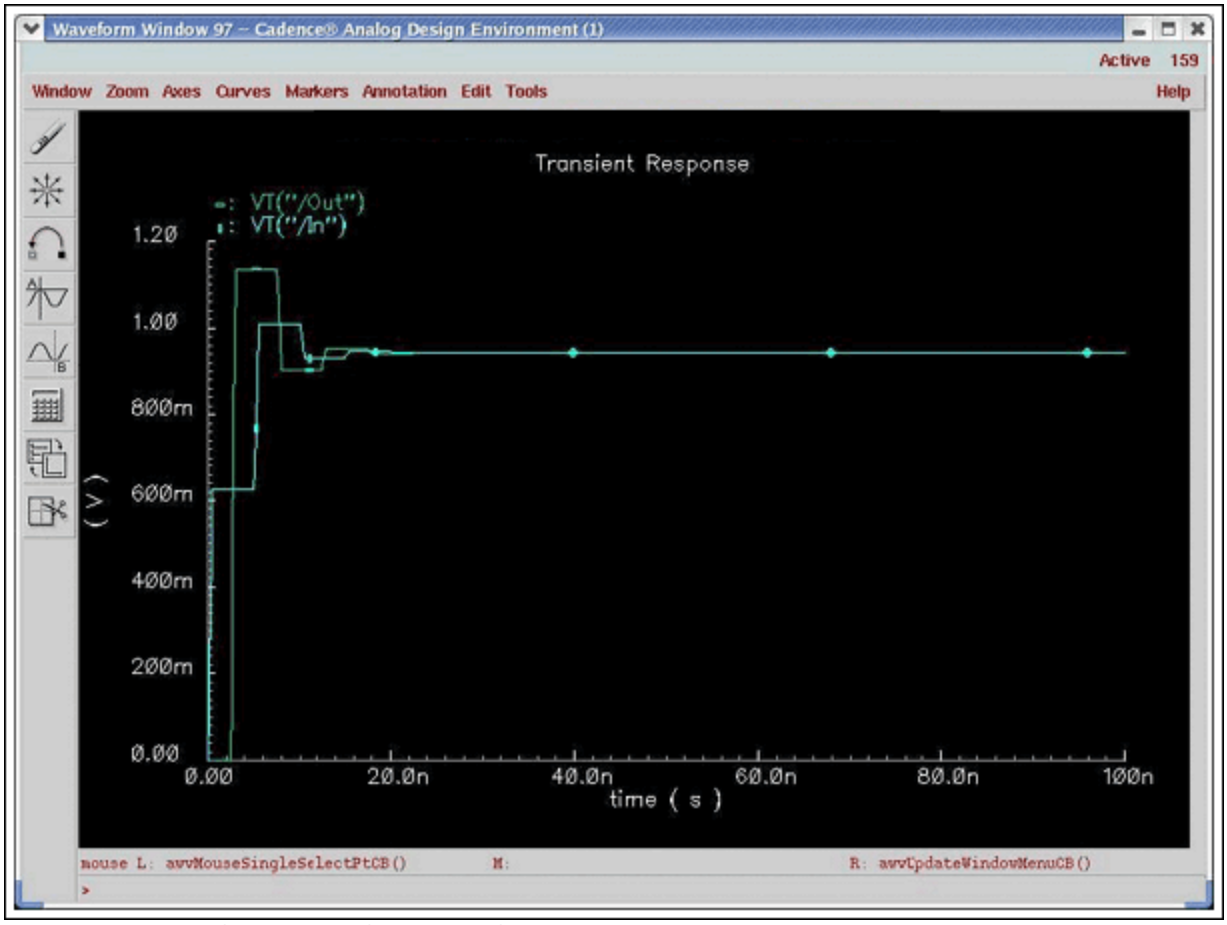

Figure 7. R_S = 30Ω, R_L = 500Ω, Z_O = 50Ω, τ = 2.5ns.

Case 4 (R_S = 50Ω, R_L = 50Ω, Z_O = 50Ω, τ = 2.5ns)

Finally, Case 4 illustrates the idea of matching the input to the transmission line and also matching the transmission line to the output. **Figure 8** shows the desired waveform that we expect at the V_{OUT} node. There are no oscillations, ringing, or overshoots.

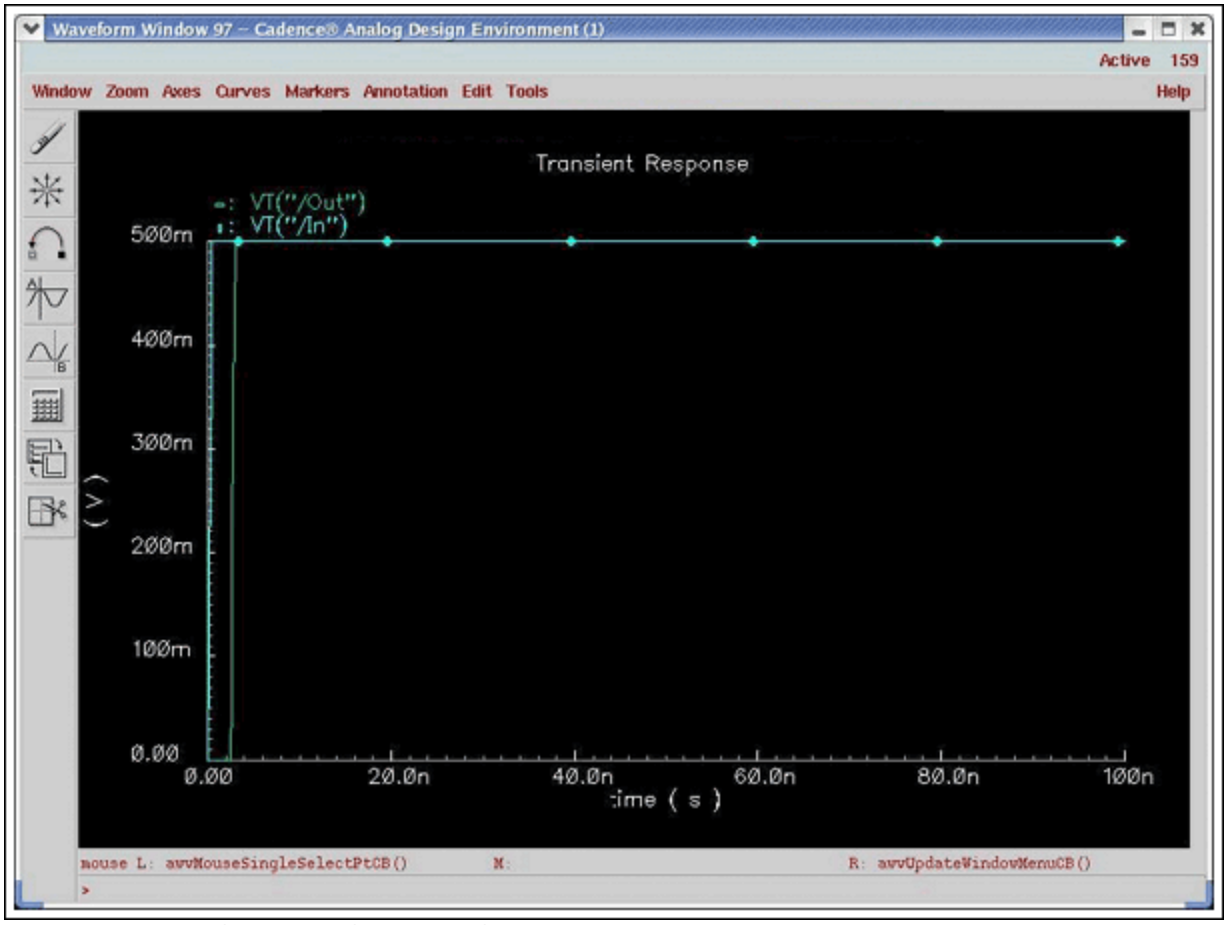

Figure 8. R_S = 50Ω, R_L = 50Ω, Z_O = 50Ω, τ = 2.5ns.

Discussion of Case Results

1. The four cases discussed represent a simple subset of many possible cases that can create problems similar to that seen above. It is obvious that we should match the source, transmission line, and the load for the best results. However, matching these can be more difficult than the above cases suggest. Some of the areas that need to be looked at carefully are:
    a. **Source** This source needs to have its impedance matched as well as possible over a large bandwidth, and this is not always feasible. Also, our source could already have artifacts on its edges such as ringing, overshoots, undershoots, drooping, and so on that further complicate the matching.
    b. **Transmission Line** This line is usually a printed circuit board (PCB) trace, long coaxial cable, simple wire, or twisted-pair cable. The modeling of this path is not always as simple as having impedances of 50Ω. It can have a complex distribution of impedances, and can be further complicated by the actual geometry of the trace itself.
    c. **Load** The load is not always a simple resistive load. This load has more complex impedances attached to it, which also need to be considered. The addition of connectors further complicates the load.
2. Not matching the source, signal path, and load carefully can lead to problems from full oscillations, or bad ringing effects, at the output. These problems are shown very clearly in Figures 5, 6, and 7.
3. The four cases also show that we can reduce or eliminate the ringing problem that was highlighted. For these cases, it was effective to simply add more impedance to the output of the low impedance

source to increase its output impedance, making it closer to the desired impedances of 50Ω. Terminating the high impedance load was also effective for obtaining impedances of 50Ω.

4. It is important to realize that ringing and artifacts on the pulse edges can modify waveforms, which can greatly affect system performance. These artifacts, in particular, can cause incorrect triggering if applied to the inputs of comparators. The artifacts can also increase delays in the signal path. Optimizing the signal path helps to reduce these unwanted effects.

Analyzing and Verifying the Results

Bounce Diagram

Theoretically, you can draw out what is commonly known as a "bounce" diagram to verify the above results for all the cases above. This is a useful exercise to get a better understanding of how these signals appear at the output. Using bounce diagrams can be useful, but require quite a bit of time and can be very difficult to use once we make the circuit more complex. The easiest approach is the SPICE approach suggested in the following *Simulation* section. The four cases were simulated using one of the many SPICE simulators.

Simulation

The fastest approach to optimizing a signal path is the use of a SPICE type of simulator. The circuit can be as simple as that shown in Figure 4. It is important to keep the following points in mind.

1. Use an accurate model of the source, as depicted in Figure 4. Only the output section of the source needs to be modeled. This model should show the series resistance, series inductance, and shunt capacitance.
2. The transmission line depicted in Figure 4, whether it be a PCB trace, coaxial cable, twisted pair cable, etc., also need to be accurately modeled.
3. Finally, the Figure 4 load must also be modeled precisely to reflect the resistance, inductance, and shunt capacitance.

A good tool to model the source, transmission line, and load is time domain reflectometry (TDR). The use of TDR allows you to measure the R, L, and C components so that you can build a more accurate model.

Summary

It can easily be seen that signal degradation occurs when we fail to carefully match the entire signal path of the source, transmission line, and load. This has been demonstrated in the four cases discussed above. If we do not achieve this matching, then we can expect unforeseen errors. It is also shown that the use of a SPICE type of simulator, with its simplified modeling approach, can show the problems quickly. With this information, solutions can be designed and verified rapidly as well.

As frequencies get higher and higher, it becomes very apparent that a great deal of effort must be placed on modeling and simulating the entire signal path. This will ensure the most accurate and predictable results.

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