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TUTORIAL 4083

Thermal Characterization of IC Packages

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Abstract: Thermal characterization of packages is critical for the performance and reliability of IC applications. This article describes the standard thermal package properties: thermal resistance (known as "theta" or Θ), Θ_{JA} , Θ_{JC} , and Θ_{CA} . Thermal calculations and references for more information on thermal management are provided.

Introduction

Thermal management should be considered during package selection to ensure high product reliability. All ICs generate heat when power is applied to them. Therefore, to maintain the device's junction temperature below the maximum allowed, effective heat flow from the IC through the package to the ambient is essential. This article helps designers and customers understand basic IC thermal-management concepts. In discussing package heat transfer, it defines important terms for thermal characterization, which begin with thermal resistance and its various "theta" representations. The article also provides thermal calculations and data to ensure proper junction (die), case (package), and board temperature.

The Importance of Thermal Resistance

Thermal management of semiconductors involves thermal resistance, which is an important figure of merit describing the heat transfer properties of material. In calculations, thermal resistance is identified as "Theta," derived from the Greek word for heat, "thermos." It is thermal resistance that particularly interests us.

The thermal resistance of an IC package is the measure of the package's ability to transfer heat generated by the IC (die) to the circuit board or the ambient. Given the temperatures at two points, the amount of heat flow from one point to the other is completely determined by the thermal resistance. By knowing the thermal resistance of a package, one can calculate the IC's junction temperature for a given power dissipation and its reference temperature.

The Maxim website ([Manufacturing](#), [Layout](#), [Production](#), [QA/Reliability](#), [Procurement](#)) provides information about commonly used thermal-resistance values for ICs.

Definitions

The following section defines Theta (Θ) and Psi (Ψ), standard terms used in thermal characterization of IC packages.

Θ_{JA} is the thermal resistance from junction to ambient, measured as °C/W. Ambient is regarded as thermal "ground." Θ_{JA} depends on the package, board, airflow, radiation, and system characteristics. Generally, the effects of radiation are negligible. Θ_{JA} values are listed for natural convection conditions (no forced air) only.

Θ_{JC} is the thermal resistance from junction to case. Case is a specified point on the outside surface of the package. Θ_{JC} depends on the package materials (the lead frame, mold compound, die attach adhesive) and on the specific package design (die thickness, exposed pad, internal thermal vias, and thermal conductivity of the metals used).

For leaded packages, the Θ_{JC} reference point on the case is where pin 1 emerges from the plastic. For standard plastic packages, Θ_{JC} is measured at the corner of pin 1. It is measured at the center of the exposed-pad surface for exposed-pad packages. The Θ_{JC} measurement is done by attaching the package directly to an "infinite heat sink," usually a liquid-cooled copper block which can absorb any amount of heat flow with no thermal resistance. The measurement represents the transfer of heat from the die to the package surface purely by conduction.

Note that Θ_{JC} considers only the resistance of heat flow paths to the surface of the package. For this reason Θ_{JC} is always smaller than Θ_{JA} . Thus, Θ_{JC} represents a specific, conductive, heat-path thermal resistance, whereas Θ_{JA} represents conductive, convective, and radiative heat paths.

Θ_{CA} is thermal resistance from case to ambient. Θ_{CA} includes thermal resistances for all heat paths from outside the package to ambient.

Given the above definitions, we see that:

$$\Theta_{JA} = \Theta_{JC} + \Theta_{CA}$$

Θ_{JB} is thermal resistance from junction to board. Θ_{JB} quantifies the junction-to-board thermal path and is typically measured on the board adjacent to the package near pin 1 (< 1mm from the package edge). Θ_{JB} includes thermal resistance from two sources: from the IC's junction to a reference point on the package bottom, and through the board under the package.

To measure Θ_{JB} , convection from the top of the package is blocked and a cold plate is attached to the board's far side opposite the package location. See **Figure 1** below.

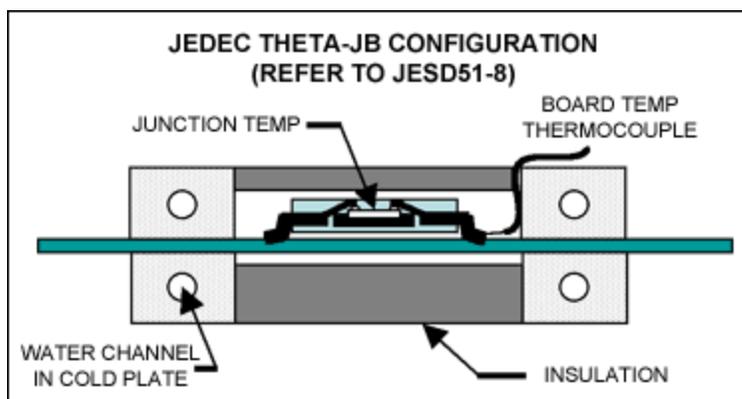


Figure 1. Illustration of the process for measuring Θ_{JB} .

Ψ_{JB} is the junction-to-board *thermal-characterization parameter*, measured in units of °C/W. The JESD51-12, *Guidelines for Reporting and Using Package Thermal Information*, clarifies that thermal-characterization parameters are not the same as thermal resistances. Instead, Ψ_{JB} measures component power flowing through multiple thermal paths rather than a single direct path, as in thermal resistance, Θ_{JB} . Thus, Ψ_{JB} thermal paths include convection from the top of the package, a fact that makes Ψ_{JB} more useful for customer applications. Refer to the JEDEC standards JESD51-8 and JESD51-12 for more detailed specifications on this parameter.

Designers can determine Θ_{JB} and Ψ_{JB} values by thermal modeling or direct measurement. In either case, follow these steps:

1. Control the power dissipation conditions appropriate for Θ_{JB} or Ψ_{JB} .
2. Determine the die temperature, typically using a diode on chip.
3. Determine the PCB temperature at < 1mm from the package's edge.
4. Determine the power dissipation.

Ψ_{JT} is the characterization parameter that measures temperature change between the junction temperature and the temperature of the top of the package. Ψ_{JT} is useful for estimating the junction temperature when the temperature on top of the package and the power dissipation are known.

Thermal Calculations

Junction Temperature

$$T_J = T_A + (\Theta_{JA} \times P)$$

Where:

T_J = junction temperature

T_A = ambient temperature, and

P = power dissipation in Watts

T_J can also be calculated by using Ψ_{JB} or Ψ_{JT} values as.

$$T_J = T_B + (\Psi_{JB} \times P)$$

Where:

T_B = board temperature measured within 1mm of the package

$$T_J = T_T + (\Psi_{JT} \times P)$$

Where:

T_T = temperature measured at the center of the top of package.

Note: product data sheets specify the maximum allowable junction temperature for each device.

Maximum Allowable Power Dissipation

$$P_{max} = (T_{J-max} - T_A) / \Theta_{JA}$$

Maxim listings of maximum allowable power assume an ambient temperature of +70°C and a maximum allowable junction temperature of +150°C.

Deration Function

This function describes how much the power dissipation must be reduced for each °C of ambient temperature over +70°C. The deration function is expressed in mW/°C.

$$\text{Deration function} = P / (T_J - T_A)$$

Where:

T_A is typically +70°C (commercial)

And:

T_J is the maximum allowable junction temperature, typically +150°C.

To find the maximum allowable power when the ambient temperature is above +70°C (for example, +85°C in the extended temperature range), proceed as follows:

$$P_{\text{max85C}} = P_{\text{max70C}} - (\text{Deration Function} \times (85 - 70))$$

Thermal Characterization and Measurement Conditions

The thermal performance of an IC package must be measured with JEDEC-standard methodologies and equipment. Characterizations run with application-specific boards can yield different results. It is also understood that the JEDEC-defined configurations do not represent typical real-world systems. Instead, the JEDEC configurations allow standardized thermal analysis and measurements for consistency; they are most useful for comparing the thermal figures of merit among package variations.

JEDEC specifications are available at: [JEDEC](#). Note that the JEDEC standards cover different thermal applications.

JEDEC Specification Titles

JESD51: Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)

JESD51-1: Integrated Circuit Thermal Measurement Method—Electrical Test Method (Single Semiconductor Device)

JESD51-2: Integrated Circuit Thermal Test Method Environmental Conditions—Natural Convection (Still Air)

JESD51-3: Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

JESD51-4: Thermal Test Chip Guideline (Wire Bond Type Chip)

JESD51-5: Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms

JESD51-6: Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)

JESD51-7: High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

JESD51-8: Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board

JESD51-9: Test Boards for Area Array Surface Mount Package Thermal Measurements

JESD51-10: Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements.

JEDEC51-12: Guidelines for Reporting and Using Electronic Package Thermal Information.

Summary of JEDEC Thermal, Multilayer Test-Board Specification JESD51-7

High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

The thermal test board described in the JESD51-7 specification is most appropriate for Maxim IC applications.

Material: FR-4

Layers: two signals (front and backside) and two planes (internal)

Finished thickness: 1.60 ±0.16mm

Metal thickness:

- Front and backside: 2oz copper (0.070mm finished thickness)
- Two internal planes: 1oz. copper (0.035mm finished thickness)

Dielectric layer thickness: 0.25mm to 0.50mm

Board size: 76.20mm x 114.30mm ±0.25mm for packages less than 27mm on a side

Component Side Trace Design

Traces should be laid out so that the test device is centered on the board. Traces must extend at least 25mm from the edge of the package body. Trace widths shall be 0.25 ±10% for 0.5mm or greater pitch packages. For packages with finer pitches, the trace width shall equal the lead width. Trace pattern and trace termination requirements are specified in JESD51-7.

Backside Trace Design

Component side traces terminated with through-hole vias can be connected to the edge connector by traces or by wire (22 AWG or smaller, copper wire). JESD51-7 specifies the current limits for different wire sizes.

Power and ground planes must be unbroken except for via isolation clearance patterns. The planes must not be present within 9.5mm of the edge connector pattern.

Exposed-Pad Packages

A critical requirement for thermal performance in exposed-pad (EP) packages (such as QFNs, DFNs (dual flat pack no-leads), and EP-TQFPs) is the design of thermal vias under the exposed pad solder joint. In a typical thermal-characterization board design there is an array of 4, 9, or 16 thermal vias connecting to the nearest ground plane. The thermal improvement becomes asymptotic above 25 vias. Understanding the direct relationship between board thermal vias and system thermal performance is critical. Refer to JESD51-5 for board-design enhancements for exposed-pad packages.

Solder Coverage

When customers characterize their board soldering processes, they should target 90% or better coverage under the solder joint. When the solder joint voids approach 50% or more, the resulting disconnection of thermal vias will have a catastrophic effect on thermal resistance.

Thermal Modeling

FLOTHERM® and other thermal-analysis software programs allow accurate package and system thermal predictions. When appropriate thermal models are combined with empirical data, the user can have high

confidence that the results accurately reflect real-world applications.

Electrical design tools such as PSPICE or Cadence® tools can be used to make simple thermal models of packages. The package elements are represented as resistors connecting to the board in a resistor network. When the package model is confirmed to agree with empirical data, then the model can be used to predict package variations, including: die sizes, exposed pad sizes, fused leads, or the number of grounds connected to planes. These "what if" models give a reasonably accurate prediction of customized configurations.

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Application Note 4083: <http://www.maximintegrated.com/an4083>

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