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#### APPLICATION NOTE 4060

# How to Generate PWM Waveforms Using Timer B on MAXQ Microcontrollers

Jun 20, 2007

*Abstract: This application note describes how to set up and use the Timer B in the MAXQ® family of microcontrollers to generate desired PWM waveforms. The action will require that the compare functionality be enabled. The note includes source code for reference.*

## Introduction

The MAXQ microcontrollers have three types of timers: Timer 0, Timer 1, and Timer 2. Timer B is an enhanced version of Timer 1 with modifications to support different input-clock prescaling and set/reset/compare output functionality. This application note details how to set up and use Timer B to generate desired waveforms. Source code examples are included for reference.

## Timer B Registers and Their Use

The MAXQ core configures Timer B through a set of Special Function Registers (SFR):

- TBCN—Timer B Control Register
- TBV—Timer B Value Register
- TBR—Timer B Reload/Capture Register
- TBC—Timer B Compare Register

### Timer B Control Register: TBCN

The Timer B Control register is 16-bit wide and unrestricted read and write. It is cleared to 0000h on all forms of reset. Below are brief descriptions of the register bit configuration.

Bit 0: The CP/RLD bit is used to set either Capture or Reload mode for Timer B. When this bit is set to 1, Timer B is in Capture mode. When this bit is clear to 0, Timer B is in Reload mode.

Bit 1: The ETB bit is used to enable a Timer B interrupt. Setting this bit to 1 enables the interrupt from the Timer B TFB and EXFB flags.

Bit 2: The TRB bit is used to enable Timer B operation.

Bit 3: The EXENB bit is used to enable the Capture/Reload function on the TBB pin for a negative transaction. When operating in autoreload mode (CP/RLD = 0) with the output-compare functionality enabled (this mode will be important later), enabling the TBB input function (EXENB = 1) will allow compare output negative transitions to set the EXFB flag. No reload will occur, however, as a result of the external negative edge detection.

Bit 4: The DCEN bit is used to enable a count-down option for Timer B. In conjunction with the TBB pin, this bit controls the direction that Timer B counts. Setting this bit to 1 causes Timer B to count up if pin TBB is 1, and count down if pin TBB is 0. Timer B always counts up when this bit is 0. When the compare-mode functionality of Timer B is enabled, the up/down count control of Timer B is controlled internally, based on the compare-mode settings. In the compare modes, the DCEN bit controls whether the timer ramps up and resets (DCEN = 0), or ramps up and down (DCEN = 1).

Bit 5: The TBOE bit is used to enable the clock-output function on the TBA pin.

Bit 6: The EXFB bit is used to flag when a negative transaction occurs on the TBB pin. This bit also toggles whenever Timer B overflows or underflows if CP/RLD = 0, DCEN = 0, and TBCS:TBCR = 00b.

Bit 7: The TFB bit is used to set a flag when Timer B overflows or underflows.

Bit 8-10: The TBPS2:0 are used as a prescaler applied to the system clock input to Timer B clock:

Timer B clock = System clock / (2<sup>2\*TBPS2:0</sup>)

The values of TBPS2:0 = 11xb are reserved.

Bit 11-12: The TBCS:TBCR bits are used to configure Timer B in compare mode if TBCS:TBCR <> 00b. These compare-mode bits define several conditions: whether the PWM/compare-mode output function is enabled on the TBB pin; what is the initial output starting state; and what compare-mode output function is in effect.

Bit 14-13: Reserved bits

Bit 15: The C/TB bit is used to determine whether Timer B functions as a timer or a counter.

### **Timer B Value Register: TBV**

The Timer B Value register is a 16-bit register and is cleared to 0000h on all forms of reset. This register is unrestricted read/write and is used to load and read the 16-bit Timer B value.

### **Timer B Capture/Reload Register: TBR**

Timer B Capture/Reload register is a 16-bit register and is cleared to 0000h on all forms of reset. This register is unrestricted read/write and is used to capture the TBV value when the Timer B is configured in capture mode. This register is also used as the 16-bit reload value when Timer B is configured in autoreload mode.

### **Timer B Compare Register: TBC**

The Timer B Compare register is a 16-bit register and is cleared to 0000h on all forms of reset. This register is unrestricted read/write and is for comparing TBC to the TBV value when Timer B operates in compare mode.

## Operational Modes of Timer B

Timer B can be configured in capture or reload mode by setting the CP/RLD bit in the Timer B Control register. Values of TBCS:TBCR<>00b will set Timer B in compare mode. It is not necessary to prevent configuration of the Timer B capture mode (CP/RLD=1) and the PWM compare output mode at the same time, however, this is not an intended Timer B mode of operation. Timer B can also be configured in compare mode, in which there are three different compare functions: RESET, SET, and TOGGLE.

This following section reviews methods for configuring Timer B in these different operational modes.

### Capture Mode

Bit 0 CP/RLD of the Timer B Control register determines whether the capture or reload mode is used for Timer B. Setting this bit to 1 causes a Timer B capture to occur when a falling edge is detected on the TBB timer pin if bit 3 EXENB of Control register is 1. Setting bit 3 EXENB to 0 causes Timer B to ignore all external events on the TBB pin. The captured value is loaded into the reload register TBR.

### Reload Mode

Clearing the CP/RLD bit to 0 causes an autoreload to occur when Timer B overflows or a falling edge is detected on TBB if EXENB is 1. If compare functionality is enabled, the frequency and duty cycle of the output waveforms can be modified by changing the values in the Reload (TBR) and Compare (TBC) registers. In this way, the MAXQ processor can generate a pulse-width modulated (PWM) waveform.

### Compare Mode

The compare mode is only enabled when the values of the compare mode bits are different from 0, and when Timer B is recommended to be in reload mode. The PWM outputs can be selectively enabled and the starting polarity can be inverted, depending on the value of these bits. The limits on frequency and duty cycle are determined by the frequency of the clock selected as source (i.e., the system or alternate clock) and the clock divisor selected. As noted above, there are three compare modes (SET, RESET, and TOGGLE) with a predefined initial state of the TBB pin.

1. The compare RESET mode is selected when CP/RLD = 0 (reload mode) and values of TBCS:TBCR are 01, respectively. In this mode, the TBB will reset on a TBC match and set on 0000h. Depending on the relative values between the TBR and TBC registers and on the up/down count, the timer will generate different PWM waveforms. If Timer B does not implement TBC, then it will only set on 0000h. In this mode the initial value of the TBB pin is LOW.
2. The compare SET mode is selected when CP/RLD = 0 (reload mode) and the values of TBCS:TBCR are 10, respectively. In this mode, the TBB will set on a TBC match and set on TBR. Depending on the relative values between the TBR and TBC registers and on the up/down count, the timer will generate different PWM waveforms. If Timer B does not implement TBC, then it will only reset on TBR. In this mode the initial value of the TBB pin is HIGH.
3. The compare TOGGLE mode is selected when CP/RLD = 0 (reload mode) and values of TBCS:TBCR are 11, respectively. In this mode, the TBB will toggle on a TBC match (except TBR or 0000h). Depending on the relative values between the TBR and TBC registers and on the up/down count, the timer will generate different PWM waveforms. If Timer B does not implement TBC, then it will only toggle on a TBR match. In this mode the initial value of TBB pin is unchanged.

The initial state for the TOGGLE mode depends on the previous SET or RESET mode. This means that to establish a specific starting state, the TBCS:TBCR bits should be configured to SET or RESET momentarily when changing from Compare disable to Compare Toggle Mode.

As mentioned above, we are particularly interested in this compare mode that is used to generate PWM

on the TBB pin of Timer B. The PWM waveform greatly depends on the relative values between TBR and TBC, with or without the TBC register, and the value of DCEN bit (**Table 1**).

## PWM Waveform of Timer B in Compare Mode

### Timer B Without TBC Register

The pin set/reset that can result from the TBC compare match can never occur for the SET and RESET modes. The user can only define a starting pin state that will take effect when the timer is enabled. Pin set or clear operations for the respective RESET and SET modes will still occur. For the TOGGLE mode, the TBR will be used to generate a 50% duty-cycle PWM. See **Table 1** and **Figure 1**.

**Table 1. Timer B Output Function Without a TBC Register**

TBCS:TBCR	Function	Initial State (If TBR = 0)
00	None (Compare disable)	No change
01 (RESET)	Set on 0000h	Low
10 (SET)	Reset on TBR match	High
11 (TOGGLE)	Toggle on TBR match	No change

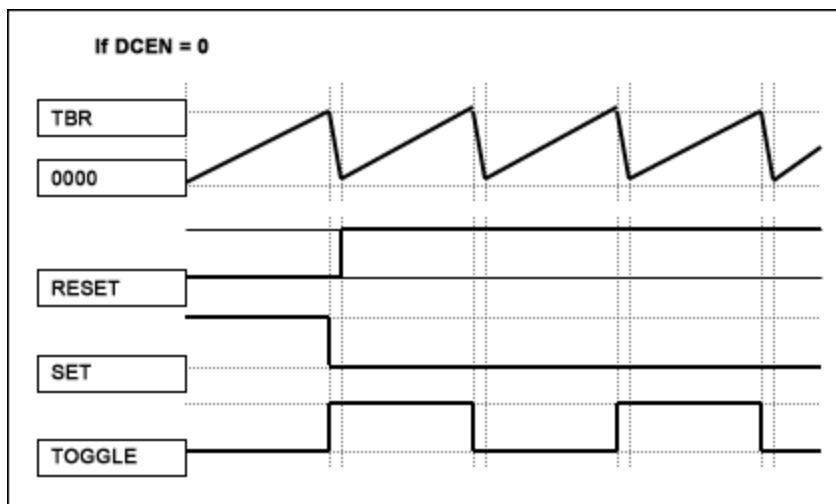


Figure 1.

- Set or clear the TBB pin timed at TBR+1 and TBR, respectively for RESET and SET operations.
- Generate a 50% duty cycle for TOGGLE mode at period  $2 \cdot TBR + 2$ .

### Example 1: Set the TBB pin after 1 second since the timer was on (use RESET compare mode).

- Frequency of the Timer B: Calculate Timer B frequency based on a 12MHz system clock.
- Use RESET compare mode with DCEN = 0 to set the TBB pin.
- Calculate the values of TBR to delay 1 second by using below formula:

$(TBR+1) \times \text{timer cycle} = 1\text{s}$  where 1 timer cycle =  $1/\text{system clock}$   
 $(TBR+1)/\text{system clock} = 1 \Rightarrow TBR = \text{system clock} - 1$ . Value of TBR  $\leq 0\text{FFFFH}$ .  
 We need to choose system clock  $\leq 0\text{FFFFH} = 65535$  or  
 prescaler  $\geq 12000000/65535 = 183$ . We pick a prescaler = 256.  
 $\Rightarrow TBR = 12000000/256 - 1 = 46874$

Sample code:

```

move    TB2CN,#000H      ; Reset Timer B
move    TB2CN,#0C00H     ; Timer B clock = system clock/256
                          ; and in compare RESET mode
move    TB2R, #46874     ; Set reload value of Timer 2 TBR = 46874
move    TB2V, #0001H     ; Reset TBV=0x01 just to avoid set
                          ; operation on 0000h
move    TB2CN.2,#1       ; Start Timer B to generate PWM

```

**Example 2: Generate a 1MHz waveform with a 50% duty cycle starting with LOW (use TOGGLE compare mode). (See Figure 2.)**

- Frequency of the Timer B: Calculate the Timer B frequency based on a 12MHz system clock.
- Use the TOGGLE compare mode with DCEN = 0 to set the TBB pin.
- Calculate the values of TBR with a desired PWM frequency of 1MHz by using the formula:

$$\text{Period} = (2 \times \text{TBR} + 2) \times \text{timer cycle} = 1/1000000 \text{ where } 1 \text{ timer cycle} = 1/12\text{MHz} \Rightarrow 2 \times \text{TBR} + 2 = 12000000/1000000 = 12 \text{ or } \text{TBR} = 5$$

Sample code:

```

move    TB3CN,#000H      ; Reset Timer B
move    TB3CN,#0800H     ; Configure Timer B clock in RESET
                          ; Compare mode to start LOW
move    TB3CN,#1800H     ; Timer B clock = system clock
                          ; and in compare TOGGLE mode with DCEN = 0
move    TB3R, #5          ; Set reload value of Timer 3 TB3R = 5
move    TB3V, #000H     ; Reset TBV=0x00
move    TB3CN.2,#1       ; Start Timer B to generate PWM

```

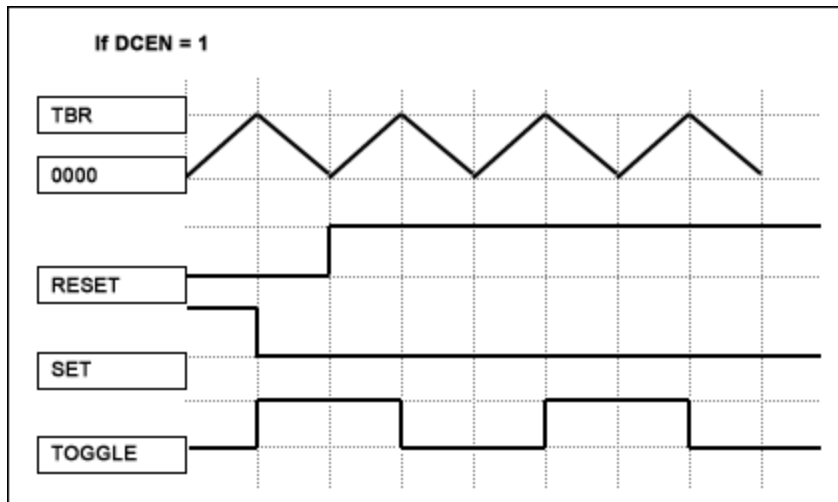


Figure 2.

- Set or clear the TBB pin timed at  $2 \times \text{TBR}$  and  $\text{TBR}$ , respectively, for RESET and SET operations.
- Generate a 50% duty cycle for TOGGLE mode at period  $4 \times \text{TBR}$ .

**Example 3: Reset the TBB pin after a 1µs delay (use SET compare mode).**

- Frequency of the Timer B: Calculate Timer B frequency based on a 12MHz system clock.
- Use SET compare mode with DCEN = 1 to set the TBB pin.
- Calculate the values of TBR to delay 1µs by using the formula:

$$\text{TBR} \times \text{timer cycle} = 1\mu\text{s where } 1 \text{ timer cycle} = 1/\text{system clock}$$

TBR/system clock = 1µs => TBR = 12000000/1000000. The value of TBR = 12.

Sample code:

```

move    TB3CN,#000H      ; Reset Timer B
move    TB3CN,#1010H    ; Timer B clock = system clock
                        ; and in compare SET mode with DCEN = 1
move    TB3R, #12       ; Set reload value of Timer 3 TB3R = 12
move    TB3V, #000H     ; Reset TBV = 0x00
move    TB3CN.2,#1      ; Start Timer B to generate PWM

```

**Example 4: Generate a 1MHz waveform with a 50% duty cycle starting with HIGH (use TOGGLE compare mode).**

- Frequency of the Timer B: Calculate Timer B frequency based on a 12MHz system clock.
- Use TOGGLE compare mode with DCEN = 1 to set the TBB pin.
- Calculate the values of TBR with a desired PWM frequency of 1Mhz by using the formula:

$$\text{Period} = (4 \times \text{TBR}) \times \text{timer cycle} = 1/1000000 \text{ where } 1 \text{ timer cycle} = 1/12\text{MHz} \Rightarrow 4 \times \text{TBR} = 12000000/1000000 = 12 \text{ or } \text{TBR} = 3$$

Sample code:

```

move    TB2CN,#000H      ; Reset Timer B
move    TB2CN,#01000H    ; Configure Timer B clock in SET
                        ; Compare mode to start HIGH
move    TB2CN,#1810H    ; Timer B clock = system clock
                        ; and in compare TOGGLE mode with DCEN=1
move    TB2R, #3         ; Set reload value of Timer 2 TB2R = 3
move    TB2V, #000H     ; Reset TBV = 0x00
move    TB2CN.2,#1      ; Start Timer B to generate PWM

```

**Timer B with TBC Register**

When the TBC register is within the counting range (TBC < TBR), the SET and RESET compare functions essentially provide the same functionality by using a TBR reload value to change the frequency. The TOGGLE compare mode allows a 50% duty-cycle PWM waveform. With the TBC register outside the range (TBC > TBR) or in the special cases of TBC = TBR and TBC = 0, the SET and RESET functions allow a timer clear or set of the TBB pin. See **Table 2** and **Figure 3**.

**Table 2. Timer B Output Function with TBC Register**

TBCS:TBCR	Function	Initial State (If TBR = 0)
00	None (Compare disable)	No change
01 (RESET)	Reset on TBC match, set on 0000h	Low
10 (SET)	Set on TBC match, reset on TBR match	High
11 (TOGGLE)	Toggle on TBC match (except TBR or 0)	No change

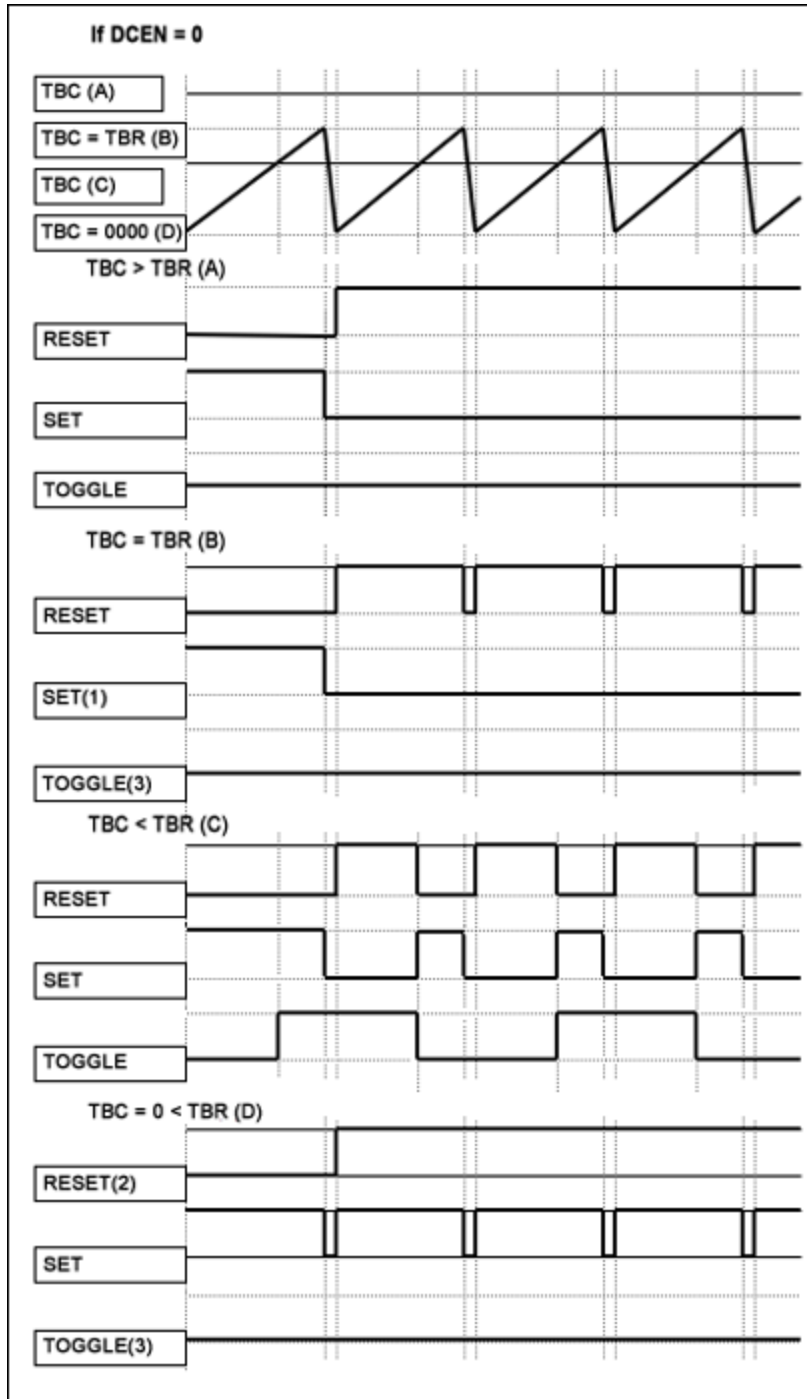


Figure 3.

- TBC > TBR: Set or clear the TBB pin for the respective RESET and SET modes. TOGGLE mode is disabled.
- TBC = TBR or TBC = 0: See notes 1, 2, and 3 after **Example 8** below.
- TBC < TBR: PWM is generated with a duty cycle and period as shown below:
  - SET mode =  $(TBR - TBC)/(TBR + 1)$  with a period of  $TBR + 1$
  - RESET mode =  $TBC/(TBR + 1)$  with a period of  $TBR + 1$

- TOGGLE mode = 50% with period  $2 \times \text{TBR} + 2$

**Example 5: Generate a 32kHz waveform with a 50% duty cycle starting HIGH (use SET compare mode).**

- Frequency of the Timer B: This is the same as a 12MHz system clock.
- Use SET compare mode with DCEN = 0 to generate this waveform.
- Calculate the values of TBR and TBC with a desired PWM frequency of 32kHz using the formula:

$$\text{Period} = (\text{TBR} + 1) \times \text{timer cycle} = 1/32000 \text{ where } 1 \text{ timer cycle} = 1/12\text{MHz}$$

$$\text{TBR} + 1 = 12000000/32000 \Rightarrow \text{TBR} = (12000000/32000) - 1 = 372$$

- Duty cycle =  $(\text{TBR} - \text{TBC})/(\text{TBR} + 1) = 50\% \Rightarrow \text{TBC} = 186$

Sample code:

```

move    TB0CN,#1000H      ; Configure Timer B clock as same as
                        ; system clock and in compare SET mode
move    TB0C, #00186     ; set compare value of Timer 0 TBC = 186
move    TB0R, #00372     ; Set reload value of Timer 0 TBR=372
move    TB0V, #0000H     ; Reset TBV=0x00
move    TB0CN.2,#1       ; Start Timer B to generate PWM

```

**Example 6: Generate a 512Hz waveform with a 50% duty cycle starting LOW (use TOGGLE mode). (See Figure 4.)**

- Frequency of the Timer B: This is the same as a 12MHz system clock.
- Use TOGGLE compare mode with DCEN = 0 to generate this waveform.
- Calculate the values of TBR and TBC with a PWM frequency of 512Hz using the formula:

$$\text{Period} = \text{timer cycle} / (2 \times \text{TBR} + 2) = 1/512 \text{ where } 1 \text{ timer cycle} = 1/12\text{MHz}$$

$$512 = 12000000 / (2 \times \text{TBR} + 2) \Rightarrow \text{TBR} = ((12000000/512) - 2) / 2 = 23434 / 2 = 11717$$

- Duty cycle = 50% regardless  $\text{TBC} < 11717$

Sample code:

```

move    TB1CN,#0800H     ; Configure Timer B clock in RESET
                        ; Compare mode to start LOW
move    TB1CN,#1800H     ; Configure Timer B clock as same as
                        ; system clock and in compare TOGGLE mode
move    TB1C, #005000    ; Set compare value of Timer 1 TBC = 5000
move    TB1R, #011717    ; Set reload value of Timer 1 TBR = 11717
move    TB1V, #0000H     ; Reset TBV=0x00
move    TB1CN.2,#1       ; Start Timer B to generate PWM

```



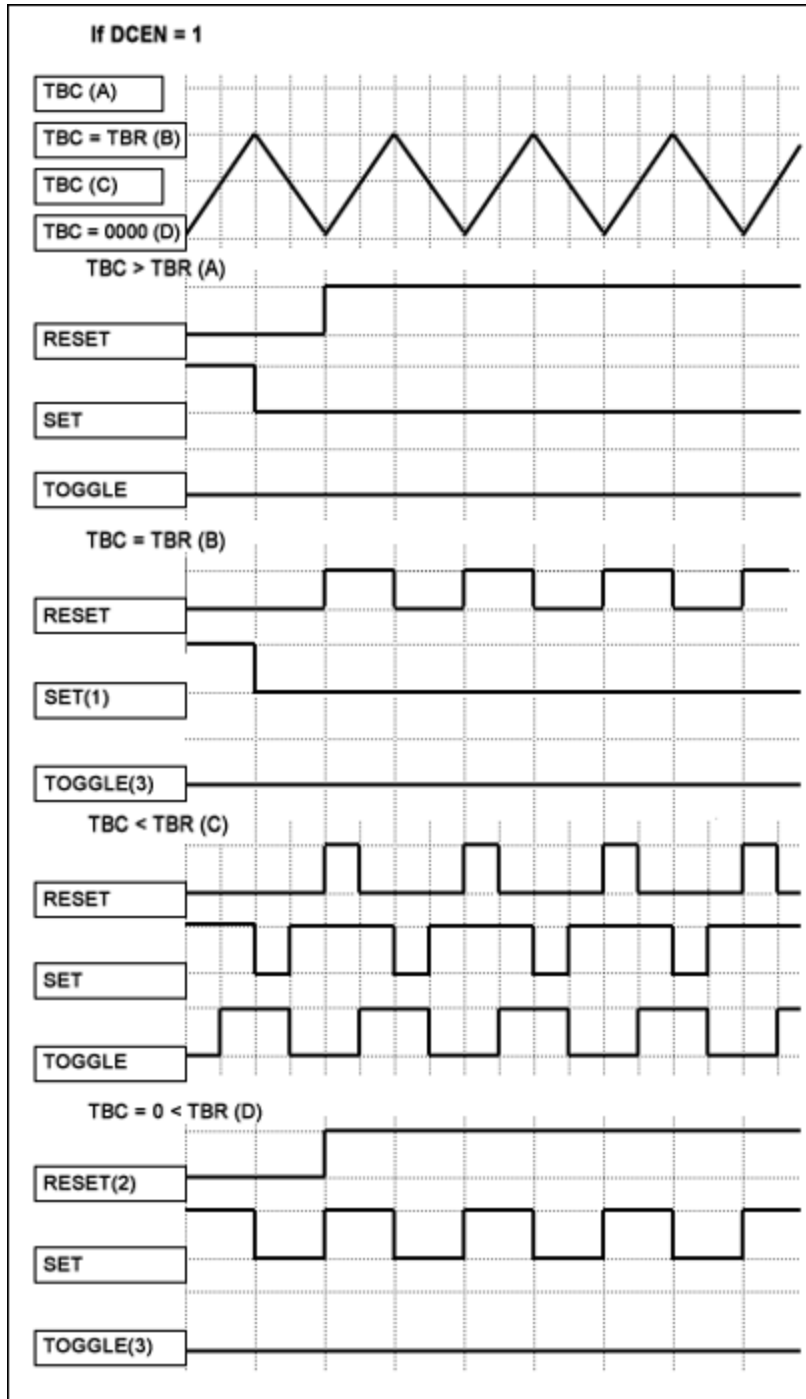


Figure 4.

- TBC > TBR: Set or clear the TBB pin for the respective RESET and SET modes. TOGGLE mode is disabled.
- TBC = TBR or TBC = 0: See notes 1, 2, and 3 after **Example 8**.
- TBC < TBR: PWM is generated with a period of  $2 \times TBR$  and with the duty cycle defined as below:
  - SET mode =  $(TBR - TBC)/(2 \times TBR)$
  - RESET mode =  $TBC/(2 \times TBR)$
  - TOGGLE mode =  $TBC/TBR$  (Start HIGH) or  $(TBR - TBC)/TBR$  (start LOW)<sup>4</sup>

**Example 7: Generate a 32kHz waveform with a 30% duty cycle starting LOW (use RESET compare mode).**

- Frequency of the Timer B: 3MHz or system clock/4.
- Use RESET compare mode with DCEN = 1 to generate this waveform.
- Calculate the frequency of the PWM waveform using the formula:

$$\text{Period} = \text{timer cycle}/(2 \times \text{TBR}) = 1/32000 \text{ where } 1 \text{ timer cycle} = 1/3\text{MHz}$$
$$\text{TBR} = (3000000/32000)/2 = 98/2 = 49$$

- Duty cycle =  $\text{TBC}/(2 \times \text{TBR}) = 30\% \Rightarrow \text{TBC} = 29$

Sample code:

```
move    TB0CN,#0910H      ; Configure Timer B clock in system
                          ; clock/4, in compare RESET mode, and
                          ; DCEN = 1
move    TB0C, #00029      ; Set compare value of Timer 0 TBC = 29
move    TB0R, #00049      ; Set reload value of Timer 0 TBR = 49
move    TB0V, #0000H      ; Reset TBV = 0x00
move    TB0CN.2,#1        ; Start Timer B to generate PWM
```

**Example 8: Generate a 512Hz waveform with a 40% duty cycle starting HIGH (use TOGGLE mode).**

- Frequency of the Timer B: This is the same as a 12MHz system clock
- Use TOGGLE compare mode with DCEN = 1 to generate this waveform.
- Calculate the values of TBR and TBC with a PWM frequency of 512Hz using the formula:

$$\text{Period} = \text{timer cycle}/(2 \times \text{TBR}) = 512 \text{ where } 1 \text{ timer cycle} = 1/12\text{MHz}$$
$$512 = 12000000/(2 \times \text{TBR}) \Rightarrow \text{TBR} = (12000000/512)/2 = 23437/2 = 11718$$

- Duty cycle = 40% or  $\text{TBC}/\text{TBR} = 0.4 \Rightarrow \text{TBC} = 4687$

Sample code:

```
move    TB1CN,#01000H     ; Configure Timer B clock in SET
                          ; compare mode to start HIGH
move    TB1CN,#1810H      ; Configure Timer B clock as same as
                          ; system clock in compare TOGGLE mode
                          ; and DCEN = 1
move    TB1C, #004687     ; Set compare value of Timer 1 TBC = 4687
move    TB1R, #011718     ; Set reload value of Timer 1 TBR=11718
move    TB1V, #0000H      ; Reset TBV = 0x00
move    TB1CN.2,#1        ; Start Timer B to generate PWM
```

**Notes:**

<sup>1</sup>When the output compare function is configured to the SET mode, configuring TBC = TBR disables the TBC compare match operation. The timer will not set when TBC = TBR.

<sup>2</sup>When the output compare function is configured to the RESET mode, configuring TBC = 0 disables the TBC compare reset operation. The timer will not reset when TBC = 0.

<sup>3</sup>When the output compare function is configured to the TOGGLE mode, configuring TBC = 0 or TBC = TBR disables the toggle function. The output PWM will be either LOW or HIGH, depending on the initial starting state of the TBB pin.

<sup>4</sup>The initial state for the TOGGLE mode depends on the previous SET or RESET mode. This means that the TBCS:TBCR bits should be configured to SET (start HIGH) or RESET (start LOW) momentarily when changing from 'Compare disable' to 'Compare TOGGLE mode' to establish a specific starting state.

## Examples

All the above examples are executed on a MAXQ microcontroller with Timer B. The device has four Timer Bs, of which Timers 0 and 1 have TBC registers and Timers 2 and 3 do not. The clock is running at approximately 12Mhz.

## Additional Notes

- When in compare mode with DCEN = 1, the timer is always counting up regardless of the current value of the TBB pin. The timer functions like this because the counting direction is controlled internally.
- The normal counting range will be between 0000h to TBR for counting up and from TBR to 0000h for counting down. **Note:** this counting differs from TBR to 0FFFFh and from 0FFFFh to TBR, as in other timers.
- Three source-clock prescaler bits (TBPS2:0) set a prescale value of  $2^{(N \times 2)}$  where N = 0, 1, 2, 3, 4, and 5, which is applied to the Timer B source clock.

## Conclusion

The Timer B in MAXQ microcontrollers can provide different PWM waveforms, depending on the relative values of the TBC and TBR registers and on the state of DCEN bit. Timer B will work with or without Compare register TBC. Tables 1 and 2 summarize the Timer B output function without and with the TBC compare register, respectively. Figures 1 through 4 show the typical PWM waveforms on the pin TBB of Timer B for each particular configuration. For all cases, the user can determine the PWM period and duty cycle with the defined formulas.

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