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APPLICATION NOTE 4032

HFTA-16.0: ESD Protection for Bipolar Integrated Circuits

Apr 23, 2007

Abstract: It is well known that electrostatic discharge (ESD) sends potentially destructive energy pulses to an integrated circuit (IC). Many design characteristics will affect the part's ESD performance. This application note discusses several issues that a circuit designer should consider to protect an IC from unshielded ESD.

Introduction

Electrostatic discharge (ESD) events send potentially destructive energy pulses to an integrated circuit (IC). Well-designed ICs have protection circuits to handle the ESD that can occur while the IC is being assembled into an application circuit. The IC must also handle ESD energy that penetrates electrostatic shields into the final circuit after assembly. Besides mechanical shielding, power-supply decoupling capacitors can help handle ESD; however, improper capacitor selection can make the IC more vulnerable. To properly protect an integrated circuit from unshielded ESD, the following issues should be considered.

- Delivery model for transfer of ESD to the IC
- ESD protection inside the IC
- Interaction between application circuits and the IC's internal ESD protection
- Modification of the application circuit to improve the ESD protection for the IC

ESD Delivery Models

Electrostatic discharge levels are described in terms of voltage. This voltage results from the charge stored on a capacitor that is transferred to the IC. The voltage and current stress on the IC results from the relation of the impedance between the IC and the ESD source. ESD testers are modeled after expected sources of charge.

Two models of charged objects are commonly used for ESD tests (**Figure 1**). The human body model (HBM) represents charge stored on a person's body (the 100pF capacitor) with discharge through the skin (the 1.5kΩ resistor). The machine model (MM) represents charge stored on a metallic object. Discharge in the MM is then limited only by the interconnect inductance.

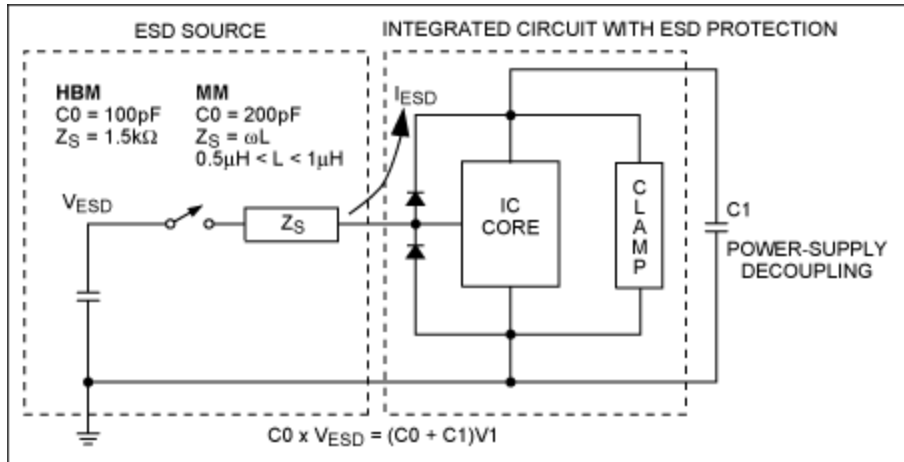


Figure 1. Models for ESD testing.

The following concepts are useful in evaluating the delivery of ESD to an IC.

1. The IC impedance is low for voltages above normal power-supply levels:

$$I_{ESD} = \frac{V_{ESD}}{Z_S}$$

For the HBM in Figure 1, $Z_S = Z_{HBM} = 1.5\text{k}\Omega$

2. For the MM, current is limited by the MM's impedance ($\sim 50\Omega$):

$$Z_{MM} = \frac{v}{i} = \sqrt{\frac{L}{C_0}}$$

The characteristic impedance calculated above results from energy (E) in a low-resistance L-C circuit:

$$E = \frac{1}{2} \times C_0 \times v^2 \text{ and } E = \frac{1}{2} \times L \times i^2$$

3. If the ESD current flows primarily into a power-supply decoupling capacitor, the voltage across the IC depends on conservation of charge:

$$Q = C \times V \text{ and } Q_{\text{Final}} = Q_{\text{Initial}}$$

$$V_1 \times (C_0 + C_1) = V_{ESD} \times C_0 \text{ (See Figure 1.)}$$

4. The energy levels, when applied over a short period that can damage an IC, are on the order of micro-Joules. This is an important consideration when external supply decoupling capacitors are present. The energy delivered to the IC for supply capacitance (C_1) in Figure 1 is given by:

$$E = \frac{1}{2} \times C_1 \times V_1^2$$

5. Heating results from power dissipation (P). By stretching the energy discharge over a longer time (t), the heating is reduced:

$$P = \frac{E}{t}$$

The delivery of ESD energy to low impedance can be considered a current (concepts 1 and 2 above). For high impedance, the energy is delivered as a voltage by charge transfer to the supply decoupling and stray capacitance of the IC (concept 3). IC damage derives typically from energy on the order of micro-Joules applied over times much less than a microsecond (concepts 4 and 5 above).

IC Internal-Protection Circuits

Standard protection schemes limit the voltage and current that can reach the IC core circuitry. Protection devices illustrated in Figure 1 include:

- ESD Diodes—a low-impedance path from signal pin to supply rail or ground, depending on polarity.
- Clamps—connected between supplies, clamps draw no current under normal supply conditions but develop low impedance during an ESD event.

ESD Diodes

If an IC pin is subjected to a HBM test where the initial voltage on the tester is 2kV, then the discharge current through the ESD diode (**Figure 2**) is about 1.33A:

$$I_{ESD} = \frac{2kV}{1.5k\Omega}$$

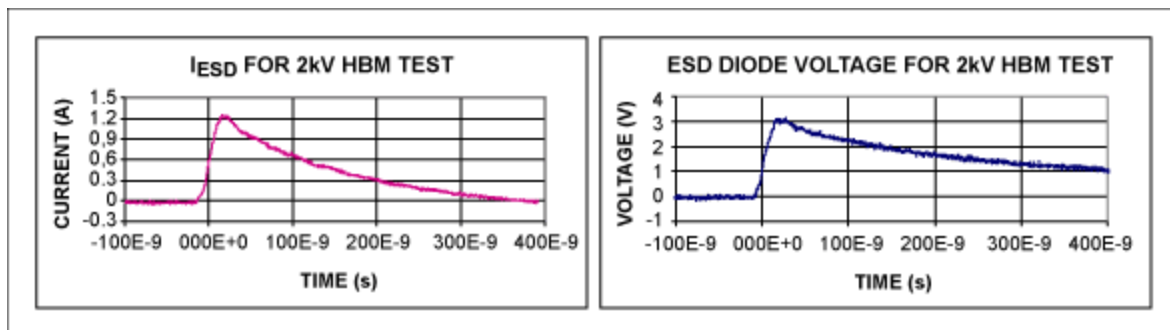


Figure 2. ESD diode current and voltage (measured data).

The pin voltage during an HBM test is limited, theoretically, to a diode drop. Large currents create I-R drops in the ESD diode and connecting traces, thus resulting in some extra voltage on the signal pin as seen in Figure 2.

To determine whether an IC can handle an ESD level such as 2kV, consult the manufacturer's documentation. The rating for the IC will state the maximum voltage, V_{ESD} in Figure 1, which the IC can withstand for a specific type of ESD source. The ESD tolerance for a Maxim IC can be found in the device's reliability report.

Supply Clamps

Clamp operation in a bipolar IC is similar to the onset of breakdown in the core circuits being protected. **Figure 3** shows a detailed circuit for the clamp in Figure 1. Overvoltage on the clamp transistor results in avalanche current from collector to base. Forward bias of the base emitter further increases collector

current, thus producing a condition called "snapback." A V-I characteristic of the clamp is shown in Figure 4.

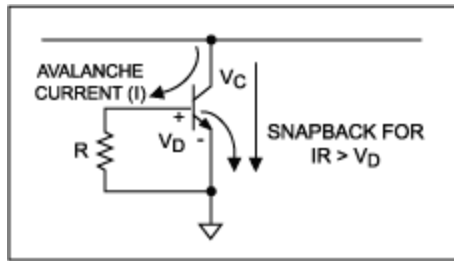


Figure 3. Clamp circuit for the clamp shown in Figure 1.

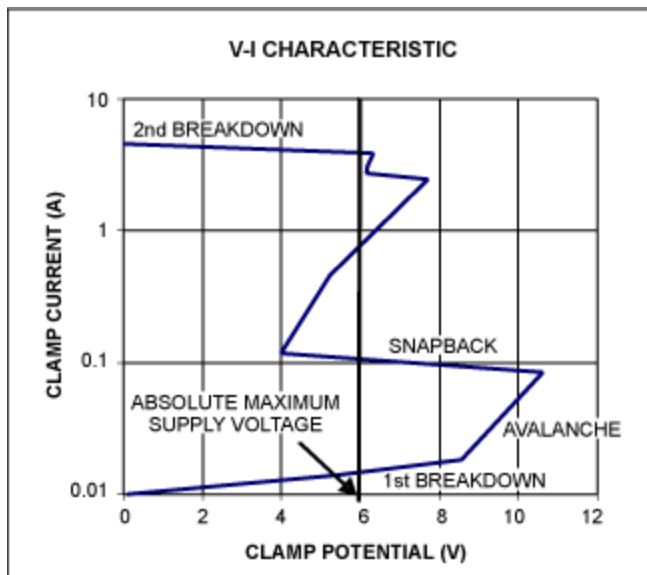


Figure 4. Clamp V-I characteristic.

The clamp turns on before any of the other circuits in the IC can be damaged. The clamp is also large enough so that the ESD current will not cause it to go into secondary breakdown. Operation of the clamp during a 2kV HBM test is recorded in Figure 5. The voltage in Figure 5 includes I-R drops and the clamp voltage after snapback.

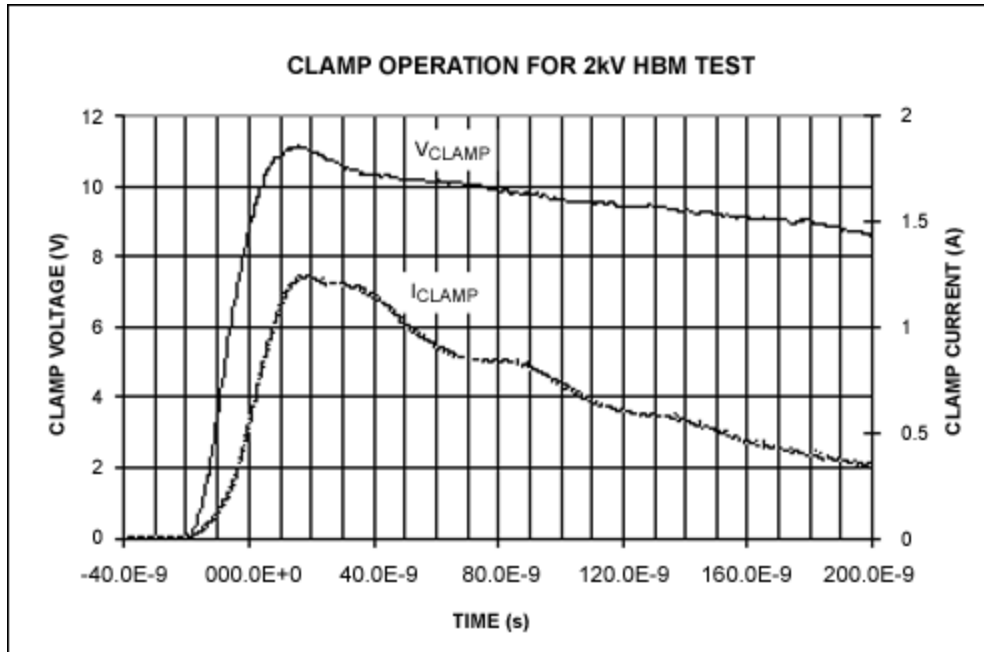


Figure 5. Clamp operation (measured data).

ESD Protection and Application Circuits

Clamp voltage varies from first breakdown to the ON value after snapback, as seen in Figure 5. To ensure that the clamp is off for normal operating conditions, designs often make the clamp voltage higher than the IC's absolute maximum voltage.

Power-supply decoupling capacitors interfere with clamp operation. Charge transferred to decoupling capacitors can produce higher voltage than the IC's absolute maximum, but not high enough for the clamp to turn on. The capacitor then functions as an energy source that can be dumped into the part nearly instantaneously.

For a given supply decoupling capacitor, the initial voltage that can develop during ESD testing results from the principle of conservation of charge. The voltage could reach 20V in a 2kV HBM test applied to a 0.01μF decoupling capacitor:

$$V_1 = V_{ESD} \times \frac{C_0}{(C_0 + C_1)}$$

or

$$20V = 2kV \times \frac{100pF}{(100pF + 0.01\mu F)}$$

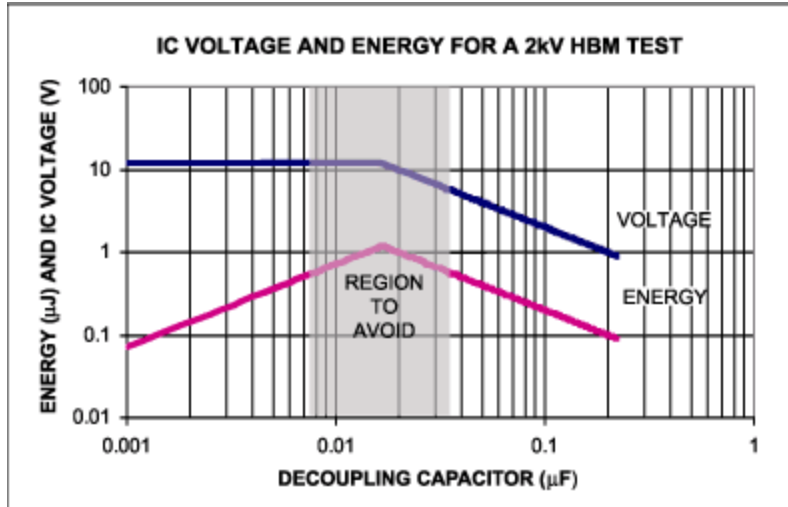


Figure 6. Energy and voltage vs. power-supply decoupling capacitance.

The dependence of available energy on the capacitance of the pin being protected is shown in **Figure 6**. For small decoupling capacitors, the clamp limits the voltage (V_1) by going into snapback. Approximately constant snapback voltage results in energy that increases in proportion to the capacitance. Once the supply decoupling capacitor is large enough that charge transfer does not produce enough voltage on the clamp for snapback, the energy stored begins to decrease as capacitance increases.

Voltages across the clamp that are larger than the IC's absolute maximum (6V, typ) and smaller than the clamp snapback (~10V) are a problem when decoupling capacitors are present because of stored energy. When ICs are tested with no external circuitry, the energy available with 10V on the pin is very low and not a threat.

Improving ESD Protection

The protection of the IC in an application can be improved by carefully selecting the size of the decoupling capacitors. Stored energy decreases with capacitance once the ESD charge no longer produces enough voltage to turn on the clamp. Consider this example for supply decoupling capacitor $C_1 \gg C_0$ in Figure 1:

Initially:

$$V_{1\text{init}} \approx V_{\text{ESD}} \times \frac{C_0}{C_1}$$

$$E_{\text{init}} = \frac{1}{2} \times C_1 \times V_1^2$$

Now consider what happens when C_1 is doubled:

$$V_{1\text{final}} \approx V_{\text{ESD}} \times \frac{C_0}{2 \times C_1}$$

$$E_{\text{final}} = \frac{1}{2} \times [2 \times C_1] \times \left[\frac{V_{1\text{init}}}{2} \right]^2 = \frac{E_{\text{init}}}{2}$$

Doubling the capacitance reduces the energy by a factor of 2.

The largest energy that can be absorbed in an HBM test is on the order of 1μJ for small-geometry, high-speed, bipolar integrated circuits. With a 2kV HBM test, the clamp will activate for capacitors smaller than about 0.02μF (Figure 6). To keep the available energy on the decoupling capacitor well below 1μJ, there are two choices of decoupling capacitance: either the capacitor should be larger than 0.05μF, or smaller than about 0.005μF. When higher test voltages must be used, the size of the large 0.05μF capacitor must increase proportional to the test voltage.

Unfortunately, it is not always possible to use large decoupling capacitors. Inrush current requirements can limit capacitor size. If the rate of applied voltage is not controlled, then the only limit on inrush is the size of the decoupling capacitor:

$$I_{IN} = C1 \times \frac{dV}{dt}$$

The connection of the decoupling capacitor to the supply voltage will always have some inductance. Often a filter inductance is added to this connection. In this configuration the maximum inrush current results from the characteristic impedance of the filter inductance and decoupling capacitors. This impedance (Z_0 in **Figure 7**) is similar to the current limit in the MM tester.

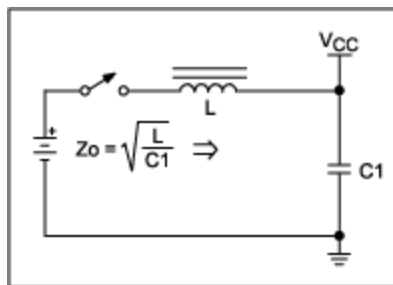


Figure 7. The power-supply impedance for large C1.

By limiting inrush current with an inductor, large filter capacitors (C1) are possible; voltage applied to the IC during an ESD event is below the part's absolute maximum rating.

Practical ways to improve ESD protection include:

- Use a large filter capacitor so that the maximum ESD voltage will be less than the absolute maximum for the IC pin.
- Use a small filter capacitor to ensure that the IC clamp activates at low energy.
- Increase the series inductance to limit inrush current, thus allowing large capacitors.
- Add external clamps, such as Zener diodes in **Figure 8**, to keep the ESD voltages below the absolute maximum rating of the device (**Figure 9**).

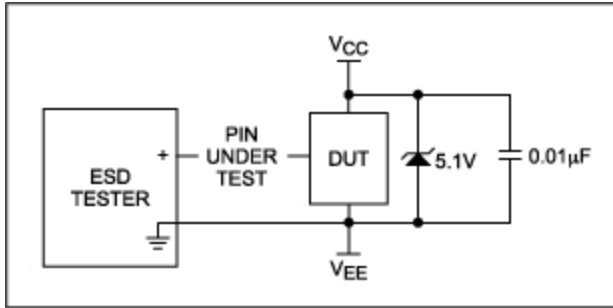


Figure 8. Zener ESD protection diode.

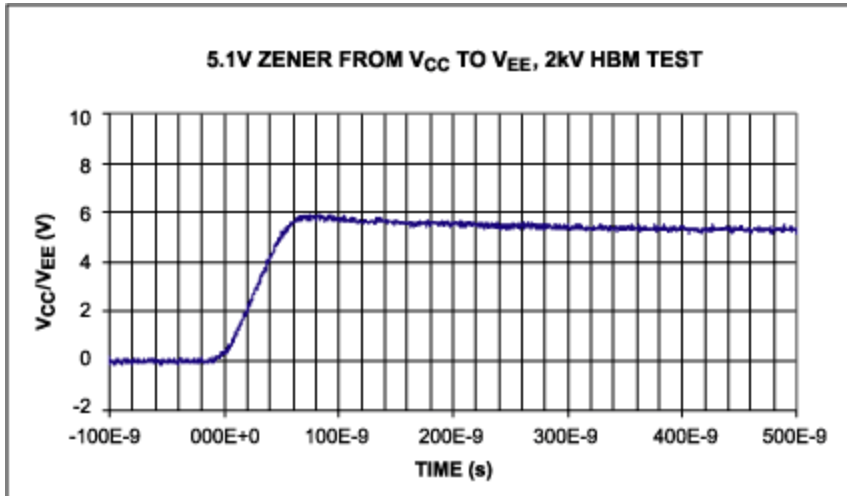


Figure 9. Improved clamping with a Zener protection diode (measured data).

Conclusion

ESD events that penetrate an application circuit's electrostatic shield are handled by the IC and its surrounding components. Power-supply decoupling capacitors can be an inexpensive way to reduce ESD stress on the IC. Many characteristics of a design affect ESD performance, and some considerations are summarized below:

1. Determine the test voltage (V_{ESD}) appropriate for the application. (2kV HBM or 100V MM are typical.)
2. Review the IC's ESD specification to ensure that the IC's diodes, clamps, and conductance paths are adequate for the test voltage. This information is in the reliability report for Maxim ICs.
3. Analyze the voltages that will be produced when external capacitors, such as power-supply filters (C1), are added to the IC.
4. Consider alternate supply filtering schemes to allow larger capacitors when voltages between the absolute maximum for the IC (typically 6V) and the clamp voltage (typically 8V to 10V) occur during an ESD event.
5. Use an external ESD protection device such as a Zener diode if a small supply decoupling capacitor must be used.

A similar article was published in the November 2006 issue of *Wireless Design and Development*.

More Information

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