Keywords: extended system information bus, ESIB, single chip transceivers, SCTs, transceiver

APPLICATION NOTE 401

Extended System Information Bus (ESIB) Control Application

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Abstract: The 3-wire extended system information bus (ESIB) function allows the interrupt status or other user-selectable alarm status information for multiple single chip transceivers (SCTs) to be accessed in a single read cycle.

Introduction

This application note is intended to show how the 3-wire extended system information bus (ESIB) function allows the interrupt status or other user-selectable alarm status information for multiple single-chip transceivers (SCTs) to be accessed in a single read cycle. This allows for streamlined access of certain status registers from a group of up to eight SCT ports with the host not needing to poll each port separately. The ESIB feature was first available on the DS2155 and DS21Q55, but any product with this feature can participate in an ESIB group because all SCTs within an ESIB group are independent from each other.

Extended System Information Bus (ESIB)

ESIB allows up to eight SCT ports to share an 8-bit CPU bus for reporting alarms and interrupt status as a group with a single bus read. There are two control registers (ESIBCR1 and ESIBCR2) and four information registers (ESIB1, ESIB2, ESIB3, and ESIB4). For example, eight DS2155s (or two DS21Q55s) can be grouped into an ESIB group. A single read of the ESIB1 register of any member of the ESIB group yields the interrupt status of all eight ports. Through ESIB2, the host can gather synchronization status for all members of the group. ESIB3 and ESIB4 can be programmed to report various alarms on a port-by-port basis. There are three device pins involved in forming an ESIB group: ESIBS0, ESIBS1, and ESIBRD. A 10kΩ pullup resistor must be provided on ESIBS0, ESIBS1, and ESIBRD. **Figure 1** shows an example of four DS2155 devices connected in an ESIB group.

ESIB Pins	
Signal Name:	**ESIBS0**
Signal Description:	**Extended System Information Bus Select 0**
Signal Type:	**Input/Output**
Used to group two to eight SCTs into a bus-sharing mode for alarm and status reporting.	

Signal Name:	**ESIBS1**
Signal Description:	**Extended System Information Bus Select 1**

Signal Type:	**Input/Output**

Used to group two to eight SCTs into a bus-sharing mode for alarm and status reporting.

Signal Name:	**ESIBRD**
Signal Description:	**Extended System Information Bus Read**
Signal Type:	**Input/Output**

Used to group two to eight SCTs into a bus-sharing mode for alarm and status reporting.

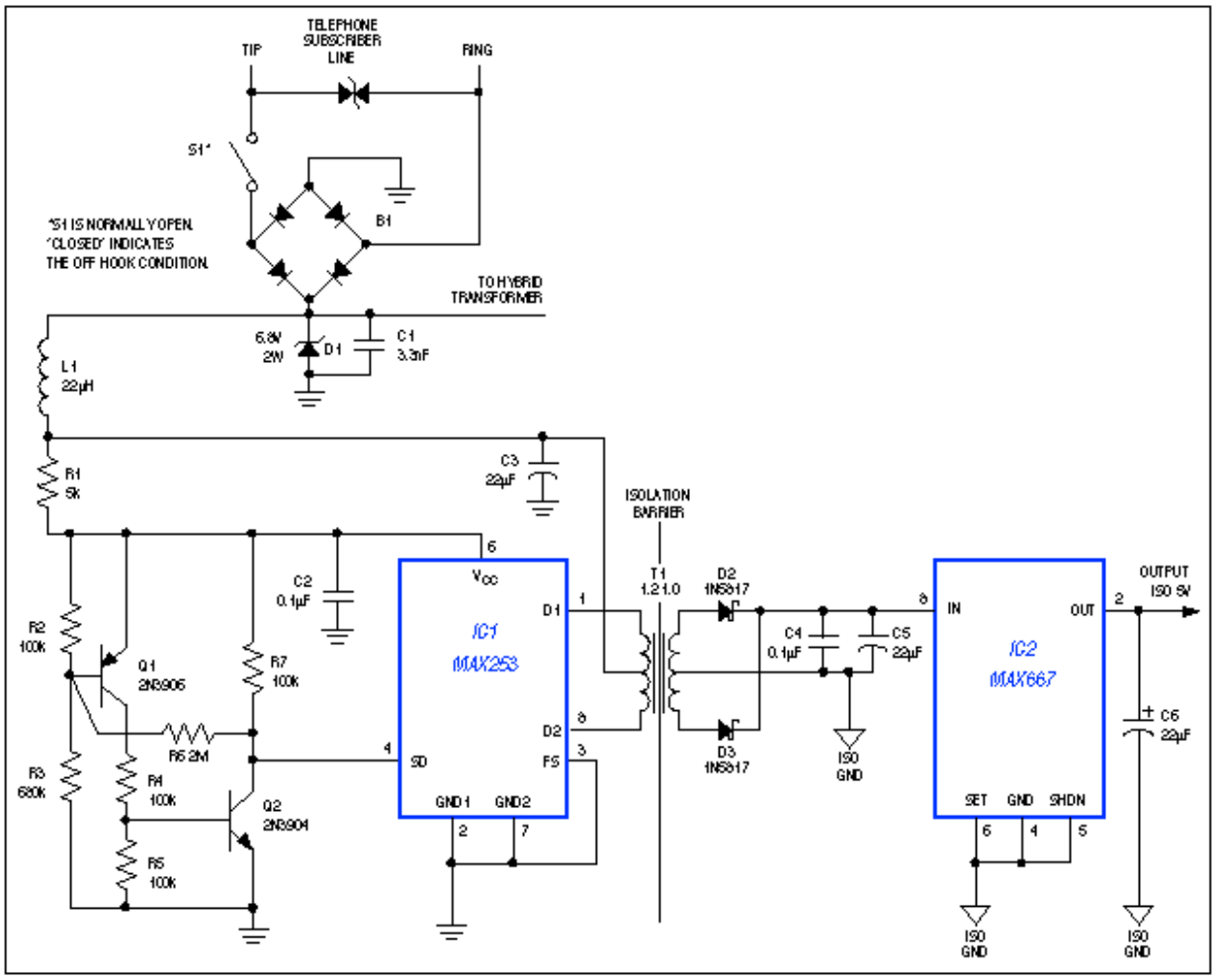

Figure 1. ESIB pin connection.

Interrupt Handling

Status registers are the only sources of interrupts in devices with the ESIB feature. On power-up, all writeable registers are automatically cleared. Since bits in the IMRx registers have to be set = 1 to allow a particular event to cause an interrupt, no interrupts can occur until the host selects which events are to product interrupts. Since there are potentially many sources of interrupts, several ESIB functions are

available to help sort out and identify which event is causing an interrupt. When an interrupt occurs, the host should first read the IIR1 and IIR2 registers (interrupt information registers) to identify which status register (or registers) is producing the interrupt. Once that is determined, the individual status register or registers can be examined to determine the exact source. Once an interrupt has occurred, the interrupt handler routine should set the INTDIS bit (CCR3.6) to stop further activity on the interrupt pin. After all interrupts have been determined and processed, the interrupt hander routine should re-enable interrupts by setting the INTDIS bit = 0.

ESIB Registers

Register Name: **ESIBCR1**
Register Description: **Extended System Information Bus Control Register 1**
Register Address: **B0h**

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	ESIBSEL2	ESIBSEL1	ESIBSEL0	ESIEN
Default	0	0	0	0	0	0	0	0

Bit 0/Extended System Information Bus Enable (ESIEN)

0 = disabled
1 = enabled

Bits 1 to 3/Output Data Bus Line Select (ESIBSEL0 to ESIBSEL2). These bits tell the SCT what data bus bit to output the ESIB data on when one of the ESIB information registers is accessed. Each port in the ESIB group must have a unique bit selected.

ESIBSEL2	ESIBSEL1	ESIBSEL0	Bus Bit Driven
0	0	0	AD0
0	0	1	AD1
0	1	0	AD2
0	1	1	AD3
1	0	0	AD4
1	0	1	AD5
1	1	0	AD6
1	1	1	AD7

Bits 4 to 7/Unused, must be set to 0 for proper operation

Register Name: **ESIBCR2**
Register Description: **Extended System Information Bus Control Register 2**
Register Address: **B1h**

Bit #	7	6	5	4	3	2	1	0
Name	--	ESI4SEL2	ESI4SEL1	ESI4SEL0	--	ESI3SEL2	ESI3SEL1	ESI3SEL0
Default	0	0	0	0	0	0	0	0

Bits 0 to 2/Address ESI3 Data Output Select (ESI3SEL0 to ESI3SEL2). These bits select what status is to be output when the SCT decodes an ESI3 address during a bus read operation.

ESI3SEL2	ESI3SEL1	ESI3SEL0	STATUS OUTPUT	
			T1 MODE	E1 MODE
0	0	0	RBL	RUA1
0	0	1	RYEL	RRA
0	1	0	LUP	RDMA
0	1	1	LDN	V52LNK
1	0	0	SIGCHG	SIGCHG
1	0	1	ESSLIP	ESSLIP
1	1	0	--	--
1	1	1	--	--

Bit 3/Unused, must be set to 0 for proper operation

Bits 4 to 6/Address ESI4 Data-Output Select (ESI4SEL0 to ESI4SEL2). These bits select what status is to be output when the SCT decodes an ESI4 address during a bus read operation.

ESI4SEL2	ESI4SEL1	ESI4SEL0	STATUS OUTPUT	
			T1 MODE	E1 MODE
0	0	0	RBL	RUA1
0	0	1	RYEL	RRA
0	1	0	LUP	RDMA
0	1	1	LDN	V52LNK
1	0	0	SIGCHG	SIGCHG
1	0	1	ESSLIP	ESSLIP
1	1	0	--	--
1	1	1	--	--

Bit7/Unused, must be set to 0 for proper operation

Register Name: **ESIB1**
Register Description: **Extended System Information Bus Register 1**
Register Address: **B2h**

Bit #	7	6	5	4	3	2	1	0
Name	DISn	DISn	DISn	DISn	DISn	DISn	DISn	DISn
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Device Interrupt Status (DISn). Causes all devices participating in the ESIB group to output their interrupt status on the appropriate data bus line selected by the ESIBSEL0 to ESIBSEL2 bits of the ESIBCR1 register.

Register Name: **ESIB2**
Register Description: **Extended System Information Bus Register 2**
Register Address: **B3h**

Bit #	7	6	5	4	3	2	1	0
Name	DRLOSn	DRLOSn	DRLOSn	DRLOSn	DRLOSn	DRLOSn	DRLOSn	DRLOSn
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/Device Receive Loss-of-Sync (DRLOSn). Causes all devices participating in the ESIB group to output their frame synchronization status on the appropriate data bus line selected by the ESIBSEL0 to ESIBSEL2 bits of the ESIBCR1 register.

Register Name: **ESIB3**
Register Description: **Extended System Information Bus Register 3**
Register Address: **B4h**

Bit #	7	6	5	4	3	2	1	0
Name	UST1n	UST1n	UST1n	UST1n	UST1n	UST1n	UST1n	UST1n
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/User-Selected Status 1 (UST1n). Causes all devices participating in the ESIB group to output status or alarms as selected by the ESI3SEL0 to ESI3SEL2 bits in the ESIBCR2 configuration register on the appropriate data bus line selected by the ESIBSEL0 to ESIBSEL2 bits of the ESIBCR2 register.

Register Name: **ESIB4**
Register Description: **Extended System Information Bus Register 4**
Register Address: **B5h**

Bit #	7	6	5	4	3	2	1	0
Name	UST2n	UST2n	UST2n	UST2n	UST2n	UST2n	UST2n	UST2n
Default	0	0	0	0	0	0	0	0

Bits 0 to 7/User-Selected Status 2 (UST2n). Causes all devices participating in the ESIB group to output status or alarms as selected by the ESI4SEL0 to ESI4SEL2 bits in the ESIBCR2 configuration register on the appropriate data bus line selected by the ESIBSEL0 to ESIBSEL2 bits of the ESIBCR2 register .

Conclusion

This application note has shown how the ESIB allows ease of status updates of certain registers, as well as other user-selectable alarm status information, within a predefined group of single-chip transceivers.

If you have further questions about ESIB control, please contact the Telecommunication Applications support team.

DS2155/DS21Q55 Information
For more information about the DS2155/DS21Q55, please consult the DS2155 and DS21Q55 data sheets available on our website at www.maximintegrated.com/telecom.

Related Parts		
DS2155	T1/E1/J1 Single-Chip Transceiver	Free Samples
DS21Q55	Quad T1/E1/J1 Transceiver	

More Information
For Technical Support: http://www.maximintegrated.com/support
For Samples: http://www.maximintegrated.com/samples
Other Questions and Comments: http://www.maximintegrated.com/contact

Application Note 401: http://www.maximintegrated.com/an401
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