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APPLICATION NOTE 4002

Understanding Flip-Chip and Chip-Scale Package Technologies and Their Applications

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Abstract: Driven by the trend to smaller, lighter, and thinner consumer products, smaller package types have been developed. Indeed, packaging has become a key determinant for using or abandoning a device in a new design. This article first defines the terms "flip chip" and "chip-scale package" and explains the technical development of wafer-level packaging (WLP) technology. Next it discusses practical aspects of using wafer-level packaged devices. Topics in that discussion include: determining the availability of flip-chip/UCSP™ packaging for a given device; identifying a flip chip/UCSP by its marking; the reliability of wafer-level packaged parts; and finding applicable reliability information. The document concludes with an outlook on future packaging developments, references to documents used in writing this application note, and links to additional literature that addresses topics not discussed here.

Introduction

The advance in semiconductor technology has created chips with transistor counts and functions that were unthinkable a few years ago. Portable electronics, as we know it today, would not be possible without equally exciting developments in IC packaging. Driven by the trend towards smaller, lighter, and thinner consumer products, smaller package types have been developed. The smallest possible package will always be the size of the chip itself. **Figure 1** illustrates the steps that take an IC from wafer to individual chip. **Figure 2** shows an actual chip-scale package (CSP).

The concept of chip-size packaging evolved in the 1990s. Among the CSP categories that were defined by 1998, the wafer-level CSPs emerged as economical choices for a wide variety of applications from low-pin-count devices, such as EEPROMs, to ASICs and microprocessors. CSP devices are manufactured in a process called wafer-level packaging (WLP). The major benefit of WLP is that all package fabrication and testing is done on wafer. The cost of WLP drops as the wafer size increases and as the die shrinks. As an early adopter of the technology, Dallas Semiconductor started shipping wafer-level packaged products in 1999.

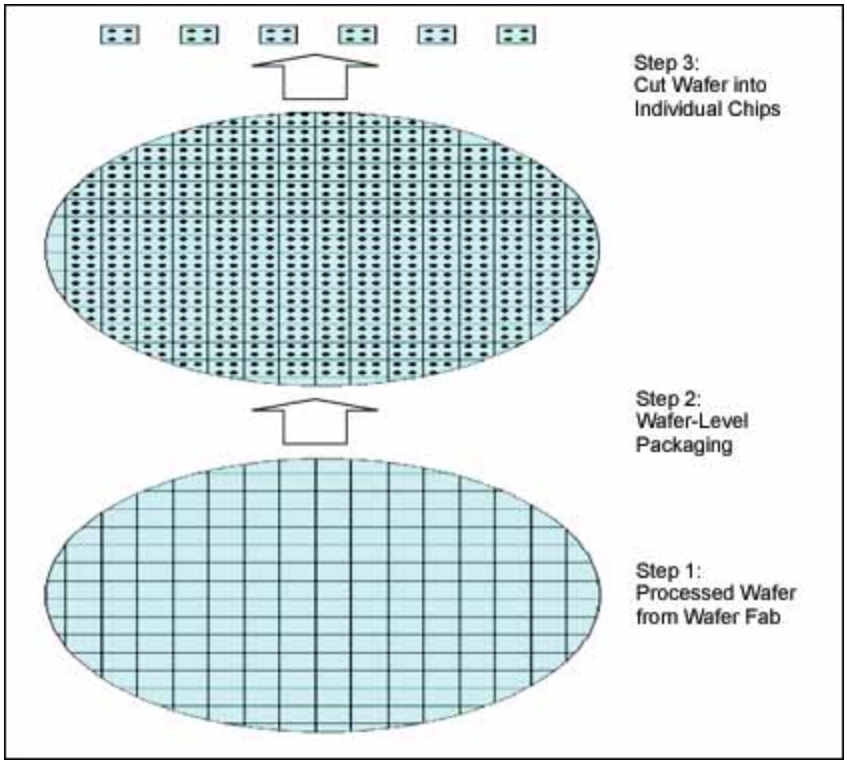

Figure 1. Wafer-level packaging (simplified) ultimately separates individual chips from the processed wafer.

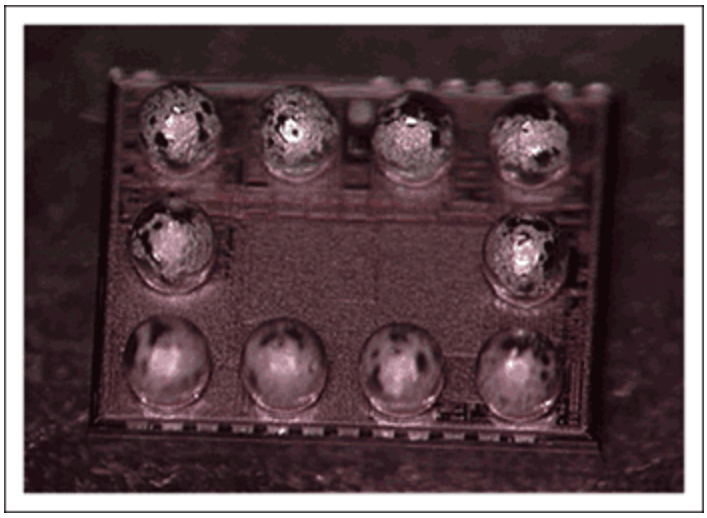

Figure 2. A 12-bump chip-scale package, 3 × 4 bumps, with 2 bump locations not populated.

Nomenclature

There is still confusion in the industry over the nomenclature of WLP. Wafer-level approaches for CSPs are unique because there is no bonding technique inside the package. Further confusion exists on what to call the packaged chip. Frequently used descriptive names are: flip chip (STMicroelectronics and Dallas Semiconductor®), CSP, chip-scale package, WLCSP, WL-CSP, MicroSMD (National Semiconductor), UCSP (Maxim Integrated Products), bumped die, and MicroCSP (Analog Devices).

At Maxim®/Dallas Semiconductor, the terms "flip chip" and "chip-scale package" were initially used synonymously for all types of wafer-level packaged dies. Over the years, further distinction developed for the packages. Within this document and in all Maxim materials, including the Company's website, the term "flip chip" describes a wafer-level packaged die with **bumps of any shape that can sit at any location** (with clearances to the edges). The term "chip-scale package" describes a wafer-level packaged die with **spherical bumps** located on a **grid** with a predefined pitch. **Figure 3** illustrates these differences. Note that not all grid locations need to be populated.

The flip-chip dimensions in Figure 3 reflect the *first generation* of Dallas Semiconductor WLP products; the chip-scale package dimensions are compiled from various vendors, including Maxim. Key dimensions of current Maxim and newer Dallas Semiconductor chip-scale packaged products are shown in **Table 1**.

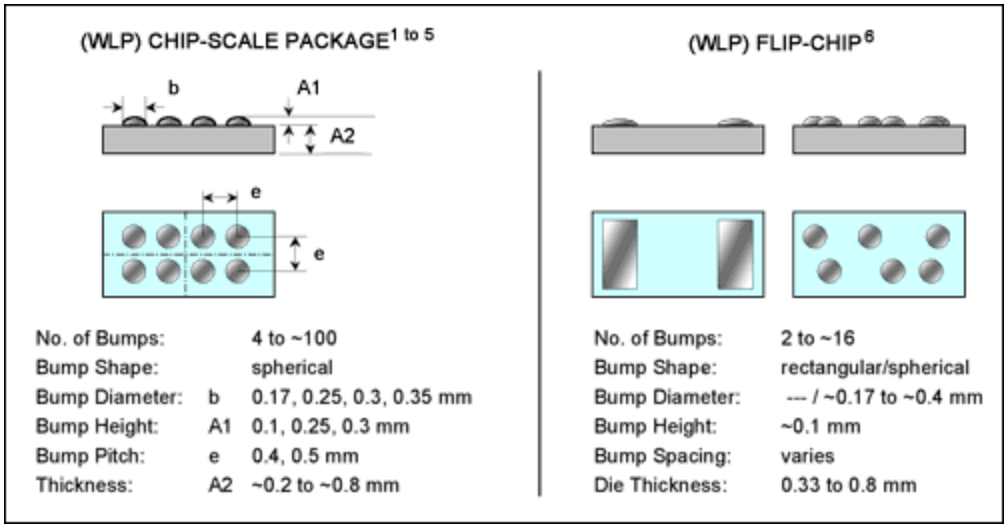

Figure 3. Illustration shows the typical dimensions and differences between a chip-scale package and a flip-chip package.

Table 1. Maxim and Dallas Semiconductor UCSP (Chip-Scale Package) Nominal Dimensions[7]

Parameter	Designator	Value
No. of Bumps	(---)	4 to 36
Bump Diameter	b	0.30, 0.35mm
Bump Height	A1	0.25, 0.3mm
Bump Pitch	e	0.5mm
Die Thickness	A2	0.33, 0.38mm

Wafer-Level Packaging (WLP) Technology

Vendors that offer WLP parts have either their own WLP fab or outsource the packaging process. Accordingly, the manufacturing processes vary, as do the requirements that the users must meet to ensure reliability of the end product. An interesting overview on the past and future of WLP is found in the articles *Wafer-Level Packaging Has Arrived,*[8] *The Wafer-Level Packaging Evolution*,[9] and *WLCSP Technology Direction*.[10] FCI in Phoenix, Arizona, and Unitive® at Research Triangle Park, North Carolina, created standards in WLP technology under the product names UltraCSP (FCI) and Xtreme (Unitive). Amkor, which acquired Unitive, offers its WLP service to the semiconductor industry

worldwide.[11]

The bumps that connect the chip to the traces on the circuit/wiring board were originally made from an eutectic* alloy of tin and lead (Sn63Pb37). Initiatives to reduce the contents of hazardous substances in electronic products (RoHS) are forcing the semiconductor industry to adopt alternatives, such as Pb-free bumps (Sn96.5Ag3Cu0.5) or high-Pb bumps (Pb95Sn5). Each alloy has its own melting point and, therefore, requires a specific temperature profile (duration at the specific temperatures) in the component assembly reflow process.

Integrated circuits are designed to provide all the electrical functions needed and to fit into a specific set of packages. The bond pads on the chip are connected to the pins of a conventional package through wire bonding. Design rules for conventional packages require the bond pads to be located at the perimeter of a chip. To avoid two designs for the same chip (one for conventional packages and one for the CSP), a redistribution layer is generally required to connect bumps to bond pads.

Determining Flip Chip/UCSP Availability, Lead-Free Compliance

Only a small percentage of Maxim/Dallas Semiconductor devices is available as flip chip or UCSP. The easiest way to verify package availability is through the QuickView function for a device on the Company website. After a part number search, a QuickView data sheet is displayed, which includes a short device description, key features, package options, URLs to application notes, links to more information (such as reliability reports, evaluation kits). The top right of the QuickView gives access to the Part Number Table. If multiple part numbers share a data sheet, the Part Number Table has a drop-down box for selecting specific part numbers. Clicking on Go opens a window that displays the ordering part numbers, package descriptions, URLs to package drawings, temperature range, and whether the package is lead-free. Look for FCHIP or UCSP. The flip-chip/UCSP package designator for Dallas Semiconductor parts is an "X". Maxim UCSPs typically have a "B" in the suffix that follows the numerical portion of the part number.[12] Package drawings accessible from the Part Number Table always include orientation information. Since UCSP drawings typically apply to multiple devices with slightly different die sizes, the electrical assignment of the bumps is not included; that information is found in the device's data sheet. As flip-chip drawings apply only to a specific chip, the drawings do typically include electrical assignments.

Flip-Chip/UCSP Topmark (Device Identification)

Most flip chips and UCSPs do not have space for the conventional marking that is common with plastic packages. The smallest UCSPs (4 bumps) have just enough space for an orientation mark and a 6-character code spread over two lines. The orientation mark also indicates whether a package is "standard" (eutectic bumps), high-Pb (#), or Pb-free (+). See **Figure 4**.

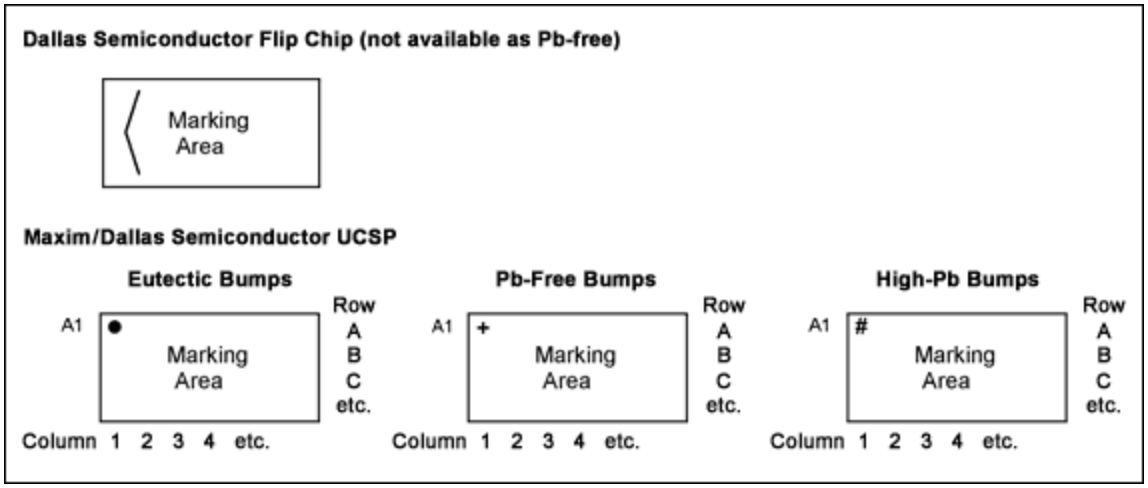

Figure 4. Flip chip and UCSP marking templates.

The Topmark Coding for UCSPs is typically accessible from the **More Information** section of the QuickView. In some cases, the information is also included in data sheets. For a reverse lookup, i.e., determining the device's package from the topmark, one can either use the web-based Topmark Coding function or download the complete topmark table[13] and use a search function to identify the corresponding device(s). A topmark code is used for UCSPs with up to 12 bumps. Larger UCSPs have sufficient space to brand a full part number plus date code and lot information. **Table 2** shows the brands used for Maxim parts.

Table 2. Typical Maxim UCSP Brands

Maxim Brand		Legend
2-lines	mmm nxx	
3-lines	mmm nxx YWW	
4-lines	pppp sss nxx YWW	**mmm** Topmark code **pppp** Part number (numeric portion only) **sss** Part number suffix **n** Production-related code, number **xx** Production-related code, letters **YWW** Date code If branded, "MAX" is in the same line as the A1 marker.
4-lines, alternate	pppp sss n YWW xxxxx	
5-lines	MAX pppp sss n YWW	

xxxxx	

The branding style shown in **Table 3** applies to Dallas Semiconductor flip chips and UCSPs. The laser marking is very small and requires a magnifying glass to read it. Dallas Semiconductor's flip chips use a similar approach for the smallest devices; the 2-digit device code (also known as Family Code) is branded followed by a die revision code. This approach does not require a cross-reference list.

Table 3. Typical Dallas Semiconductor Flip-Chip and UCSP Brands

Dallas Semiconductor Brand		Legend	
1-line	dcrrδ	**dc**	2-digit device (family) code
2-lines	DSpppp rrδ#xx	**pppp**	Part number (numeric portion only)
		YYWW	Date code
		δ	Alternate date code
3-lines	DSppppp yywwrr ###xx	**rr**	Die revision code
		###xx	Production-related code

Reliability of Wafer-Level Packaged Parts

The wafer level package (flip chip and UCSP) represents a unique packaging form factor that might not perform equally to a packaged product through traditional mechanical reliability tests. The package's reliability is integrally linked to the user's assembly methods, circuit-board material, and usage environment. The user should closely review these issues when considering use of WLP parts. Performance through Operating Life Test and Moisture Resistance remains uncompromised, as it is primarily determined by the wafer-fabrication process.

Mechanical stress performance is a greater concern for a WLP. Flip chips and UCSPs are attached through direct solder contact to the user's PC board, thus foregoing the inherent stress relief of a packaged product lead frame. Solder-joint contact integrity must, therefore, be considered. Further information on board layout considerations, assembly process flow, solder paste screen printing, component placement, reflow temperature profile requirements, epoxy encapsulation, and visual inspection acceptance criteria is found in the Dallas Semiconductor Wafer-Level Package Assembly Guide.[14] Information on Maxim's qualification plan and test data is detailed in Application Note 1891.[15] Reliability information is accessed from product QuickViews, on the "Technical Documents" tab. If information on the flip chip, UCSP, or WLP version is not found, request a report using the support center.

Conclusion

Today flip chips and CSP remain a novel technology with continuing development. Improvements already underway will apply a backside lamination coating (BSL), which protects the inactive side of the die against light and mechanical impact and improves the readability of the laser marking under brightfield illumination. Along with BSL, one should expect a reduced die thickness to keep the overall assembly height unchanged. The Maxim UCSP dimensions (see Table 1) describe the package conditions as of February 2007. Following the general trend in the industry, these dimensions are likely to shrink. Therefore, it is crucial that a designer verifies actual package dimensions from the respective package drawings before finishing the circuit-board layout. In addition, it is important to know the specific alloy composition of the bump die WLP, especially if a device is not advertised and marked as Pb-free. Some devices with high-Pb bumps (Pb95Sn5) have been tested with a Pb-free board assembly reflow process

and were found compatible without significantly affecting their reliability.[16, 17] Devices with eutectic SnPb bumps require a similar eutectic SnPb solder paste and are, therefore, not compatible to a Pb-free assembly environment.

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2. National Semiconductor, AppNote 1281 (PDF, 225kB)
3. National Semiconductor, AppNote 1412 (PDF, 828kB)
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5. STMicroelectronics, AppNote 2348 (PDF, 333kB)
6. Maxim Integrated Products, FCHIP drawings
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11. Amkor Technology, Wafer Level Packaging Data Sheet
    - Select "Data Sheet" in the Wafer Level Packaging Data Sheet
    - Click on "Open Data Sheet"
12. Maxim Product Naming Conventions
13. Topmark Cross-Reference Table
    - Use section 1. Topmark to Part Number and enter the entire topmark, with + or # (if found) preceeding the code Do not rely on the complete listing, because it is no longer maintained.
14. Application note 3377, "Maxim Wafer-Level Package Assembly Guide"
15. Application note 1891, "Wafer-Level Packaging (WLP) and Its Applications"
16. Application note 3505, "Assembling High-Lead (Pb) DS2502 Flip-Chips in a Pb-Free Assembly Flow"
17. Application note 3599, "Assembling High-Lead (Pb) DS2761 Flip-Chips in a Pb-Free Assembly Flow"

*The term "eutectic" is used in metallurgy to describe the alloy of two or more component materials having the relative concentrations specified at the eutectic point. When a noneutectic alloy changes from liquid to solid, one component of the alloy crystallizes at one temperature and the other at a different temperature. With a eutectic alloy, the mixture solidifies as one at a single temperature having a sharp melting point. This contrasts to a noneutectic alloy, which exhibits a plastic melting range. (Adapted from http://www.answers.com/topic/eutectic-point)

The DS2430A is no longer recommended for new designs.

Related Parts		
DS1804	Nonvolatile Trimmer Potentiometer	Free Samples
DS1845	Dual NV Potentiometer and Memory	Free Samples
DS2401	Silicon Serial Number	Free Samples
DS2411	Silicon Serial Number with V_{CC} Input	Free Samples
DS2417	1-Wire Time Chip With Interrupt	Free Samples
DS2430A	256-Bit 1-Wire EEPROM	
DS2431	1024-Bit 1-Wire EEPROM	Free Samples
DS2432	1Kb Protected 1-Wire EEPROM with SHA-1 Engine	Free Samples
DS2482-100	Single-Channel 1-Wire Master	Free Samples
DS2482-101	Single-Channel 1-Wire® Master with Sleep Mode	Free Samples
DS2502	1Kb Add-Only Memory	Free Samples
DS2762	High-Precision Li+ Battery Monitor with Alerts	Free Samples

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