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APPLICATION NOTE 389

DS2155 Internal BERT Programming

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Abstract: Application note 389 describes how to use the internal Bit Error Rate Test (BERT) controller found in the Dallas Semiconductor DS2155 T1/E1/J1 single chip transceiver (SCT). Testing the bit error rate of a line which carries voice or data traffic determines how well the line will perform in actual use. Each line must meet a minimum level of performance before it can be used in a telecommunications system. In most designs, a separate device is used to interface with the transceiver but with the DS2155, these functions are built into the device. The application note contains step-by-step instructions of how to program the DS2155 internal BERT and perform a simple bit error rate test. It explains all of the choices that need to be made and gives detailed information on the internal registers used for each operation. In the end, the designer should have enough information to implement the necessary bit error rate test in the target system.

Overview

One of the new features inside the DS2155 single-chip transceiver is the bit error-rate tester (BERT). The BERT can be used to generate pseudorandom patterns, repetitive patterns, alternating word patterns, and the modified 55 octet (Daly) pattern. While the DS2155 BERT does not contain all of the capabilities of the Dallas Semiconductor standalone BERT devices such as the DS2172 and DS2174, it does provide many of the common patterns used in telecom test systems. This document contains the steps necessary to initialize the DS2155 BERT and start the bit error-rate testing process.

Programming the DS2155 BERT

1. Enable the BERT, configure the BERT direction, and, if in T1 mode, configure the BERT for framed or unframed operation using the BERT interface control register (BIC @ 0xEA).
2. Select the desired BERT pattern using the pattern-select bits located in BERT Control Register 1 (BC1.4-BC1.2 @ 0xE0).
    1. When using a pseudorandom pattern, the repetitive-pattern set registers (BRP1-BRP4 @ 0xDC-0xDF) should all be set to 0xFF.
    2. When using a repetitive pattern, it is necessary to load the pattern using the repetitive-pattern set registers (BRP1-BRP4 @ 0xDC-0xDF) and to set the pattern length using the repetitive-pattern length bits in BERT Control Register 2 (BC2.3-BC2.0 @ 0xE1). If the pattern is not 32 bits in length it should be repeated until all 32 bits are used and the repetitive-pattern length bits should be set to a multiple of the actual pattern length.
    3. When using a repetitive word pattern, one word should be loaded into repetitive-pattern set registers 1 and 2 (BRP1-BRP2 @ 0xDC-0xDD). The second word should be loaded into repetitive-pattern set registers 3 and 4 (BRP3-BRP4 @ 0xDE-0xDF). The BERT alternating

count-rate register also needs to be set to the number of times each word repeat.

3. Using the special per-channel operation functions, each channel can be individually configured to transmit and receive BERT data. Set the per-channel pointer register (PCPR @ 0x28) to 0x11 to configure the channels to transmit and receive BERT data. Use the per-channel data registers (PCDR1-PCDR4 @ 0x29-0x2C) to assign the channels that contain BERT data.
4. Toggle the transmit pattern load bit located in BERT Control Register 1 (BC1.7 @ 0xE0) from low to high to load the pattern into the BERT transmitter.
5. Toggle the force resynchronization bit located in BERT Control Register 1 (BC1.0 @ 0xE0) from low to high to resynchronize the BERT receiver.
6. Read the BERT-in-synchronization bit located in Status Register 9 (SR9.0 @ 0x26) and wait until this bit is set to 1, which indicates that the BERT receiver has matched the proper pattern.
7. Toggle the load bit and error counters bit located in BERT Control Register 1 (BC1.1 @ 0xE0) from low to high to clear the bit and error counters. This resets and starts a new bit and error count cycle. It also latches the current bit count into the BERT bit count registers and current error count into the BERT error count registers, which at this point contain garbage values and should be ignored.
8. Select the desired method for running BERT test.
    1. The test can either be run for a set time period based on an external system.
    2. Status Register 9 (SR9 @ 0x26) can be monitored for different events that pertain to the operation of the BERT. Along with Status Register 9, Interrupt Mask Register 9 (IMR9 @ 0x27) can be used to trigger interrupts based on the events reported in Status Register 9.
9. Toggle the load bit and error counters bit located in BERT Control Register 1 (BC1.1 @ 0xE0) from low to high. This latches the current bit count into the BERT bit count registers (BBC1-BBC4 @ 0xE3-0xE6) and the current error count into the BERT error count registers (BEC1-BEC3 @ 0xE7-0xE9). These two values contain the statistical information about the BERT test. Since this bit also resets the counters, it can be necessary to store these values in external memory allow for longer test periods. The new values would just be added to previously stored values.
10. Steps 8 and 9 can be repeated for long test periods.
11. If it is necessary to insert a specific error rate or a single bit error into the transmitted stream, the single bit-error insert bit located in BERT Control Register 2 (BC2.4 @ 0xE1) or error insert bits located in BERT Control Register 2 (BC2.5-BC2.7 @ 0xE1) can be used.

Related Parts		
DS2155	T1/E1/J1 Single-Chip Transceiver	Free Samples
DS2156	T1/E1/J1 Single-Chip Transceiver TDM/UTOPIA II Interface	Free Samples
DS21Q55	Quad T1/E1/J1 Transceiver	

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