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APPLICATION NOTE 374

DS2155 vs. DS21x5y: Software and Hardware Considerations

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Abstract: Application note 374 describes the hardware and software considerations when upgrading an existing DS21x5y design to use the DS2155 device. The Dallas Semiconductor DS2155 T1/E1/J1 single chip transceiver (SCT) has a broader feature set and as such the designer must make changes in software and hardware when migrating to the DS2155 from the DS21x5y device. Any designer who is thinking of upgrading an existing design to use the DS2155 should read this application note. The application note contains detailed information for software migration such as: register location changes, how individual functions have changed from the DS21x5y to the DS2155, and which new functions are available on the DS2155. It also covers migration for the hardware interface and covers topics such as: interfacing with other devices, changes to the line interface, and new functions that are available in the DS2155. In the end, the designer should have enough information to easily migrate an existing design which uses the DS21x5y to the DS2155 device.

This note uses the device number DS21x52 to refer to both the DS21352 and DS21552. Also, references to DS21x54 will correspond to both the DS21354 and DS21554. Whenever DS21x5y is used, it refers to all the parts mentioned above.

1. Overview

The DS2155 is a software selectable T1, J1 or E1 Single Chip Transceiver (SCT) for short and long haul applications. This application note intends to highlight many of the differences between the DS2155 and the previous family of Dallas Semiconductor's SCTs. While, the DS2155 is pin compatible with previous Dallas Semiconductor SCT's (DS2152/54, DS21352/552, & DS21552/554) the register set for the device is much more complex. In the following pages, we will identify features from the DS21x5y devices and pinpoint their register locations in the DS2155. Additionally, some of the new features available in the DS2155 and what provisions need to be made existing DS21x5y designs or new designs in order to use the DS2155 will be discussed. This note is broken into 4 sections. First, the location of DS21x52 (T1) and DS21x54 (E1) features will be linked to the DS2155 register map. The note will then discuss some of the new features that are available to users in all modes of operation. The last section deals with hardware considerations when using the DS2155.

1.1 Contents

1.2 How to Read the Register Mapping Tables

This note will discuss each register of the DS21x52 and DS21x54 SCTs. In some cases the entire register has been kept intact, but has been relocated to a new address. For these cases the new address of the register in the DS2155 along with the DS2155 register abbreviation will be listed. In other cases, single bits from the registers have been relocated to different address. If a bit has been relocated, the DS21x5y register will be presented in the following manner. First, two lines identifying the DS21x5y

registers abbreviation, name and hexadecimal address will be given, followed by a register table consisting of 4 rows will follow. The first row of the register table will always be the same and will identify the control bit position in the DS21x5y register. Row 2 will contain the control bit name within the DS21x5y register. The last 2 rows in the register table identify where to find the control bit in the DS2155. Row 3 provides the user with the DS2155's abbreviated register name where the control bit can be found. The last row gives the address and bit number of the new location. For example, a bit that has been relocated in the DS2155 to bit position 3 in the register at the location of address A5 Hex would have the value A5.3 placed in the 55 Addr.Bit row.

DS21x5y Register: *RE: Register Example*
DS21x5y Register Address: *xx Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	B7	NEWREG	addr.bit
6	B6	NEWREG	addr.bit
5	B5	NEWREG	addr.bit
4	B4	NEWREG	addr.bit
3	B3	NEWREG	addr.bit
2	B2	NEWREG	addr.bit
1	B1	NEWREG	addr.bit
0	B0	NEWREG	addr.bit

If the functionality and/or name of the control bit has changed or if additional information is required, it will be indicated by an * in the register table. The additional information for these control bits will be presented below the register table.

2. Software Considerations: DS2155 vs. DS21x52 (T1)

This section will present the registers for the DS21352 and DS21552. The registers are presented in the order that they appear in the DS21352 and DS21552 data sheet.

ID Register

DS21x52 Register: *IDR: Device Identification Register*
DS21x52 Register Address: *0F Hex*

The Device Identification Register (IDR) for the DS2155 is located at the same address as the IDR for the DS21x52. The upper four bits display the DS2155 ID (1011) and the lower four bits display the die revision.

Receive Control Registers

DS21x52 Register: *RCR1: Receive Control Register 1*
DS21x52 Register Address: *2B Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	LCVCRF	ERCNT	41.0
6	ARC	T1RCR1	03.6
5	OOF1	T1RCR1	03.5

4	OOF2	T1RCR1	03.4
3	SYNCC	T1RCR1	03.3
2	SYNCT	T1RCR1	03.2
1	SYNCE	T1RCR1	03.1
0	RESYNC	T1RCR1	03.0

DS21x52 Register: *RCR2: Receive Control Register 2*
DS21x52 Register Address: *2C Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	RCS	*See below*	*See below*
6	RZBTSI	T1RCR2	04.2
5	RSDW	IOCR1	01.6*
4	RSM	IOCR1	01.5*
3	RSIO	IOCR1	01.4
2	RD4YM	T1RCR2	04.0
1	FSBE	ERCNT	41.2
0	MOSCRF	ERCNT	41.1

- RSM, bit 4, has been renamed as RSMS1. There is no new functionality associated with the bit.
- RSDW, bit 5, has been renamed as RSMS2. There is no new functionality associated with the bit.
- RCS, bit 7, was used to generate either a 7F idle code or the digital milliwatt pattern. In the DS2155, the digital milliwatt pattern is generated using the T1RDMR1 (0C Hex), T1RDMR2 (0D Hex), and T1RDMR3 (0E Hex) registers. See section 10.1 of the DS2155 data sheet for more information on generating the digital milliwatt pattern. Idle code generation has changed in the DS2155. See section 18 of the DS2155 data sheet for more information.

Transmit Control Registers

DS21x52 Register: *TCR1: Transmit Control Register 1*
DS21x52 Register Address: *35 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	LOTCMC	CCR1	See below
6	TFPT	T1TCR1	05.6
5	TCPT	T1TCR1	05.5
4	TSSE	T1TCR1	05.4
3	GB7S	T1TCR1	05.3
2	TFDLS	T1TCR1	05.2
1	TBL	T1TCR1	05.1
0	TYEL	T1TCR1	05.0

- LOTCMC, bit 7, has been combined with other functions to simplify the selection of the transmit clock source. The two bits, Transmit Clock Source Select 0 (TCSS0) and Transmit Clock Source Select 1 (TCSS1), are located in the DS2155's Common Control Register 1 (CCR1, address 70

Hex) in bit positions 1 and 2 respectively.

DS21x52 Register: *TCR2: Transmit Control Register 2*
DS21x52 Register Address: *36 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	TEST1	MSTRREG	00.3
6	TEST0	MSTRREG	00.2
5	TZBTSI	T1TCR2	06.1
4	TSDW	IOCR1	01.3
3	TSM	IOCR1	01.2
2	TSIO	IOCR1	01.1
1	TD4YM	T1TCR2	06.2
0	TB7ZS	T1TCR2	06.0

Common Control Registers

DS21x52 Register: *CCR1: Common Control Register 1*
DS21x52 Register Address: *37 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	TESE	ESCR	4F.4
6	ODF	IOCR1	01.0
5	RSAO	PCPR	28.7*
4	TSCLKM	IOCR2	02.1
3	RSCLKM	IOCR2	02.0
2	RESE	ESCR	4F.0
1	PLB	LBCR	4A.1
0	FLB	LBCR	4A.0

- RSAO, bit 5, has been renamed as RSAOICS and been placed in the Per-Channel Pointer Register. In the DS21x52, setting the RSAO bit would force all of the extracted robbed-bit signaling positions to one. If the user wished to invoke this option on a per-channel basis, the RPCSI control bit in CCR4.6 and the receive channel blocking registers had to be set accordingly. In the DS2155, the user sets the RSAOICS bit and then selects, via the Per-Channel Data Register 1-3, the channels in which to force the robbed-bit signaling bits to one. See section 7 of the DS2155 data sheet for more information on per-channel operation.

DS21x52 Register: *CCR2: Common Control Register 2*
DS21x52 Register Address: *38 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	TFM	T1CCR1	07.2
6	TB8ZS	T1TCR2	06.7
5	TSLC96	T1TCR2	06.6
4	TFDL	T1TCR2	06.5*

3	RFM	T1RCR2	04.6
2	RB8ZS	T1RCR2	04.5
1	RSLC96	T1RCR2	04.4
0	RZSE	T1RCR2	04.3

- TFDL, bit 4, has been renamed as TZSE. No additional functionality has been associated with this bit.

DS21x52 Register: *CCR3: Common Control Register 3*
DS21x52 Register Address: *30 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	RESMDM	ESCR	4F.1
6	TCLKSRC	CCR1	*See Below*
5	RLOSF	CCR1	70.0
4	RSMS	IOCR1	01.7
3	PDE	T1CCR1	07.1
2	ECUS	ERCNT	41.5
1	TLOOP	T1CCR1	07.0
0	TESMDM	ESCR	4F.5

- TCLKSRC, bit 6, has been combined with other functions to simplify the selection of the transmit clock source. Two bits, Transmit Clock Source Select bit 0 (TCSS0) and bit 1 (TCSS1) are located in the DS2155's Common Control Register 1 (CCR1, address 70 Hex) in bit positions 1 and 2 respectively.

DS21x52 Register: *CCR4: Common Control Register 4*
DS21x52 Register Address: *11 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	RSRE	PCPR	28.6*
6	RPCSI	*See Below*	*See Below*
5	RFSA1	*See Below*	*See Below*
4	RFE	SIGCR	40.4
3	RFF	SIGCR	40.3
2	THSE	PCPR	28.3*
1	TPCSI	*See Below*	*See Below*
0	TIRFS	*See Below*	*See Below*

- Control bit 0, TIRFS, has been incorporated in the new functionality for idle code generation. See section 18 of the DS2155 data sheet for more detail.
- Control bit 1, TPCSI, has been incorporated into the per-channel register operation. See sections 7 and 17 of the DS2155 data sheet for additional information.
- THSE, bit 2, has been renamed as THSCS. See sections 7 and 17 of the DS2155 data sheet for information on per-channel register operation.

- RFSA, control bit 5, has been incorporated into the per-channel register function. The user sets the BTCS bit in the PCPR register and selects the channels which are to be forced to one by writing to the PCDR1-PCDR3 registers. See sections 7 and 17 of the DS2155 data sheet for additional information.
- RPCSI, bit 6, has been incorporated into the per-channel register function. See sections 7 and 17 of the DS2155 data sheet for additional information.
- RSRE, bit 7, has been renamed as RSRCS. See sections 7 and 17 of the DS2155 data sheet for additional information on receive signaling re-insertion.

DS21x52 Register: *CCR5: Common Control Register 5*
DS21x52 Register Address: *19 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	TJC	T1TCR1	05.7
6	LLB	LBCR	4A.3
5	LIAIS	LIC2	79.4*
4	TCM4	TDS0SEL	74.4
3	TCM3	TDS0SEL	74.3
2	TCM2	TDS0SEL	74.2
1	TCM1	TDS0SEL	74.1
0	TCM0	TDS0SEL	74.0

- LIAIS, bit 5, has been renamed as TUA1. No additional functionality has been associated with this bit

DS21x52 Register: *CCR6: Common Control Register 6*
DS21x52 Register Address: *1E Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	RJC	T1RCR2	04.1
6	RESA	ESCR	4F.3*
5	TESA	ESCR	4F.7*
4	RCM4	RDS0SEL	76.4
3	RCM3	RDS0SEL	76.3
2	RCM2	RDS0SEL	76.2
1	RCM1	RDS0SEL	76.1
0	RCM0	RDS0SEL	76.0

- TESA, bit 5, has been renamed as TESALGN. There is no new functionality associated with the bit.
- RESA, bit 6, has been renamed as RESALGN. There is no new functionality associated with the bit.

DS21x52 Register: *CCR7: Common Control Register 7*
DS21x52 Register Address: *0A Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	LIRST	LIC2	79.6

6	RLB	LBCR	4A.2
5	RESR	ESCR	4F.2
4	TESR	ESCR	4F.6
3	-	-	-
2	LIUSI	LIC3	7A.2*
1	CDIG	LIC3	7A.0*
0	LIUODO	LIC2	79.0*

- LIUODO, bit 0, has been renamed as CLDS. In the DS21x52, this bit determined whether the TTIP and TRING outputs would be open drain or not. In the DS2155, setting this bit to a one will redefine the operation of the transmit line driver. When this bit is set to a one and LIC1.5 = LIC1.6 = LIC1.7 = 0, then the device will generate a square wave at the TTIP and TRING outputs instead of a normal waveform. When this bit is set to a one and LIC1.5 = LIC1.6 = 0 and LIC1.7 = 1, then the device will force TTIP and TRING outputs to become open drain drivers instead of their normal push-pull operation. This bit should be set to zero for normal operation of the DS2155.
- CDIG, bit 1, has been renamed as TAOZ. There is no new functionality associated with the bit.
- LIUSI, bit 2, has been renamed as RSCLKE. There is no new functionality associated with the bit. However, there is now a TSCLKE control bit available in the DS2155, which controls G.703 support for the transmitter.

Status and Information Registers

DS21x52 Register: *RIR1: Receive Information Register 1*
DS21x52 Register Address: *22 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	COFA	INFO1	10.5
6	8ZD	INFO1	10.4
5	16ZD	INFO1	10.3
4	RESF	SR5	1E.2
3	RESE	SR5	1E.1*
2	SEFE	INFO1	10.2
1	B8ZS	INFO1	10.1
0	FBE	INFO1	10.0

- RESE, bit 3, has been renamed as RESEM. There is no new functionality associated with this bit.

DS21x52 Register: *RIR2: Receive Information Register 2*
DS21x52 Register Address: *31 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	RLOSC	SR2	18.4
6	LRCLC	SR2	18.5*
5	TESF	SR5	1E.5
4	TESE	SR5	1E.4*
3	TSLIP	SR5	1E.3

2	RBLC	SR2	18.6*
1	RPDV	INFO1	10.7
0	TPDV	INFO1	10.6

- RBLC, bit 2, has been renamed as RUA1C. There is no new functionality associated with this bit.
- TESE, bit 4, has been renamed as TESEM. There is no new functionality associated with this bit.
- LRCLC, bit 6, has been replaced by RCLC in the DS2155. The functionality of the bit is the same. The difference is where the clear criteria is monitored. In the DS21x52, the bit was monitoring RTIP/RRING for the clear criteria. In the DS2155, the RCLC bit is cleared based on data into the framer, not the line interface.

DS21x52 Register: *RIR3: Receive Information Register 3*
DS21x52 Register Address: *10 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	RL1	INFO2	*See Below*
6	RL0	INFO2	*See Below*
5	JALT	SR1	16.4
4	LORC	SR3	1A.3
3	FRCL	SR2	18.1*
2	-	-	-
1	-	-	-
0	-	-	-

- FRCL, bit 3, has been renamed as RCL. There is no new functionality associated with this bit.
- RL0, bit 6, and RL1, bit 7, have been replaced by additional monitoring capabilities. The DS2155 will report the signal strength at RTIP and RRING in 2.5dB increments via RL3-RL0 located in Information Register 2 (INFO2, address = 11 Hex). This feature is helpful when trouble shooting line performance problems.

DS21x52 Register: *SR1: Status Register 1*
DS21x52 Register Address: *20 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	LUP	SR3	1A.5
6	LDN	SR3	1A.6
5	LOTC	SR3	1A.4
4	RSLIP	SR5	1E.0
3	RBL	SR2	18.2*
2	RYEL	SR2	18.3
1	LRCL	SR1	16.3
0	RLOS	SR2	18.0

- RBL, bit 3, has been renamed as RUA1. There is no new functionality associated with this bit.

DS21x52 Register: *SR2: Status Register 2*

DS21x52 Register Address: *21 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	RMF	SR4	1C.2
6	TMF	SR4	1C.4
5	SEC	SR1	16.6*
4	RFDL	SR8	24.3*
3	TFDL	SR8	24.2*
2	RMTCH	SR8	24.1
1	RAF	SR8	24.4*
0	RSC	SR1	16.5*

- RSC, bit 0, has been renamed as RSCOS. In the DS21x52, this bit was set when the DS21x52 detected a change of state in ANY of the robbed-bit signaling bits. The DS2155 allows the user to select the channels that will be monitored. Via the Receive Signaling Change Of State Interrupt Enable Registers (RSCSE through RSCSE4), the user can select the channels in which a change of state in the robbed-bit signaling bits will set this status bit.
- RAF, bit 1, has been renamed as RFDLAD. There is no new functionality associated with this bit.
- TFDL, bit 3, has been renamed as TFDLE. There is no new functionality associated with this bit.
- RFDL, bit 4, has been renamed as RFDLF. There is no new functionality associated with this bit.
- SEC, bit 5, has been renamed as TIMER. In the DS21x52, this bit was set on increments of one second (referenced to RCLK). In the DS2155, this bit follows the error counter update interval as determined by the ECUS bit in the Error Counter Configuration Register (ERCNT). In T1 mode, this bit can be configured to set on increments of 1 second or 42ms (referenced to RCLK).

DS21x52 Register: *IMR1: Interrupt Mask Register 1*
DS21x52 Register Address: *7F Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	LUP	IMR3	1B.5
6	LDN	IMR3	1B.6
5	LOTC	IMR3	1B.4
4	SLIP	IMR5	1F.0*
3	RBL	IMR2	19.2*
2	RYEL	IMR2	19.3
1	LRCL	IMR1	17.3
0	RLOS	IMR2	19.0

- RBL, bit 3, has been renamed as RUA1. There is no new functionality associated with this bit.
- SLIP, bit 2, has been renamed as RSLIP. There is no new functionality associated with this bit.

DS21x52 Register: *IMR2: Interrupt Mask Register 2*
DS21x52 Register Address: *6F Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	RMF	IMR4	1D.2

6	TMF	IMR4	1D.4
5	SEC	IMR1	17.6*
4	RFDL	IMR8	25.3*
3	TFDL	IMR8	25.2*
2	RMTCH	IMR8	25.1
1	RAF	IMR8	25.4*
0	RSC	IMR1	17.5*

- RSC, bit 0, has been renamed as RSCOS. In the DS21x52, this bit would enable the device to generate an interrupt when the DS21x52 detected a change of state in ANY of the robbed-bit signaling bits. The DS2155 allows the user to select the channels that will be monitored. Via the Receive Signaling Change Of State Interrupt Enable Registers (RSCSE through RSCSE4), the user can select the channels in which a change of state in the robbed-bit signaling bits will generate an interrupt provided the RSCOS bit is set by the user.
- RAF, bit 1, has been renamed as RFDLAD. There is no new functionality associated with this bit.
- TFDL, bit 3, has been renamed as TFDLE. There is no new functionality associated with this bit.
- RFDL, bit 4, has been renamed as RFDLF. There is no new functionality associated with this bit.
- SEC, bit 5, has been renamed as TIMER. In the DS21x52, this bit enabled the interrupt on increments of one second (referenced to RCLK). In the DS2155, this bit follows the error counter update interval as determined by the ECUS bit in the Error Counter Configuration Register (ERCNT). In T1 mode, this bit can be configured to interrupt on increments of 1 second or 42ms (referenced to RCLK).

Error Count Registers

The error count registers have been kept intact, but have been relocated. In addition, the Path Code Violation Count Register 1 and the Multiframes Out Of Sync Count Register 1 no longer share a common address and therefore are both 16-bit counters. See section 15 in the DS2155 data sheet for additional information on the error count registers.

DS21x52 Registers: *LCVCR1, LCVCR2: Line Code Violation Count Register 1 & 2*
DS21x52 Register Address: *23 Hex, 24 Hex*

DS21x52 Registers: *PCVCR1, PCVCR2: Path Code Violation Count Register 1 & 2*
DS21x52 Register Address: *25 Hex (Same as MOSCR1), 26 Hex*

DS21x52 Register: *MOSCR1, MOSCR2: Multiframes Out Of Sync Count Register 1 & 2*
DS21x52 Register Address: *25 Hex (Same as PCVCR1), 27 Hex*

DS21x52 Register	DS21x52 Register Abbreviation	DS2155 Register Abbreviation	DS2155 Address (Hex)
Line Code Violation Count Register 1	LCVCR1 (23 Hex)	LCVCR1	42
Line Code Violation Count Register 2	LCVCR2 (24 Hex)	LCVCR2	43
Path Code Violation Count Register 1	PCVCR1 (25 Hex)*	PCVCR1	44
Path Code Violation Count Register 1	PCVCR2 (26 Hex)	PCVCR2	45
Multiframes Out Of Sync Count Register 1	MOSCR1 (25 Hex)*	FOSCR1	46
Multiframes Out Of Sync Count Register 2	MOSCR2 (27 Hex)	FOSCR2	47

- In the DS21x52, PCVCR1 and MOSCR1 shared the count register located at address 25 Hex. The two error counters no longer share a register in the DS2155.

DS0 Monitoring Function Registers

Both the Transmit DS0 Monitor Register and Receive DS0 Monitor Register has been relocated to a new address.

DS21x52 Register: *TDS0M: Transmit DS0 Monitor Register*
DS21x52 Register Address: *1A Hex*

DS21x52 Register: *RDS0M: Receive DS0 Monitor Register*
DS21x52 Register Address: *1F Hex*

DS21x52 Register	DS21x52 Register Abbreviation	DS2155 Register Abbreviation	DS2155 Address (Hex)
Transmit DS0 Monitor Register	TDS0M (1A Hex)	TDS0M	75
Receive DS0 Monitor Register	RDS0M (1F Hex)	RDS0M	77

Signaling Registers

Receive Signaling Registers 1 through 12 can be found at the same address. However, the signaling information contained in the signaling registers has been rearranged. See section 17 of the DS2155 data sheet for additional information on signaling operation.

DS21x52 Register: *RS1 to RS12: Receive Signaling Registers*
DS21x52 Register Address: *60 to 6B Hex*

- Receive Signaling Registers 1 through 12 can be found at the same address.
- In the ESF framing mode, there can be up to four signaling bits per channel (A, B, C, and D). In the D4 framing mode, there are only two signaling bits per channel (A and B). In the D4 framing mode, the framer will replace the C and D signaling bit positions with the A and B signaling bits from the previous multiframe. Hence, whether the framer is operated in either framing mode, the user needs only to retrieve the signaling bits every 3 ms. The Receive Signaling Registers are frozen and not updated during a loss of sync condition (SR2.0 = 1). They will contain the most recent signaling information before the "OOF" occurred.
- The following table shows the new the arrangement for the Receive Signaling Registers. In T1 mode, RS13-RS16 are not used.

Transmit Signaling Registers (T1 Mode, ESF Format)

Register Name	DS2155 Address								
		(MSB)							(LSB)
TS1	50	CH2-A	CH2-B	CH2-C	CH2-D	CH1-A	CH1-B	CH1-C	CH1-D
TS2	51	CH4-A	CH4-B	CH4-C	CH4-D	CH3-A	CH3-B	CH3-C	CH3-D
TS3	52	CH6-A	CH6-B	CH6-C	CH6-D	CH5-A	CH5-B	CH5-C	CH5-D
TS4	53	CH8-A	CH8-B	CH8-C	CH8-D	CH7-A	CH7-B	CH7-C	CH7-D
TS5	54	CH10-A	CH10-B	CH10-C	CH10-D	CH9-A	CH9-B	CH9-C	CH9-D
TS6	55	CH12-A	CH12-B	CH12-C	CH12-D	CH11-A	CH11-B	CH11-C	CH11-D
TS7	56	CH14-A	CH14-B	CH14-C	CH14-D	CH13-A	CH13-B	CH13-C	CH13-D

TS8	57	CH16-A	CH16-B	CH16-C	CH16-D	CH15-A	CH15-B	CH15-C	CH15-D
TS9	58	CH18-A	CH18-B	CH18-C	CH18-D	CH17-A	CH17-B	CH17-C	CH17-D
TS10	59	CH20-A	CH20-B	CH20-C	CH20-D	CH19-A	CH19-B	CH19-C	CH19-D
TS11	5A	CH22-A	CH22-B	CH22-C	CH22-D	CH21-A	CH21-B	CH21-C	CH21-D
TS12	5B	CH24-A	CH24-B	CH24-C	CH24-D	CH23-A	CH23-B	CH23-C	CH23-D

Transmit Signaling Registers (T1 Mode, D4 Format)

Register Name	DS2155 Address								
		(MSB)							(LSB)
TS1	50	CH2-A	CH2-B	**CH2-A**	**CH2-B**	CH1-A	CH1-B	**CH1-A**	**CH1-B**
TS2	51	CH4-A	CH4-B	**CH4-A**	**CH4-B**	CH3-A	CH3-B	**CH3-A**	**CH3-B**
TS3	52	CH6-A	CH6-B	**CH6-A**	**CH6-B**	CH5-A	CH5-B	**CH5-A**	**CH5-B**
TS4	53	CH8-A	CH8-B	**CH8-A**	**CH8-B**	CH7-A	CH7-B	**CH7-A**	**CH7-B**
TS5	54	CH10-A	CH10-B	**CH10-A**	**CH10-B**	CH9-A	CH9-B	**CH9-A**	**CH9-B**
TS6	55	CH12-A	CH12-B	**CH12-A**	**CH12-B**	CH11-A	CH11-B	**CH11-A**	**CH11-B**
TS7	56	CH14-A	CH14-B	**CH14-A**	**CH14-B**	CH13-A	CH13-B	**CH13-A**	**CH13-B**
TS8	57	CH16-A	CH16-B	**CH16-A**	**CH16-B**	CH15-A	CH15-B	**CH15-A**	**CH15-B**
TS9	58	CH18-A	CH18-B	**CH18-A**	**CH18-B**	CH17-A	CH17-B	**CH17-A**	**CH17-B**
TS10	59	CH20-A	CH20-B	**CH20-A**	**CH20-B**	CH19-A	CH19-B	**CH19-A**	**CH19-B**
TS11	5A	CH22-A	CH22-B	**CH22-A**	**CH22-B**	CH21-A	CH21-B	**CH21-A**	**CH21-B**
TS12	5B	CH24-A	CH24-B	**CH24-A**	**CH24-B**	CH23-A	CH23-B	**CH23-A**	**CH23-B**

Note: In D4 format, TS1-TS12 contains signaling data for two frames. Bold type indicates data for second frame.

Per-Channel Code (Idle) Generation Registers

The method for generating idle codes has changed in the DS2155. The DS2155 contains a 64-byte Idle Code Array accessed by the Idle Array Address Register (IAAR) and the Per-Channel Idle Code Register (PCICR). The contents of the array contain the idle codes to be substituted into the appropriate transmit or receive channels. This substitution can be enabled and disabled on a per-channel basis by the Transmit Channel Idle Code Enable registers (TCICE1-4) and Receive Channel Idle Code Enable registers (RCICE1-4). The following table gives the DS2155 register that closely resembles the corresponding DS21x52 register. See section 18 of the DS2155 for additional information on per-channel idle code generation.

DS21x52 Register: *TIR1, TIR2, TIR3: Transmit Idle Registers 1, 2, 3*
DS21x52 Register Address: *3C, 3D, 3E Hex*

DS21x52 Register: *TIDR: Transmit Idle Definition Register*
DS21x52 Register Address: *3F Hex*

DS21x52 Register: *TCC1, TCC2, TCC3: Transmit Channel Control Registers*
DS21x52 Register Address: *16, 17, 18 Hex*

DS21x52 Register: *RMR1, RMR2, RMR3: Receive Mark Registers*
DS21x52 Register Address: *2D, 2E, 2F Hex*

DS21x52 Register: *TC1 to TC24: Transmit Channel Registers*
DS21x52 Register Address: *50 to 57 Hex & 40 to 4F Hex*

DS21x52 Register: *RC1 to RC24: Receive Channel Registers*
DS21x52 Register Address: *80 to 8F Hex & 58 to 5F Hex*

DS21x52 Register: *RCC1, RCC2, RCC3: Receive Channel Control Registers*
DS21x52 Register Address: *1B, 1C, 1D Hex*

DS21x52 Register	DS21x52 Register Abbreviation	DS2155 Register Abbreviation	DS2155 Address (Hex)
Transmit Idle Register 1	TIR1 (3C Hex)	TCICE1	80
Transmit Idle Register 2	TIR2 (3D Hex)	TCICE2	81
Transmit Idle Register 3	TIR3 (3E Hex)	TCICE3	82
Transmit Idle Definition Register	TIDR (3F Hex)	PCICR	7F
Transmit Channel Control Register 1	TCC1 (16 Hex)	PCDR1	29
Transmit Channel Control Register 2	TCC2 (17 Hex)	PCDR2	2A
Transmit Channel Control Register 3	TCC3 (18 Hex)	PCDR3	2B
Receive Mark Register 1	RMR1 (2D Hex)	RCICE1	84
Receive Mark Register 2	RMR1 (2E Hex)	RCICE2	85
Receive Mark Register 3	RMR1 (2F Hex)	RCICE3	86
Transmit Channel Registers 1 to 24	TC1 to TC24	*	*
Receive Channel Registers 1 to 24	RC1 to RC24	*	*
Receive Channel Control Registers 1-3	RCC1 to RCC3	*	*

TC1 to TC24, RC1 to RC24, and RCC1 to RCC3 have been incorporated in the new functionality of the per-channel idle code generation. See section 18 of the DS2155 data sheet for more detail.

Channel Blocking Registers

DS21x52 Register: *RCBR1, RCBR2, RCBR3: Receive Channel Block Registers*
DS21x52 Register Address: *6C, 6D, 6E Hex*

DS21x52 Register: *TCBR1, TCBR2, TCBR3: Transmit Channel Block Registers*
DS21x52 Register Address: *32, 33, 34 Hex*

DS21x52 Register	DS21x52 Register Abbreviation	DS2155 Register Abbreviation	DS2155 Address (Hex)
Receive Channel Block Register 1	RCBR1 (6C Hex)	RCBR1	88
Receive Channel Block Register 2	RCBR2 (6D Hex)	RCBR2	89
Receive Channel Block Register 3	RCBR3 (6E Hex)	RCBR3	8A
Transmit Channel Block Register 1	TCBR1 (32 Hex)	TCBR1	8C
Transmit Channel Block Register 2	TCBR2 (33 Hex)	TCBR2	8D
Transmit Channel Block Register 3	TCBR3 (34 Hex)	TCBR3	8E

HDLC Registers

While the DS21x52 has only one HDLC controller, the DS2155 has two enhanced HDLCs. Each controller is configurable for use with time slots, or Sa4 to Sa8 bits (E1 Mode) or the FDL (T1 Mode). The transmit and receive path buffers in the DS2155 have been doubled to 128-bytes. When used with time slots, the user can select any time slot or multiple time slots, contiguous or non-contiguous, as well as any specific bits within the time slot(s) to assign to the HDLC controllers.

The HDLC controller performs the necessary overhead for generating and receiving Performance Report Messages (PRM) as described in ANSI T1.403 and the messages as described in AT&T TR54016. The HDLC controller automatically generates and detects flags, generates and checks the CRC check sum, generates and detects abort sequences, stuffs and de-stuffs zeros, and byte aligns to the data stream. The 128-byte buffers in the HDLC controller are large enough to allow a full PRM to be received or transmitted without host intervention.

The user must take care to not map both transmit HDLC controllers to the same Sa bits, time slots or, in T1 mode, map both controllers to the FDL. HDLC #1 and HDLC #2 are identical in operation and therefore, when applicable, each DS21x52 register bit will be mapped to two addresses.

DS21x52 Register: HCR: *HDLC Control Register*
DS21x52 Register Address: *00 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	RBR	BOCC	37.3
6	RHR	HxRC*	31.7 32.7
5	TFS	HxTC*	90.3 A0.3
4	THR	HxTC*	90.5 A0.5
3	TABT	HxTC*	*See below*
2	TEOM	HxTC*	90.2 A0.2
1	TZSD	HxTC*	90.1 A0.1
0	TCRCD	HxTC*	90.0 A0.0

- HxTC refers to H1TC and H2TC located at addresses 90 Hex and A0 Hex respectively.
- HxRC refers to H1RC and H2RC located at addresses 31 Hex and 32 Hex respectively.
- TABT, bit 3, has been incorporated into the Transmit HDLC Reset (THR) bit.

DS21x52 Register: *HSR: HDLC Status Register*
DS21x52 Register Address: *01 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	RBOC	SR8	24.0
6	RPE	SR6 SR7	20.5 22.5

5	RPS	SR6 SR7	20.4 22.4
4	RHALF	SR6 SR7	20.3* 22.3*
3	RNE	SR6 SR7	20.2 22.2
2	THALF	SR6 SR7	20.1* 22.1*
1	TNF	SR6 SR7	20.0 22.0
0	TMEND	SR6 SR7	20.6 22.6

- The status bits for HDLC #1 have been mapped to Status Register 6 (SR6) in the DS2155.
- The status bits for HDLC #2 have been mapped to Status Register 7 (SR7) in the DS2155.
- THALF, bit 2, has been renamed to TLWM. In the DS21x52, THALF is set when the transmit 64-byte FIFO empties beyond the halfway point. For the DS2155, the TLWM bit will be set when the transmit 128-byte FIFO empties beyond the low water mark as defined by the TFLWM0-TFLWM2 bits located in the FIFO control register (H1FC, H2FC). The low water mark is programmable to one of 8 different levels.
- RHALF, bit 4, has been renamed to RHWM. In the DS21x52, RHALF is set when the receive 64-byte FIFO fills beyond the halfway point. For the DS2155, the RHWM bit will be set when the receive 128-byte FIFO fills beyond the high water mark as defined by the RFHWM0-RFHWM2 bits located in the FIFO control register (H1FC, H2FC). The high water mark is programmable to one of 8 different levels.

DS21x52 Register: *HIMR: HDLC Interrupt Mask Register*
DS21x52 Register Address: *02 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	RBOC	IMR8	25.0
6	RPE	IMR6 IMR7	21.5 23.5
5	RPS	IMR6 IMR7	21.4 23.4
4	RHALF	IMR6 IMR7	21.3* 23.3*
3	RNE	IMR6 IMR7	21.2 23.2
2	THALF	IMR6 IMR7	21.1* 23.1*
1	TNF	IMR6 IMR7	21.0 23.0
0	TMEND	IMR6 IMR7	21.6 23.6

- The interrupt mask bits for HDLC #1 have been mapped to HDLC Interrupt Mask Register 6 (IMR6)

in the DS2155.

- The interrupt mask bits for HDLC #2 have been mapped to HDLC Interrupt Mask Register 7 (IMR7) in the DS2155.
- THALF, bit 2, has been renamed to TLWM. When THALF is enabled in the DS21x52, the device will generate an interrupt when the transmit 64-byte FIFO empties beyond the halfway point. For the DS2155, the device will generate an interrupt, if TLWM is enabled, when the transmit 128-byte FIFO empties beyond the low water mark as defined by the TFLWM0-TFLWM2 bits located in the FIFO control register (H1FC, H2FC). The low water mark is programmable to one of 8 different levels.
- RHALF, bit 4, has been renamed to RLWM. When RHALF is enabled in the DS21x52, the device will generate an interrupt when the receive 64-byte FIFO fills beyond the halfway point. For the DS2155, the device will generate an interrupt, if RHWM is enabled, when the receive 128-byte FIFO fills beyond the high water mark as defined by the RFHWM0-RFHWM2 bits located in the FIFO control register (H1FC, H2FC). The high water mark is programmable to one of 8 different levels.

DS21x52 Register: *RHIR: Receive HDLC Information Register*
DS21x52 Register Address: *03 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	RABT	INFO5 INFO6	*See below*
6	RCRCE	INFO5 INFO6	*See below*
5	ROVR	INFO5 INFO6	*See below*
4	RVM	INFO5 INFO6	*See below*
3	REMPTY	INFO5 INFO6	2E.3 2F.3
2	POK	INFO5 INFO6	*See below*
1	CBYTE	HxRPBA*	9C.7* AC.7*
0	OBYTE	INFO4*	#1 2D.1* #2 2D.3*

- The HDLC information bits for HDLC #1 have been mapped to the Receive HDLC #1 Information Register, INFO5.
- The HDLC information bits for HDLC #2 have been mapped to the Receive HDLC #2 Information Register, INFO6.
- OBYTE, bit 0, is renamed as H1OBT for HDLC #1 and H2OBT for HDLC #2. Both H1OBT & H2OBT can be found in the HDLC Event Information Register (INFO4, address 2D Hex). There is no new functionality associated with this bit.
- HxRPBA refers to H1RPBA and H2RPBA, located at addresses 9C Hex and AC Hex respectively.
- CBYTE, bit 1, has been renamed as MS. Unlike the operation of the CBYTE bit in the DS21x52, the MS bit will be low when the byte available for reading the receive FIFO is the last byte of a message. MS will be high when the byte available for reading is the first byte of the continuation of a message.

- POK, bit 2, has been incorporated into the Receive Packet Status bits (PS0-PS2) located in INFO5 and INFO6.
- RVM, bit 4, has been incorporated into the Receive Packet Status bits (PS0-PS2) located in INFO5 and INFO6.
- ROVR, bit 5, has been incorporated into the Receive Packet Status bits (PS0-PS2) located in INFO5 and INFO6.
- RCRCE, bit 6, has been incorporated into the Receive Packet Status bits (PS0-PS2) located in INFO5 and INFO6.
- RABT, bit 7, has been incorporated into the Receive Packet Status bits (PS0-PS2) located in INFO5 and INFO6.

DS21x52 Register: *RBOC: Receive Bit Oriented Code Register*
DS21x52 Register Address: *04 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	LBD	SR2	18.7
6	BD	INFO2	11.6
5	BOC5	*See below*	*See below*
4	BOC4	*See below*	*See below*
3	BOC3	*See below*	*See below*
2	BOC2	*See below*	*See below*
1	BOC1	*See below*	*See below*
0	BOC0	*See below*	*See below*

- BOC0-BOC5, bits 0-5, share the RFDL register in the DS2155. See section 22 of the DS2155 for additional information on the BOC controller.

DS21x52 Register: *RHFR: Receive HDLC FIFO*
DS21x52 Register Address: *05 Hex*

- The Receive HDLC FIFO Register has been relocated to address 9E Hex for HDLC #1 and AE Hex for HDLC #2.
- The lower 7 bits of the Receive Packet Bytes Available registers (H1RPBA, H2RPBA) indicate the number of bytes that can be read from the receive FIFO. The value indicated by the lower seven bits in these registers informs the host as to how many bytes can be read from the receive FIFO without going past the end of a message. This value will refer to one of four possibilities, the first part of a packet, the continuation of a packet, the last part of a packet, or a complete packet. After reading the number of bytes indicated by this register the host then checks the HDLC Information register for detailed message status. See section 24.4.2 of the DS2155 data sheet for additional information.

DS21x52 Register: *THIR: Transmit HDLC Information Register*
DS21x52 Register Address: *06 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	-	-	-
6	-	-	-
5	-	-	-

4	-	-	-
3	-	-	-
2	TEMPTY	INFO5 INFO6	2E.5 2F.5
1	TFULL	INFO5 INFO6	2E.4 2F.4
0	TUDR	INFO4*	#1 2D.1* #2 2D.3*

- TUDR, bit 0, is renamed as H1UDR for HDLC #1 and H2UDR for HDLC #2. Both H1UDR & H2UDR can be found in the HDLC Event Information Register (INFO4, address 2D Hex). There is no new functionality associated with this bit.

DS21x52 Register: *TBOC: Transmit Bit Oriented Code Register*
DS21x52 Register Address: *07 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	SBOC	BOCC	37.0
6	HBEN	HxTC*	90.4* A0.4*
5	BOC5	*See below*	*See below*
4	BOC4	*See below*	*See below*
3	BOC3	*See below*	*See below*
2	BOC2	*See below*	*See below*
1	BOC1	*See below*	*See below*
0	BOC0	*See below*	*See below*

- BOC0-BOC5, bits 0-5, share the TFDL register in the DS2155. See section 22 of the DS2155 for additional information on the BOC controller.
- HxTC refers to H1TC and H2TC located at addresses 90 Hex and A0 Hex respectively.
- HBEN, bit 6, has been renamed as THMS. The THMS bit behaves in a different manner than the HBEN bit. See section 22 and 24 of the DS2155 for more information about the HDLCs operation.

DS21x52 Register: *THFR: Transmit HDLC FIFO*
DS21x52 Register Address: *08 Hex*

- The Transmit HDLC FIFO Register has been relocated to address 9D Hex for HDLC #1 and AD Hex for HDLC #2.
- The Transmit FIFO Buffer Available registers (H1TFBA, H2TFBA) indicate the number of bytes that can be written into the transmit FIFOs. The count from this register informs the host as to how many bytes can be written into the transmit FIFO without overflowing the buffer

DS21x52 Register: *RDC1: Receive HDLC DS0 Control Register 1*
DS21x52 Register Address: *90 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	RDS0E	HxRC	31.6*

			32.6*
6	-	-	-
5	RDS0M	*See below*	*See below*
4	RD4	*See below*	*See below*
3	RD3	*See below*	*See below*
2	RD2	*See below*	*See below*
1	RD1	*See below*	*See below*
0	RD0	*See below*	*See below*

- RD0 through RD4, bits 0 to 4, and RDS0M, bit 5, have been replaced by registers H1RCS1 to H1RCS4 for HDLC #1 and H2RCS1 to H2RCS4 for HDLC #2. Any channel or combination of channels, contiguous or not, can be assigned to an HDLC controller. When assigned to a channel(s) any combination of bits within the channel(s) can be avoided. See section 24.3 of the DS2155 for additional information on mapping the HDLC data to channels.
- HxRC refers to H1RC and H2RC located at addresses 31 Hex and 32 Hex respectively.
- RDS0E, bit 7, has been renamed to RHMS. The operation of this bit is inverted from that of the DS21x52. See section 24 of the DS2155 for additional information.

DS21x52 Register: *RDC2: Receive HDLC DS0 Control Register 2*
DS21x52 Register Address: *91 Hex*

- Receive HDLC DS0 Control Register 2 has been relocated to 96 Hex for HDLC #1 and A6 Hex for HDLC #2.

DS21x52 Register: *TDC1: Transmit HDLC DS0 Control Register 1*
DS21x52 Register Address: *92 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	TDS0E	HxTC	90.4* A0.4*
6	-	-	-
5	TDS0M	*See below*	*See below*
4	TD4	*See below*	*See below*
3	TD3	*See below*	*See below*
2	TD2	*See below*	*See below*
1	TD1	*See below*	*See below*
1	TD1	*See below*	*See below*

- TD0 through TD4, bits 0 to 4, and TDS0M, bit 5, have been replaced by registers H1TCS1 to H1TCS4 for HDLC #1 and H2TCS1 to H2TCS4 for HDLC #2. Any channel or combination of channels, contiguous or not, can be assigned to an HDLC controller. When assigned to a channel(s) any combination of bits within the channel(s) can be avoided. See section 24.3 of the DS2155 for additional information on mapping the HDLC data to channels.
- HxTC refers to H1TC and H2TC located at addresses 90 Hex and A0 Hex respectively.
- TDS0E, bit 7, has been renamed to THMS. The operation of this bit is inverted from that of the DS21x52. See section 24 of the DS2155 for additional information.

DS21x52 Register: *TDC2: Transmit HDLC DS0 Control Register 2*
DS21x52 Register Address: *93 Hex*

- Transmit HDLC DS0 Control Register 2 has been relocated to 9B Hex for HDLC #1 and AB Hex for HDLC #2.

DS21x52 Register: *RFDL: Receive FDL Register*
DS21x52 Register Address: *28 Hex*

- The Receive FDL Register has been relocated to address C0 Hex.
- The RFDL register will operate as the receive BOC message and information register when the receive BOC function is enabled by setting BOCC.4 to 1. The lower six bits of the RFDL register will contain the BOC message bits when used in this configuration. See section 22 of the DS2155 data sheet for more information.

DS21x52 Register: *RFDLM1, RFDLM2: Receive FDL Match Registers*
DS21x52 Register Address: *29 & 2A Hex*

- Receive FDL Match Registers 1 and 2 have been relocated to address C2 Hex and C3 Hex, respectively.

DS21x52 Register: *TFDL: Transmit FDL Register*
DS21x52 Register Address: *7E Hex*

- The Transmit FDL Register has been relocated to address C1 Hex.
- The TFDL register will operate as the transmit BOC message register when the transmit BOC function is enabled by setting BOCC.0 to 1. The lower six bits of the TFDL register will contain the BOC message to be transmitted. See section 22 of the DS2155 data sheet for additional information.

Line Interface, Programmable In-Band Loop Code, and Transmit Transparency Registers

DS21x52 Register: *LICR: Line Interface Control Register*
DS21x52 Register Address: *7C Hex*

DS21x52 Register: *IBCC: In-Band Code Control Register*
DS21x52 Register Address: *12 Hex*

DS21x52 Register: *TCD: Transmit Code Definition Register*
DS21x52 Register Address: *13 Hex*

DS21x52 Register: *RUPCD: Receive Up Code Definition Register*
DS21x52 Register Address: *14 Hex*

DS21x52 Register: *RDNCD: Receive Down Code Definition Register*
DS21x52 Register Address: *15 Hex*

DS21x52 Register: *TTR1, TTR2, TTR3: Transmit Transparency Registers*
DS21x52 Register Address: *39, 3A, 3B Hex*

DS21x52 Register	DS21x52 Register Abbreviation	DS2155 Register Abbreviation	DS2155 Address (Hex)

Line Interface Control Register	LICR (7C Hex)	LIC1	78
In-Band Code Control Register	IBCC (12 Hex)	IBCC	B6
Transmit Code Definition Register	TCD (13 Hex)	TCD1*	B7*
Receive Up Code Definition Register	RUPCD (14 Hex)	RUPCD1*	B9*
Receive Down Code Definition Register	RDNCD (15 Hex)	RDNCD1*	BB*
Transmit Transparency Register 1	TTR1	SSIE1	08
Transmit Transparency Register 2	TTR2	SSIE2	09
Transmit Transparency Register 3	TTR3	SSIE3	0A

- The DS2155's programmable in-band loop code generation and detection includes support for 16-bit codes. In adding this feature a second register has been added for transmit code definition and receive up/down code definition. For generation or detection of 8 bit patterns, both of the appropriate definition registers must be filled with the same value. See section 26 of the DS2155 data sheet for additional information.

Interleaved PCM Bus Operation Register

The interleave bus operation has been converted to full software control in the DS2155 and the external pins associated with this option have been reassigned to the extended system information bus function. See section 29 for more detail on the interleaved PCM bus operation.

DS21x54 Register: *IBO: Interleaved Bus Operation Register*
DS21x54 Register Address: *94 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	-	-	-
6	-	-	-
5	-	-	-
4	-	-	-
3	IBOEN	IBOC	C5.3
2	INTSEL	IBOC	C5.3*
1	MSEL0	*See below*	*See below*
0	MSEL1	See below	See below

- MSEL0 and MSEL1 are not included in the DS2155.
- INTSEL, bit 2, has been renamed IBOSEL. There is no new functionality associated with this control bit.

3. Software Considerations: DS2155 vs. DS21x54 (E1)

This section will present the registers for the DS21354 and DS21554. The registers are presented in the order that they appear in the DS21354 and DS21554 data sheet.

ID Register

DS21x54 Register: *IDR: Device Identification Register*
DS21x54 Register Address: *0F Hex*

The Device Identification Register (IDR) for the DS2155 is located at the same address as the IDR for the DS21x54. The upper four bits display the DS2155 ID (1011) and the lower four bits display the die revision.

Receive Control Registers

DS21x54 Register: *RCR1: Receive Control Register 1*
DS21x54 Register Address: *10 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	RSMF	IOCR1	01.6*
6	RSM	IOCR1	01.5*
5	RSIO	IOCR1	01.4
4	-	-	-
3	-	-	-
2	FRC	E1RCR1	33.2
1	SYNCE	E1RCR1	33.1
0	RESYNC	E1RCR1	33.0

- RSM, bit 6, has been renamed as RSMS1. There is no new functionality associated with the bit.
- RSDW, bit 7, has been renamed as RSMS2. There is no new functionality associated with the bit.

DS21x54 Register: *RCR2: Receive Control Register 2*
DS21x54 Register Address: *11 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	Sa8S	E1RCR2	34.7
6	Sa7S	E1RCR2	34.6
5	Sa6S	E1RCR2	34.5
4	Sa5S	E1RCR2	34.4
3	Sa4S	E1RCR2	34.3
2	RBCS	IOCR2	02.0*
1	RESE	ESCR	4F.0
0	-	-	-

- RBCS, bit 2, has been renamed as RSCLKM. There is no new functionality associated with the bit.

Transmit Control Registers

DS21x54 Register: *TCR1: Transmit Control Register 1*
DS21x54 Register Address: *12 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	ODF	IOCR1	01.0
6	TFPT	E1TCR1	35.7
5	T16S	E1TCR1	35.6

4	TUA1	E1TCR1	35.5
3	TsiS	E1TCR1	35.4
2	TSA1	E1TCR1	35.3
1	TSM	IOCR1	01.2
0	TSIO	IOCR1	01.1

DS21x54 Register: *TCR2: Transmit Control Register 2*
DS21x54 Register Address: *13 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	Sa8S	E1TCR2	36.7
6	Sa7S	E1TCR2	36.6
5	Sa6S	E1TCR2	36.5
4	Sa5S	E1TCR2	36.4
3	Sa4S	E1TCR2	36.3
2	ODM	CCR1	70.4
1	AEBE	E1TCR2	36.2
0	PF	CCR1	70.0*

- PF, bit 0, has been renamed as RLOSF. There is no new functionality associated with the bit.

Common Control Registers

DS21x54 Register: *CCR1: Common Control Register 1*
DS21x54 Register Address: *14 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	FLB	LBCR	4A.0
6	THDB3	E1TCR1	35.2
5	TG802	E1TCR1	35.1
4	TCRC4	E1TCR1	35.0
3	RSM	E1RCR1	33.6*
2	RHDB3	E1RCR1	33.5
1	RG802	E1RCR1	33.4
0	RCRC4	E1RCR1	33.3

- RSM, bit 3, has been renamed as RSIGM. There is no new functionality associated with the bit.

DS21x54 Register: *CCR2: Common Control Register 2*
DS21x54 Register Address: *1A Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	ECUS	ERCNT	41.5
6	VCRFS	ERCNT	41.3
5	AAIS	E1TCR2	36.1

4	ARA	E1TCR2	36.0
3	RSERC	E1RCR1	33.7
2	LOTCMC	CCR1	*See below*
1	RFF	SIGCR	40.3
0	RFE	SIGCR	40.4

- LOTCMC, bit 2, has been combined with other functions to simplify the selection of the transmit clock source. The two bits, Transmit Clock Source Select 0 (TCSS0) and Transmit Clock Source Select 1 (TCSS1), are located in the DS2155's Common Control Register 1 (CCR1, address 70 Hex) in bit positions 1 and 2 respectively.

DS21x54 Register: *CCR3: Common Control Register 3*
DS21x54 Register Address: *1B Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	TESE	ESCR	4F.4
6	TCBFS	*See Below*	*See Below*
5	TIRFS	*See Below*	*See Below*
4	-	-	-
3	RSRE	PCPR	28.6*
2	THSE	PCPR	28.3*
1	TBCS	IOCR2	02.1*
0	RCLA	E1RCR2	34.0

- TBCS, bit 1, has been renamed as TSCLKM. There is no new functionality associated with this bit.
- THSE, bit 2, has been renamed as THSCS. See sections 7 and 17 of the DS2155 data sheet for information on per-channel register operation.
- RSRE, bit 3, has been renamed as RSRCS. See sections 7 and 17 of the DS2155 data sheet for additional information on receive signaling re-insertion.
- Control bit 5, TIRFS, has been incorporated in the new functionality for idle code generation. See section 18 of the DS2155 data sheet for more detail.
- Control bit 6, TCBFS, has been incorporated into the per-channel register operation. See sections 7 and 17 of the DS2155 data sheet for additional information.

DS21x54 Register: *CCR4: Common Control Register 4*
DS21x54 Register Address: *A8 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	RLB	LBCR	4A.2
6	LLB	LBCR	4A.3
5	LIAIS	LIC2	79.4*
4	TCM4	TDS0SEL	74.4
3	TCM3	TDS0SEL	74.3
2	TCM2	TDS0SEL	74.2
1	TCM1	TDS0SEL	74.1

0	TCM0	TDS0SEL	74.0

- LIAIS, bit 1, has been renamed as TUA1. There is no new functionality associated with this bit.

DS21x54 Register: *CCR5: Common Control Register 5*
DS21x54 Register Address: *AA Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	LIRST	LIC2	79.6
6	RESA	ESCR	4F.3*
5	TESA	ESCR	4F.7*
4	RCM4	RDS0SEL	76.4
3	RCM3	RDS0SEL	76.3
2	RCM2	RDS0SEL	76.2
1	RCM1	RDS0SEL	76.1
0	RCM0	RDS0SEL	76.0

- TESA, bit 5, has been renamed as TESALGN. There is no new functionality associated with the bit.
- RESA, bit 6, has been renamed as RESALGN. There is no new functionality associated with the bit.

DS21x54 Register: *CCR6: Common Control Register 6*
DS21x54 Register Address: *1D Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	LIUODO	LIC2	79.0*
6	CDIG	LIC3	7A.0*
5	LIUSI	LIC3	7A.2*
4	-	-	-
3	-	-	-
2	TCLKSRC	CCR1	*See below*
1	RESR	ESCR	4F.2
0	TESR	ESCR	4F.6

- TCLKSRC, bit 2, has been combined with other functions to simplify the selection of the source for the transmit clock. Two bits, Transmit Clock Source Select bit 0 (TCSS0) and bit 1 (TCSS1) are located in the DS2155's Common Control Register 1 (CCR1, address 70 Hex) in bit positions 1 and 2 respectively.
- LIUSI, bit 5, has been renamed as RSCLKE. There is no new functionality associated with the bit. However, there is now a TSCLKE control bit available in the DS2155, which controls G.703 support for the transmitter.
- CDIG, bit 6, has been renamed as TAOZ. There is no new functionality associated with the bit.
- LIUODO, bit 7, has been renamed as CLDS. In the DS21x54, this bit determined whether the TTIP and TRING outputs would be open drain or not. In the DS2155, setting this bit to a one will redefine the operation of the transmit line driver. When this bit is set to a one and LIC1.5 = LIC1.6 = LIC1.7 = 0, then the device will generate a square wave at the TTIP and TRING outputs instead of a normal waveform. When this bit is set to a one and LIC1.5 = LIC1.6 = 0 and LIC1.7 = 1, then the device will force TTIP and TRING outputs to become open drain drivers instead of their normal

push-pull operation. This bit should be set to zero for normal operation of the DS2155.

Status and Information Registers

DS21x54 Register: *RIR: Receive Information Register*
DS21x54 Register Address: *08 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	TESF	SR5	1E.5
6	TESE	SR5	1E.4*
5	JALT	SR1	16.4
4	RESF	SR5	1E.2
3	RESE	SR5	1E.1*
2	CRCRC	INFO3	12.2
1	FASRC	INFO3	12.1
0	CASRC	INFO3	12.0

- RESE, bit 3, has been renamed as RESEM. There is no new functionality associated with this bit.
- TESE, bit 6, has been renamed as TESEM. There is no new functionality associated with this bit.

DS21x54 Register: *SSR: Synchronizer Status Register*
DS21x54 Register Address: *1E Hex*

- The Synchronizer Status Register has been relocated to address 30 Hex in the DS2155.

DS21x54 Register: *SR1: Status Register 1*
DS21x54 Register Address: *06 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	RSA1	SR4	1C.6
6	RDMA	SR3	1A.1
5	RSA0	SR4	1C.5
4	RSLIP	SR5	1E.0
3	RUA1	SR2	18.2
2	RRA	SR3	1A.0
1	RCL	SR1	16.3*
0	RLOS	SR2	18.0

- RCL, bit 1, has been renamed as LRCL. No additional functionality is associated with this bit.

DS21x54 Register: *SR2: Status Register 2*
DS21x54 Register Address: *07 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	RMF	SR4	1C.2
6	RAF	SR4	1C.0

5	TMF	SR4	1C.4
4	SEC	SR1	16.6*
3	TAF	SR4	1C.3
2	LOTC	SR3	1A.4
1	RCMF	SR4	1C.1
0	TSLIP	SR5	1E.3

- SEC, bit 5, has been renamed as TIMER. In the DS21x54, this bit was set on increments of one second (referenced to RCLK). In the DS2155, this bit follows the error counter update interval as determined by the ECUS bit in the Error Counter Configuration Register (ERCNT). In T1 mode, this bit can be configured to set on increments of 1 second or 42ms (referenced to RCLK).

DS21x54 Register: *IMR1: Interrupt Mask Register 1*
DS21x54 Register Address: *16 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	RSA1	IMR4	1D.6
6	RDMA	IMR3	1B.1
5	RSA0	IMR4	1D.5
4	RSLIP	IMR5	1F.0
3	RUA1	IMR2	19.2
2	RRA	IMR3	1B.0
1	RCL	IMR1	17.3*
0	RLOS	IMR2	19.0

- RCL, bit 1, has been renamed as LRCL. No additional functionality is associated with this bit.

DS21x54 Register: *IMR2: Interrupt Mask Register 2*
DS21x54 Register Address: *17 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	RMF	IMR4	1D.2
6	RAF	IMR4	1D.0
5	TMF	IMR4	1D.4
4	SEC	IMR1	17.6*
3	TAF	IMR4	1D.3
2	LOTC	IMR3	1B.4
1	RCMF	IMR4	1D.1
0	TSLIP	IMR5	1F.3

- SEC, bit 5, has been renamed as TIMER. In the DS21x54, this bit enabled the interrupt on increments of one second (referenced to RCLK). In the DS2155, this bit follows the error counter update interval as determined by the ECUS bit in the Error Counter Configuration Register (ERCNT). In T1 mode, this bit can be configured to interrupt on increments of 1 second or 42ms (referenced to RCLK).

Error Count Registers

The error count registers have been kept intact, but have been relocated. In addition, all of the count registers are now 16-bit registers because the registers that were shared in the DS21x54 are no longer shared in the DS2155. See section 15 in the DS2155 data sheet for additional information on the error count registers.

DS21x54 Registers: *VCR1, VCR2: Bipolar Violation Count Register 1 & 2*
DS21x54 Register Address: *00, 01 Hex*

DS21x54 Registers: *CRCCR1, CRCCR2: CRC4 Count Register 1 & 2*
DS21x54 Register Address: *02 Hex (Same as FASCR1), 03 Hex*

DS21x54 Register: *FASCR1, FASCR2: FAS Error Count Register 1 & 2*
DS21x54 Register Address: *02 Hex (Same as CRCCR1), 04 Hex (Same as EBCR1)*

DS21x54 Register: *EBCR1, EBCR2: E-Bit Count Register 1 & 2*
DS21x54 Register Address: *04 Hex (Same as FASCR2), 05 Hex*

DS21x54 Register	DS21x54 Register Abbreviation	DS2155 Register Abbreviation	DS2155 Address (Hex)
Bipolar Violation Count Register 1	VCR1 (00 Hex)	LCVCR1	42
Bipolar Violation Count Register 2	VCR2 (01 Hex)	LCVCR2	43
CRC4 Count Register 1	CRCCR1 (02 Hex)*	PCVCR1	44
CRC4 Count Register 2	CRCCR2 (03 Hex)	PCVCR2	45
FAS Error Count Register 1	FASCR1 (02 Hex)*	FOSCR1	46
FAS Error Count Register 2	FASCR2 (04 Hex)*	FOSCR2	47
E-Bit Error Count Register 1	EBCR1 (04 Hex)*	EBCR2	48
E-Bit Error Count Register 2	EBCR2 (05 Hex)	EBCR2	49

- In the DS21x54, CRCCR1 and FASCR1 shared the count register located at address 02 Hex. The two error counters no longer share a register in the DS2155.
- Additionally, FASCR2 and EBCR1 shared the count register located at address 04 Hex. These two error counters no longer share a register in the DS2155.

DS0 Monitoring Function Registers

Both the Transmit DS0 Monitor Register and Receive DS0 Monitor Register has been relocated to a new address.

DS21x54 Register: *TDS0M: Transmit DS0 Monitor Register*
DS21x54 Register Address: *A9 Hex*

DS21x54 Register: *RDS0M: Receive DS0 Monitor Register*
DS21x54 Register Address: *AB Hex*

DS21x54 Register	DS21x54 Register Abbreviation	DS2155 Register Abbreviation	DS2155 Address (Hex)
Transmit DS0 Monitor Register	TDS0M (A9 Hex)	TDS0M	75

Receive DS0 Monitor Register	RDS0M (AB Hex)	RDS0M	77

Signaling Registers

The Transmit Signaling Registers and Receive Signaling Registers have been relocated to 50-5F Hex and 60-6F Hex, respectively. Additionally, the signaling information contained in the signaling registers has been rearranged. See section 17 of the DS2155 data sheet for additional information on signaling operation.

DS21x54 Register: *RS1 to RS16: Receive Signaling Registers*
DS21x54 Register Address: *30 to 3F Hex*

- The Receive signaling registers have been relocated to 60-6F Hex
- The following table shows the new the arrangement for the Receive Signaling Registers.

Transmit Signaling Registers (T1 Mode, ESF Format)

Register Name	DS2155 Address								
		(MSB)							(LSB)
RS1	60	CH2-A	CH2-B	CH2-C	CH2-D	CH1-A	CH1-B	CH1-C	CH1-D
RS2	61	CH4-A	CH4-B	CH4-C	CH4-D	CH3-A	CH3-B	CH3-C	CH3-D
RS3	62	CH6-A	CH6-B	CH6-C	CH6-D	CH5-A	CH5-B	CH5-C	CH5-D
RS4	63	CH8-A	CH8-B	CH8-C	CH8-D	CH7-A	CH7-B	CH7-C	CH7-D
RS5	64	CH10-A	CH10-B	CH10-C	CH10-D	CH9-A	CH9-B	CH9-C	CH9-D
RS6	65	CH12-A	CH12-B	CH12-C	CH12-D	CH11-A	CH11-B	CH11-C	CH11-D
RS7	66	CH14-A	CH14-B	CH14-C	CH14-D	CH13-A	CH13-B	CH13-C	CH13-D
RS8	67	CH16-A	CH16-B	CH16-C	CH16-D	CH15-A	CH15-B	CH15-C	CH15-D
RS9	68	CH18-A	CH18-B	CH18-C	CH18-D	CH17-A	CH17-B	CH17-C	CH17-D
RS10	69	CH20-A	CH20-B	CH20-C	CH20-D	CH19-A	CH19-B	CH19-C	CH19-D
RS11	6A	CH22-A	CH22-B	CH22-C	CH22-D	CH21-A	CH21-B	CH21-C	CH21-D
RS12	6B	CH24-A	CH24-B	CH24-C	CH24-D	CH23-A	CH23-B	CH23-C	CH23-D
RS13	6C	CH26-A	CH26-B	CH26-C	CH26-D	CH25-A	CH25-B	CH25-C	CH25-D
RS14	6D	CH28-A	CH28-B	CH28-C	CH28-D	CH27-A	CH27-B	CH27-C	CH27-D
RS15	6E	CH30-A	CH30-B	CH30-C	CH30-D	CH29-A	CH29-B	CH29-C	CH29-D
RS16	6F	CH32-A	CH32-B	CH32-C	CH32-D	CH31-A	CH31-B	CH31-C	CH31-D

DS21x54 Register: *TS1 to TS16: Transmit Signaling Registers*
DS21x54 Register Address: *40 to 4F Hex*

- Transmit Signaling Registers 1 through 16 can be found at addresses 50 Hex through 5F Hex.
- In E1 mode, TS16 carries the signaling information. This information can be in either CCS (Common Channel Signaling) or CAS (Channel Associated Signaling) format. The 32 time slots are referenced by two different channel number schemes in E1. In "Channel" numbering, TS0 through TS31 are labeled channels 1 through 32. In "Phone Channel" numbering TS1 through TS15 are labeled channel 1 through channel 15 and TS17 through TS31 are labeled channel 15 through channel 30. See table 17-1 in the DS2155 for more information.
- The following tables show the new the arrangement for the Transmit Signaling Registers for CAS and CCS formats.

Transmit Signaling Registers (E1 Mode, CAS Format)

Register Name	DS2155 Address								
		(MSB)							(LSB)
TS1	50	0	0	0	0	X	Y	X	X
TS2	51	CH2-A	CH2-B	CH2-C	CH2-D	CH1-A	CH1-B	CH1-C	CH1-D
TS3	52	CH4-A	CH4-B	CH4-C	CH4-D	CH3-A	CH3-B	CH3-C	CH3-D
TS4	53	CH6-A	CH6-B	CH6-C	CH6-D	CH5-A	CH5-B	CH5-C	CH5-D
TS5	54	CH8-A	CH8-B	CH8-C	CH8-D	CH7-A	CH7-B	CH7-C	CH7-D
TS6	55	CH10-A	CH10-B	CH10-C	CH10-D	CH9-A	CH9-B	CH9-C	CH9-D
TS7	56	CH12-A	CH12-B	CH12-C	CH12-D	CH11-A	CH11-B	CH11-C	CH11-D
TS8	57	CH14-A	CH14-B	CH14-C	CH14-D	CH13-A	CH13-B	CH13-C	CH13-D
TS9	58	CH16-A	CH16-B	CH16-C	CH16-D	CH15-A	CH15-B	CH15-C	CH15-D
TS10	59	CH18-A	CH18-B	CH18-C	CH18-D	CH17-A	CH17-B	CH17-C	CH17-D
TS11	5A	CH20-A	CH20-B	CH20-C	CH20-D	CH19-A	CH19-B	CH19-C	CH19-D
TS12	5B	CH22-A	CH22-B	CH22-C	CH22-D	CH21-A	CH21-B	CH21-C	CH21-D
TS13	5C	CH24-A	CH24-B	CH24-C	CH24-D	CH23-A	CH23-B	CH23-C	CH23-D
TS14	5D	CH26-A	CH26-B	CH26-C	CH26-D	CH25-A	CH25-B	CH25-C	CH25-D
TS15	5E	CH28-A	CH28-B	CH28-C	CH28-D	CH27-A	CH27-B	CH27-C	CH27-D
TS16	5F	CH30-A	CH30-B	CH30-C	CH30-D	CH29-A	CH29-B	CH29-C	CH29-D

Transmit Signaling Registers (E1 Mode, CCS Format)

Register Name	DS2155 Address								
		(MSB)							(LSB)
TS1	50	1	2	3	4	5	6	7	8
TS2	51	17	18	19	20	9	10	11	12
TS3	52	33	34	35	36	25	26	27	28
TS4	53	49	50	51	52	41	42	43	44
TS5	54	65	66	67	68	57	58	59	60
TS6	55	81	82	83	84	73	74	75	76
TS7	56	97	98	99	100	89	90	91	92
TS8	57	113	114	115	116	105	106	107	108
TS9	58	13	14	15	16	121	122	123	124
TS10	59	29	30	31	32	21	22	23	24
TS11	5A	45	46	47	48	37	38	39	40
TS12	5B	61	62	63	64	53	54	55	56
TS13	5C	77	78	89	80	69	70	71	72
TS14	5D	93	94	95	96	85	86	87	88
TS15	5E	109	110	111	112	101	102	103	104
TS16	5F	125	126	127	128	117	118	119	120

Per-Channel Code Generation Registers

The method for generating idle codes has changed in the DS2155. The DS2155 contains a 64-byte Idle Code Array accessed by the Idle Array Address Register (IAAR) and the Per-Channel Idle Code Register (PCICR). The contents of the array contain the idle codes to be substituted into the appropriate transmit or receive channels. This substitution can be enabled and disabled on a per-channel basis by the Transmit Channel Idle Code Enable registers (TCICE1-4) and Receive Channel Idle Code Enable registers (RCICE1-4). The following table gives the DS2155 register that closely resembles the corresponding DS21x54 register. See section 18 of the DS2155 for additional information on per-channel idle code generation.

DS21x54Register: *TIR1, TIR2, TIR3, TIR4: Transmit Idle Registers 1, 2, 3, 4*
DS21x54 Register Address: *26, 27, 28 , 29 Hex*

DS21x54Register: *TIDR: Transmit Idle Definition Register*
DS21x54 Register Address: *2A Hex*

DS21x54Register: *TC1 to TC32: Transmit Channel Registers*
DS21x54 Register Address: *60 to 7F Hex*

DS21x54Register: *TCC1, TCC2, TCC3, TCC4: Transmit Channel Control Registers 1-4*
DS21x54 Register Address: *A0, A1, A2, A3 Hex*

DS21x54Register: *RC1 to RC32: Receive Channel Registers*
DS21x54 Register Address: *80 to 9F Hex*

DS21x54Register: *RCC1, RCC2, RCC3, RCC4: Receive Channel Control Registers*
DS21x54 Register Address: *A4, A5, A6, A7 Hex*

DS21x54 Register	DS21x54 Register Abbreviation	DS2155 Register Abbreviation	DS2155 Address (Hex)
Transmit Idle Register 1	TIR1 (26 Hex)	TCICE1	80
Transmit Idle Register 2	TIR2 (27 Hex)	TCICE2	81
Transmit Idle Register 3	TIR3 (28 Hex)	TCICE3	82
Transmit Idle Register 4	TIR4 (29 Hex)	TCICE4	83
Transmit Idle Definition Register	TIDR (7F Hex)	PCICR	7F
Transmit Channel Control Register 1	TCC1 (A0 Hex)	PCDR1	29
Transmit Channel Control Register 2	TCC2 (A1 Hex)	PCDR2	2A
Transmit Channel Control Register 3	TCC3 (A2 Hex)	PCDR3	2B
Transmit Channel Control Register 4	TCC4 (A3 Hex)	PCDR4	2C
Transmit Channel Registers 1 to 32	TC1 to TC32	*	*
Receive Channel Registers 1 to 32	RC1 to RC32	*	*
Receive Channel Control Registers 1-4	RCC1 to RCC3	*	*

- TC1 to TC32, RC1 to RC32, and RCC1 to RCC4 have been incorporated in the new functionality of the per-channel idle code generation. See section 18 of the DS2155 data sheet for more detail.

Channel Blocking Registers

DS21x54 Register: *RCBR1, RCBR2, RCBR3, RCBR4: Receive Channel Block Registers*
DS21x54 Register Address: *2B, 2C, 2D, 2E Hex*

DS21x54 Register: *TCBR1, TCBR2, TCBR3, TCBR4: Transmit Channel Block Registers*
DS21x54 Register Address: *22, 23, 24, 25 Hex*

DS21x54 Register	DS21x54 Register Abbreviation	DS2155 Register Abbreviation	DS2155 Address (Hex)
Receive Channel Block Register 1	RCBR1 (2B Hex)	RCBR1	88
Receive Channel Block Register 2	RCBR2 (2C Hex)	RCBR2	89
Receive Channel Block Register 3	RCBR3 (2D Hex)	RCBR3	8A
Receive Channel Block Register 4	RCBR4 (2E Hex)	RCBR4	8B
Transmit Channel Block Register 1	TCBR1 (22 Hex)	TCBR1	8C
Transmit Channel Block Register 2	TCBR2 (23 Hex)	TCBR2	8D
Transmit Channel Block Register 3	TCBR3 (24 Hex)	TCBR3	8E
Transmit Channel Block Register 4	TCBR4 (25 Hex)	TCBR4	8F

Additional (Sa) and International (Si) Bit Operation Registers

DS21x54 Register	DS21x54 Register Abbreviation	DS2155 Register Abbreviation	DS2155 Address (Hex)
Receive Align Frame Register	RAF (2F Hex)	RAF	C6
Receive Non-Align Frame Register	RNAF (1F Hex)	RNAF	C7
Transmit Align Frame Register	TAF (20 Hex)	TAF	D0
Transmit Non-Align Frame Register	TNAF (21 Hex)	TNAF	D1
Receive Si-Bits Align Frame	RSiAF (58 Hex)	RSiAF	C8
Receive Si-Bits Non-Align Frame	RSiNAF (59 Hex)	RSiNAF	C9
Receive Remote Alarm Register	RRA (5A Hex)	RRA	CA
Receive Sa4 Register	RSa4 (5B Hex)	RSa4	CB
Receive Sa5 Register	RSa5 (5C Hex)	RSa5	CC
Receive Sa6 Register	RSa6 (5D Hex)	RSa6	CD
Receive Sa7 Register	RSa7 (5E Hex)	RSa7	CE
Receive Sa8 Register	RSa8 (5F Hex)	RSa8	CF
Transmit Si-Bits Align Frame	TsiAF (50 Hex)	TsiAF	D2
Transmit Si-Bits Non-Align Frame	TsiNAF (51 Hex)	TsiNAF	D3
Transmit Remote Alarm Register	TRA (52 Hex)	TRA	D4
Transmit Sa4 Register	TSa4 (53 Hex)	TSa4	D5
Transmit Sa5 Register	TSa5 (54 Hex)	TSa5	D6
Transmit Sa6 Register	TSa6 (55 Hex)	TSa6	D7
Transmit Sa7 Register	TSa7 (56 Hex)	TSa7	D8
Transmit Sa8 Register	TSa8 (57 Hex)	TSa8	D9
Transmit Sa Bit Control Register	TSaCR (1C Hex)	TSaCR	DA

HDLC Registers

While the DS21x54 has only one HDLC controller, the DS2155 has two enhanced HDLCs. Each controller is configurable for use with time slots, or Sa4 to Sa8 bits (E1 Mode) or the FDL (T1 Mode). The transmit and receive path buffers in the DS2155 have been doubled to 128-bytes. When used with time slots, the user can select any time slot or multiple time slots, contiguous or non-contiguous, as well as any specific bits within the time slot(s) to assign to the HDLC controllers.

The HDLC controller performs the necessary overhead for generating and receiving Performance Report Messages (PRM) as described in ANSI T1.403 and the messages as described in AT&T TR54016. The HDLC controller automatically generates and detects flags, generates and checks the CRC check sum, generates and detects abort sequences, stuffs and de-stuffs zeros, and byte aligns to the data stream. The 128-byte buffers in the HDLC controller are large enough to allow a full PRM to be received or transmitted without host intervention.

The user must take care to not map both transmit HDLC controllers to the same Sa bits, time slots or, in T1 mode, map both controllers to the FDL. HDLC #1 and HDLC #2 are identical in operation and therefore, when applicable, each DS21x52 register bit will be mapped to two addresses.

DS21x54 Register: *HCR: HDLC Control Register*
DS21x54 Register Address: *B0 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	-	-	-
6	RHR	HxRC*	31.7 32.7
5	TFS	HxTC*	90.3 A0.3
4	THR	HxTC*	90.5 A0.5
3	TABT	HxTC*	*See below*
2	TEOM	HxTC*	90.2 A0.2
1	TZSD	HxTC*	90.1 A0.1
0	TCRCD	HxTC*	90.0 A0.0

- HxTC refers to H1TC and H2TC located at addresses 90 Hex and A0 Hex respectively.
- HxRC refers to H1RC and H2RC located at addresses 31 Hex and 32 Hex respectively.
- TABT, bit 3, has been incorporated into the Transmit HDLC Reset (THR) bit.

DS21x54 Register: *HSR: HDLC Status Register*
DS21x54 Register Address: *B1 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	FRCL	SR2	18.1
6	RPE	SR6 SR7	20.5 22.5

5	RPS	SR6 SR7	20.4 22.4
4	RHALF	SR6 SR7	20.3* 22.3*
3	RNE	SR6 SR7	20.2 22.2
2	THALF	SR6 SR7	20.1* 22.1*
1	TNF	SR6 SR7	20.0 22.0
0	TMEND	SR6 SR7	20.6 22.6

- The status bits for HDLC #1 have been mapped to Status Register 6 (SR6) in the DS2155.
- The status bits for HDLC #2 have been mapped to Status Register 7 (SR7) in the DS2155.
- THALF, bit 2, has been renamed to TLWM. In the DS21x54, THALF is set when the transmit 64-byte FIFO empties beyond the halfway point. For the DS2155, the TLWM bit will be set when the transmit 128-byte FIFO empties beyond the low water mark as defined by the TFLWM0-TFLWM2 bits located in the FIFO control register (H1FC, H2FC). The low water mark is programmable to one of 8 different levels.
- RHALF, bit 4, has been renamed to RHWM. In the DS21x54, RHALF is set when the receive 64-byte FIFO fills beyond the halfway point. For the DS2155, the RHWM bit will be set when the receive 128-byte FIFO fills beyond the high water mark as defined by the RFHWM0-RFHWM2 bits located in the FIFO control register (H1FC, H2FC). The high water mark is programmable to one of 8 different levels.

DS21x54 Register: HIMR: *HDLC Interrupt Mask Register*
DS21x54 Register Address: *B2 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	FRCL	IMR2	19.1
6	RPE	IMR6 IMR7	21.5 23.5
5	RPS	IMR6 IMR7	21.4 23.4
4	RHALF	IMR6 IMR7	21.3* 23.3*
3	RNE	IMR6 IMR7	21.2 23.2
2	THALF	IMR6 IMR7	21.1* 23.1*
1	TNF	IMR6 IMR7	21.0 23.0
0	TMEND	IMR6 IMR7	21.6 23.6

- The interrupt mask bits for HDLC #1 have been mapped to HDLC Interrupt Mask Register 6 (IMR6)

in the DS2155.

- The interrupt mask bits for HDLC #2 have been mapped to HDLC Interrupt Mask Register 7 (IMR7) in the DS2155.
- THALF, bit 2, has been renamed to TLWM. When THALF is enabled in the DS21x54, the device will generate an interrupt when the transmit 64-byte FIFO empties beyond the halfway point. For the DS2155, the device will generate an interrupt, if TLWM is enabled, when the transmit 128-byte FIFO empties beyond the low water mark as defined by the TFLWM0-TFLWM2 bits located in the FIFO control register (H1FC, H2FC). The low water mark is programmable to one of 8 different levels.
- RHALF, bit 4, has been renamed to RLWM. When RHALF is enabled in the DS21x54, the device will generate an interrupt when the receive 64-byte FIFO fills beyond the halfway point. For the DS2155, the device will generate an interrupt, if RHWM is enabled, when the receive 128-byte FIFO fills beyond the high water mark as defined by the RFHWM0-RFHWM2 bits located in the FIFO control register (H1FC, H2FC). The high water mark is programmable to one of 8 different levels.

DS21x54 Register: *RHIR: Receive HDLC Information Register*
DS21x54 Register Address: *B3 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	RABT	INFO5 INFO6	*See below*
6	RCRCE	INFO5 INFO6	*See below*
5	ROVR	INFO5 INFO6	*See below*
4	RVM	INFO5 INFO6	*See below*
3	REMPTY	INFO5 INFO6	2E.3 2F.3
2	POK	INFO5 INFO6	*See below*
1	CBYTE	HxRPBA*	9C.7* AC.7*
0	OBYTE	INFO4*	#1 2D.0* #2 2D.2*

- The HDLC information bits for HDLC #1 have been mapped to the Receive HDLC #1 Information Register, INFO5.
- The HDLC information bits for HDLC #2 have been mapped to the Receive HDLC #2 Information Register, INFO6.
- OBYTE, bit 0, is renamed as H1OBT for HDLC #1 and H2OBT for HDLC #2. Both H1OBT & H2OBT can be found in the HDLC Event Information Register (INFO4, address 2D Hex). There is no new functionality associated with this bit.
- HxRPBA refers to H1RPBA and H2RPBA, located at addresses 9C Hex and AC Hex respectively.
- CBYTE, bit 1, has been renamed as MS. Unlike the operation of the CBYTE bit in the DS21x52, the MS bit will be low when the byte available for reading the receive FIFO is the last byte of a message. MS will be high when the byte available for reading is the first byte of the continuation of a message.

- POK, bit 2, has been incorporated into the Receive Packet Status bits (PS0-PS2) located in INFO5 and INFO6.
- RVM, bit 4, has been incorporated into the Receive Packet Status bits (PS0-PS2) located in INFO5 and INFO6.
- ROVR, bit 5, has been incorporated into the Receive Packet Status bits (PS0-PS2) located in INFO5 and INFO6.
- RCRCE, bit 6, has been incorporated into the Receive Packet Status bits (PS0-PS2) located in INFO5 and INFO6.
- RABT, bit 7, has been incorporated into the Receive Packet Status bits (PS0-PS2) located in INFO5 and INFO6.

DS21x54 Register: *RHFR: Receive HDLC FIFO Register*
DS21x54 Register Address: *B4 Hex*

- The Receive HDLC FIFO Register has been relocated to address 9E Hex for HDLC #1 and AE Hex for HDLC #2.
- The lower 7 bits of the Receive Packet Bytes Available registers (H1RPBA, H2RPBA) indicate the number of bytes that can be read from the receive FIFO. The value indicated by the lower seven bits in these registers informs the host as to how many bytes can be read from the receive FIFO without going past the end of a message. This value will refer to one of four possibilities, the first part of a packet, the continuation of a packet, the last part of a packet, or a complete packet. After reading the number of bytes indicated by this register the host then checks the HDLC Information register for detailed message status. See section 24.4.2 of the DS2155 data sheet for additional information.

DS21x54 Register: *THIR: Transmit HDLC Information Register*
DS21x54 Register Address: *B6 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	-	-	-
6	-	-	-
5	-	-	-
4	-	-	-
3	-	-	-
2	TEMPTY	INFO5 INFO6	2E.5 2F.5
1	TFULL	INFO5 INFO6	2E.4 2F.4
0	TUDR	INFO4*	#1 2D.1* #2 2D.3*

- TUDR, bit 0, is renamed as H1UDR for HDLC #1 and H2UDR for HDLC #2. Both H1UDR & H2UDR can be found in the HDLC Event Information Register (INFO4, address 2D Hex). There is no new functionality associated with this bit.

DS21x54 Register: *THFR: Transmit HDLC FIFO*
DS21x54 Register Address: *B7 Hex*

- The Transmit HDLC FIFO Register has been relocated to address 9D Hex for HDLC #1 and AD

Hex for HDLC #2.

- The Transmit FIFO Buffer Available registers (H1TFBA, H2TFBA) indicate the number of bytes that can be written into the transmit FIFOs. The count from this register informs the host as to how many bytes can be written into the transmit FIFO without overflowing the buffer.

DS21x54 Register: *RDC1: Receive HDLC DS0 Control Register 1*
DS21x54 Register Address: *B8 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	RHS	*See below*	*See below*
6	RSaDS	HxRC*	31.6* 32.6*
5	RDS0M	*See below*	*See below*
4	RD4	*See below*	*See below*
3	RD3	*See below*	*See below*
2	RD2	*See below*	*See below*
1	RD1	*See below*	*See below*
0	RD0	*See below*	*See below*

- RD0 through RD4, bits 0 to 4, RDS0M, bit 5, and RHS, bit 7, have been replaced by registers H1RCS1 to H1RCS4 for HDLC #1 and H2RCS1 to H2RCS4 for HDLC #2. Any channel or combination of channels, contiguous or not, can be assigned to an HDLC controller. When assigned to a channel(s) any combination of bits within the channel(s) can be avoided. See section 24.3 of the DS2155 for additional information on mapping the HDLC data to channels.
- HxRC refers to H1RC and H2RC located at addresses 31 Hex and 32 Hex respectively.
- RSaDS, bit 6, has been replaced by RHMS. See section 24.3 of the DS2155 data sheet for additional information on mapping the receive data The mapping of HDLC data to Sa bits The operation of this bit is inverted from that of the DS21x52. See section 24 of the DS2155 for additional information on mapping the HDLC data to channels or Sa bits.

DS21x54 Register: *RDC2: Receive HDLC DS0 Control Register 2*
DS21x54 Register Address: *B9 Hex*

- Receive HDLC DS0 Control Register 2 has been relocated to 96 Hex for HDLC #1 and A6 Hex for HDLC #2.

DS21x54 Register: *TDC1: Transmit HDLC DS0 Control Register 1*
DS21x54 Register Address: *BA Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	THE	*See below*	*See below*
6	TSaDS	HxTC	90.4* A0.4*
5	TDS0M	*See below*	*See below*
4	TD4	*See below*	*See below*
3	TD3	*See below*	*See below*
2	TD2	*See below*	*See below*

1	TD1	*See below*	*See below*
0	TD0	*See below*	*See below*

- TD0 through TD4, bits 0 to 4, and TDS0M, bit 5, have been replaced by registers H1TCS1 to H1TCS4 for HDLC #1 and H2TCS1 to H2TCS4 for HDLC #2. Any channel or combination of channels, contiguous or not, can be assigned to an HDLC controller. When assigned to a channel(s) any combination of bits within the channel(s) can be avoided. See section 24.3 of the DS2155 for additional information on mapping the HDLC data to channels.
- HxTC refers to H1TC and H2TC located at addresses 90 Hex and A0 Hex respectively.
- TSaDS, bit 6, has been renamed to THMS. The operation of this bit is inverted from that of the DS21x54. See section 24 of the DS2155 for additional information.
- THE, bit 7, has been incorporated into the DS2155 via the TFDLS bit in register T1TCR1. Also, see section 24 for additional information on configuring the 2 HDLCs.

DS21x54 Register: *TDC2: Transmit HDLC DS0 Control Register 2*
DS21x54 Register Address: *BB Hex*

- Transmit HDLC DS0 Control Register 2 has been relocated to 9B Hex for HDLC #1 and AB Hex for HDLC #2.

Line Interface Control Register

DS21x54 Register: *LICR: Line Interface Control Register*
DS21x54 Register Address: *7C Hex*

- The Line Interface Control Register has been relocated to 78 Hex. The DS2155 data sheet refers to the register as Line Interface Control 1 (LIC1).

Interleaved PCM Bus Operation Register

The interleave bus operation has been converted to full software control in the DS2155 and the external pins associated with this option have been reassigned to the extended system information bus function. See section 29 for more detail on the interleaved PCM bus operation.

DS21x54 Register: *IBO: Interleaved Bus Operation Register*
DS21x54 Register Address: *B5 Hex*

Bit #	Name	55 Abbrv.	55 Addr.Bit
7	-	-	-
6	-	-	-
5	-	-	-
4	-	-	-
3	IBOEN	IBOC	C5.3
2	INTSEL	IBOC	C5.4*
1	MSEL0	*See below*	*See below*
0	MSEL1	*See below*	*See below*

- MSEL0 and MSEL1 are not included in the DS2155.
- INTSEL, bit 2, has been renamed IBOSEL. There is no new functionality associated with this control bit.

4. New DS2155 Features

The DS2155 contains all of the features found in the previous generations of Dallas Semiconductor's SCTs plus many more. Some additional features are subtle changes while others are new additions. The scope of this paper is to identify some of the new features that the DS2155 offers without getting into the specifics that are outlined in the DS2155 data sheet.

4.1 Key Additional Features in the DS2155

The follow is a list of some of the new features in the DS2155. See the DS2155 for additional information.

- Line Interface
  - Requires only a 2.048 MHz master clock for both E1 and T1 operation with an option to use a 1.544 MHz master clock for T1 operation.
  - Receive level indication in 2.5dB steps from -42.5dB to -2.5dB.
  - Internal receive termination option for 75, 100, and 120 ohm lines.
  - Square wave output.
  - Transmitter 50mA short circuit limiter with current limit exceeded indication.
  - Transmit open circuit detected indication.
  - Code Mark Inversion option.
- Clock Synthesizer
  - Output frequency includes 16.384 MHz option.
- Jitter Attenuator
  - Requires only a 2.048 MHz master clock for both E1 and T1 operation with an option to use a 1.544 MHz master clock for T1 operation.
- Framer/Formatter
  - RAI-CI detection and generation.
  - AIS-CI detection and generation.
  - E1 ETS 300 011 RAI generation.
  - G.965 V5.2 link detection.
  - In-band repeating pattern generators and detectors support up to 16-bits in length.
  - Hardware pins added to indicate carrier loss and signaling freeze.
  - Option to extend carrier loss criteria to a 1ms period as per ETS 300 233.
  - Additional events capable of generating interrupts.
- System Interface
  - Maximum backplane burst rate increased to 16.384 MHz.
- HDLC
  - Two independent HDLCs.
  - Fast load and unload features for the FIFOs.
  - SS7 support for FISU transmit and receive.
  - Transmit and receive buffers increased to 128-bytes.
  - Programmable fill levels for transmit and receive buffers.
- Test and Diagnostics
  - Programmable On-chip Bit Error Rate Testing.
  - Pseudorandom patterns including QRSS.
  - Daly pattern.

    - Error insertion single and continuos.
    - Total bit and errored bit counts.
    - Payload Error Insertion.
    - Error insertion in the payload portion of the T1 frame in the transmit path.
    - Errors can be inserted over the entire frame or selected channels.
    - Insertion options include continuous and absolute number with selectable insertion rates.
    - F-Bit corruption for line testing.
- Extended System Information Bus
    - Allows the host to read interrupt and alarm status on up to 8 ports with a single bus read. See section 4.2.3 of this note and section 30 of the DS2155 data sheet for more information.
- User Programmable Output Pins
    - Four user defined output pins for controlling external logic.
- Control Port
    - Software reset supported.
    - Flexible register space resets.

4.2 High Throughput Features in the DS2155

In addition to the features listed above, the DS2155 has several features designed to improve throughput efficiency and provide overhead relief for the host processor. The following sections give a brief overview of new features; however, please refer to the DS2155 data sheet for detailed information on each of these features.

4.2.1 Bytes Available (HDLC Controller)

The transmit and receive portion of the HDLC controllers have improved throughput features. All of these features allow the host to read and write BLOCKS of data without having to check status bits on a per-byte basis.

1. Transmit Bytes Buffer Available registers (Address 9Fh & AFh): The host can read this register to see how many bytes can be written into the transmit FIFO without over flowing the FIFO. The transmit FIFO can contain multiple messages. Also there are programmable low water marks on the transmit FIFO (this replaces the Haft Empty flag).
2. Receive Packets Bytes Available registers (Address 9Ch & ACh): The host can read this register to determine how many bytes can be read from the receive FIFO without under flowing the buffer or reading past the end of a message. Also there are programmable high water marks on the receive FIFOs.

4.2.2 SS7 Support (HDLC Controller)

Both the transmit and receive portions of the HDLC controllers have features that improve support for SS7.

1. Transmit FIFO Loop control. The transmitter has a loop feature that allows it to loop on a message in the transmit FIFO. For SS7 FISUs (Fill In Signal Units) the host only needs to write the FISU (containing the last FSN and BSN values of the last regular message unit) once. The transmitter can then repeat the FISU without host intervention until a normal message unit is ready to be transmitted.
2. Receive Consecutive FISU Detect and Delete. On the receive side, the controller will recognize a Fill In Signal Unit by its length. If the CRC is correct and the BSN is a repeat of the last signal unit's BSN, the controller will disregard the FISU without host intervention. Erred FISUs will be reported to the host.

4.2.3 Extended System Information Bus (ESIB)

The ESIB allows up to eight DS2155s to share an 8 bit CPU bus for the purpose of reporting alarm in interrupt status as a group. With a single bus read, the host can be updated with alarm or interrupt status from all eight devices. There are four registers, ESI0, ESI1, ESI2 and ESI4. As an example, 8 DS2155s can be grouped into an ESIB group. A single read of the ESI0 register of ANY member of the group will yield the interrupt status of all 8 DS2155s. Therefore the host can determine which device or devices are causing an interrupt without polling all eight devices. Via ESI1 the host can gather synchronization status on all members of the group. ESI2 and ESI4 can be programmed to report various alarms on a device by device basis.

5. Hardware Considerations: DS2155 vs. DS21x5y

The DS2155 is pin compatible with existing DS21x5y devices. This section addresses two scenarios. Scenario #1 involves placing a DS2155 into an existing DS21x5y design. In this situation, some of the new features of the DS2155 will be unavailable; however, all of the DS21x5y functionality is available. Scenario # 2 involves generating a new design based on the DS21x5y but allowing for migration to the DS2155 when available and making use of the new features. Table 1 shows a summary of the pin changes.

Table 1. Summary of Pin Changes

PIN	DS21x5y	DS2155	Comment
3	8MCLK	BPCLK	This pin is now programmable to 4.096, 8.192 or 16.384MHz
8	NC	UOP0	Bit 0 of a four bit user port
9	NC	UOP1	Bit 1 of a four bit user port
14	TEST	TSTRST	This pin will now force a register reset when high along with forcing all outputs and I/O pins into high Z.
15	NC	UOP2	Bit 2 of a four bit user port
23	NC	UOP3	Bit 3 of a four bit user port
76	FMS	ESIBRD	FMS deleted and pin reused for ESIB
36	CI	ESIBS0	CI function now controlled via software. Pin used for ESIB
54	CO	ESIBS1	CO function now controlled via software. Pin used for ESIB
26	NC	NC	Must remain a No Connect
27	NC	NC	Must remain a No Connect
28	NC	NC	Must remain a No Connect

5.1 Reassigned Pin Functions for Pins 36, 54, and 76

The Interleave Bus Option (IBO) has been converted to full software control in the DS2155 and the pins (CO, CI) reassigned to the ESIB function. These pins plus FMS are now used for a new feature (Extended System Information Bus). In this application, up to 4 SCTs can share a single, higher speed PCM bus as shown in Figure 1a. The CO and CI signals were used to establish the master/slave relationship of the devices. In the DS2155 this relationship is software configurable and the CO/CI pin function is deleted. In the DS2155 these pins have been used for another function, the ESIB as shown in Figure 1b. In addition, the FMS pin function has been deleted and replaced with a new signal to support the ESIB.

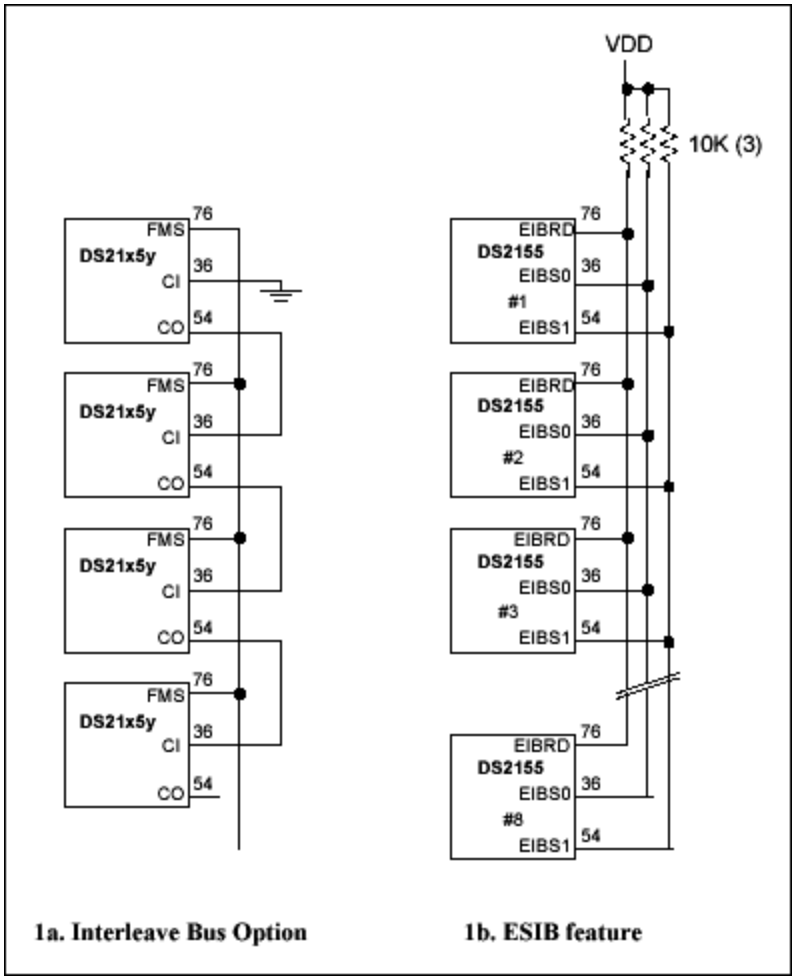

Figure 1. Pins 36, 54 and 76 usage.

Scenario #1
When the DS2155 is used in an existing DS21x5y design the ESIB must not be enabled. In this case, pins 36, 54 and 76 enter a high Z state and are therefore not affected by existing CO/CI connections. When using the DS2155 in an existing DS21x5y design the IBOs hierarchy is configured via software. The ESIB function of the DS2155 is not available in this situation.

Scenario #2
When provisioning a new DS21x5y design to accept the DS2155 the designer must plan for the reconfiguration of these pins on the PCB in order to use the ESIB feature.

5.2 New Feature for Pin 3

The TEST pin in the DS21x5y has been renamed to TSTRST in the DS2155. In the DS21x5y this pin would force all outputs and I/Os to high Z. In the DS2155 this pin will cause a register reset when set high along with forcing all outputs and I/O pins to a high Z state.

5.3 New Feature for Pin 14

The 8MCLK pin of the DS21x5y has been renamed to BPCLK in the DS2155. In the DS21x5y this pin was an 8.192MHz output. In the DS2155 this pin can be programmed to output 2.048, 4.096, 8.192, or 16.384MHz.

Scenario #1
When the DS2155 is used in an existing DS21x5y design this pin can be programmed to 8.192MHz by setting register CCR2 = 05h

5.4 Receive and Transmit Termination

The DS2155 has an enhanced line interface unit (LIU). There are internal, software selectable provisions for terminating the receive and transmit pair. Receive and transmit termination can be altered via software in the DS2155 eliminating the need to change external components. Shown in Figure 2 is the basic interface circuit for the DS2135y (3.3 volt) family. Rt is set to 0 ohms for T1, and to 11.6 ohms or 6.2 ohms in E1 mode depending on the line type (120 ohm twisted pair or 75 ohm coax) when a high return loss value is required. R is set to 50 ohms for T1 and 37.5 ohms or 60 ohms for E1 operation depending on the line type.

Scenario #1
When the DS2155 is used in an existing DS2135y design, the internal termination features can be disabled if the external circuitry cannot be modified to allow the software controllable termination features to be utilized.

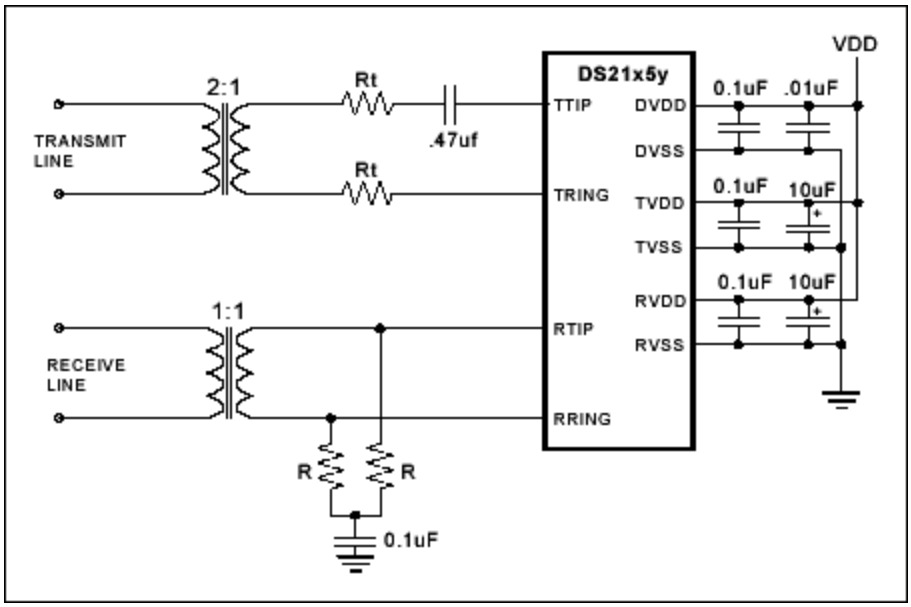

Figure 2. DS21x5y network interface.

Scenario #2
Figure 3 shows the basic circuit for the DS2155. In this circuit R is set to 60 ohms. This value is adjusted internally via software for T1 and E1 operation. Rt is not needed since the DS2155 transmitter can control source impedance via software for T1 and E1 operation. The user should consult factory application notes for "over voltage" protected interface designs.

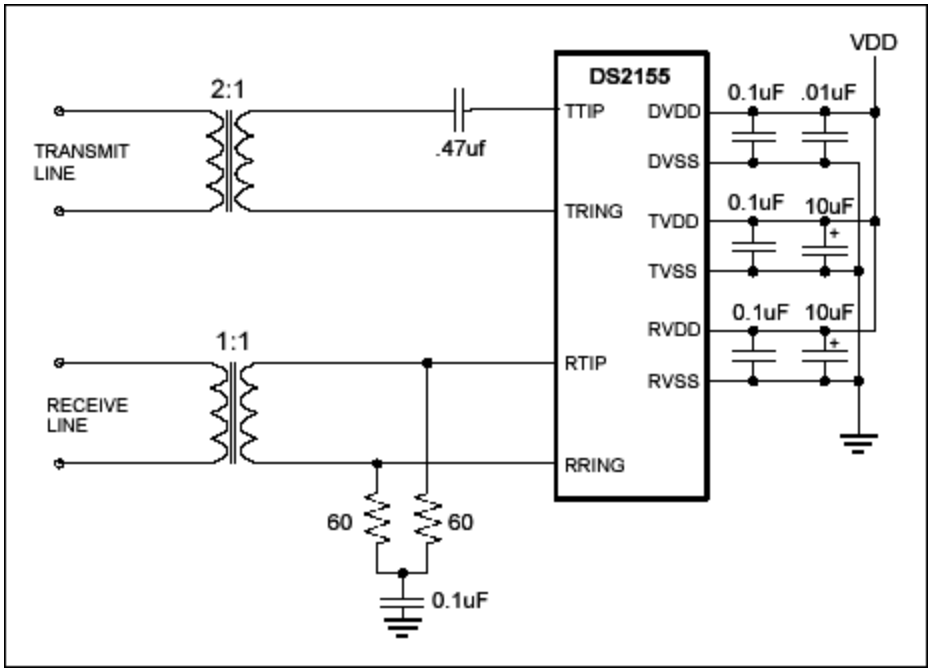

Figure 3. DS2155 network interface.

5.5 New User Output Pins in the DS2155

Four new pin functions have been added to the DS2155 to provide control of external user hardware. These pins replace 4 No Connects on the DS21x5y and are located at pins 8 (UOP0), 9 (UOP1), 23 (UOP2), and 15 (UOP3). Refer to Section 33 of the DS2155 data sheet for more information on these four pins.

Scenario #1
When using the DS2155 in an existing DS21x5y design the unterminated user outputs will not cause any problems.

Scenario #2
When provisioning a DS21x5y design to accept the DS2155, connections to these NC pins of the DS21x5y will not cause a problem.

6. Summary

The DS2155 is a T1, E1, and J1 Single Chip Transceiver (SCT) that builds upon the previous generation of SCTs offered by Dallas Semiconductor. In the process of combining the T1/J1 and E1 modes of operation into a single die, all of the functionality of the DS21x5y SCTs is kept intact, but many of the previous register addresses and control bits have been relocated in the DS2155. In addition to software considerations, the migration of designs from the DS21x5y to the DS2155 is simplified by the pin compatibility of the DS2155.

Related Parts		
DS21354	3.3V/5V E1 Single Chip Transceivers (SCT)	
DS2155	T1/E1/J1 Single-Chip Transceiver	Free Samples

DS21552	3.3V DS21352 and 5V DS21552 T1 Single Chip Transceivers	
DS21554	3.3V/5V E1 Single Chip Transceivers (SCT)	Free Samples
DS21Q352	Quad T1/E1 Transceiver (3.3V, 5.0V)	
DS21Q354	Quad T1/E1 Transceiver (3.3V, 5.0V)	
DS21Q55	Quad T1/E1/J1 Transceiver	
DS21Q552	Quad T1/E1 Transceiver (3.3V, 5.0V)	
DS21Q554	Quad T1/E1 Transceiver (3.3V, 5.0V)	

More Information
For Technical Support: http://www.maximintegrated.com/support
For Samples: http://www.maximintegrated.com/samples
Other Questions and Comments: http://www.maximintegrated.com/contact

Application Note 374: http://www.maximintegrated.com/an374
APPLICATION NOTE 374, AN374, AN 374, APP374, Appnote374, Appnote 374