The MAX3420E USB Interface Information Card

SPI Data

FDUPSPI = 1

FDUPSPI = 0 (default)

The FDUPSPI bit configures the SPI interface for full-duplex or half-duplex operation. In half-duplex mode (FDUPSPI = 0) the MISO pin can be left unconnected.

SPI Modes

The MAX3420E SPI interface works in modes (0,0) and (1,1) without alteration. The difference is the inactive SCK level. In both modes the data is changed on the SCK falling edge and sampled on the SCK rising edge. Full-duplex mode (FDUPSPI=1) is shown here.

INT pin configuration

INT pin waveforms for the three settings of the INTLEVEL and POSINT bits. In level mode the INT pin stays low until no interrupt requests are pending. In edge mode the INT pin delivers an edge whenever a new interrupt request occurs or an interrupt request bit is cleared while others are pending. The INTLEVEL mode is open-drain and requires a pullup resistor to VL.

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- A downloadable copy of this reference card
- Additional information on USB
- Maxim USB power and interface products

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Rev. August 16, 2005
To Send an IN Packet
1. Load an IN FIFO with data.
2. Load the EPINBC register with the byte count. This arms the transfer (next IN gets the data instead of a NAK).
3. INBAVIRQ asserts when packet is successfully sent.
4. Go to step 1.

To Read an OUT Packet
1. OUTDAV IRQ asserts when new OUT data is available.
2. Read the EPOUTBC register to determine how many bytes are available.
3. INBAVIRQ asserts when packet is successfully sent.
4. Re-arm the endpoint by clearing the OUTDAV IRQ bit.

**MAX3420E Resets.** For the three reset types, all register bits are cleared except the indicated bits in this table. The indicated BAVIRQ bits are set to 1, and the remaining bits shown in the table retain their states. The Revision register is read-only and is never cleared.

<table>
<thead>
<tr>
<th>Power On</th>
<th>RES# Pin or CHIPRES = 1</th>
<th>USB Bus Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN3BAVIRQ=1</td>
<td>IN3BAVIRQ=1</td>
<td>IN3BAVIRQ=1</td>
</tr>
<tr>
<td>IN2BAVIRQ=1</td>
<td>IN2BAVIRQ=1</td>
<td>IN2BAVIRQ=1</td>
</tr>
<tr>
<td>IN0BAVIRQ=1</td>
<td>IN0BAVIRQ=1</td>
<td>IN0BAVIRQ=1</td>
</tr>
<tr>
<td>CHIPRES</td>
<td>CHIPRES</td>
<td>CHIPRES</td>
</tr>
<tr>
<td>CONNECT</td>
<td>CONNECT</td>
<td>CONNECT</td>
</tr>
<tr>
<td>EPOFI0</td>
<td>EPIOUTFIFO</td>
<td>EP2INFIFO</td>
</tr>
<tr>
<td>EP3INFIFO</td>
<td>GP0UT[3:0]</td>
<td>GP0UT[3:0]</td>
</tr>
<tr>
<td>GP0UT[8:0]</td>
<td>GP0UT[8:0]</td>
<td>GP0UT[8:0]</td>
</tr>
<tr>
<td>HOS0CSTEN</td>
<td>HOS0CSTEN</td>
<td>HOS0CSTEN</td>
</tr>
<tr>
<td>IE</td>
<td>IE</td>
<td>IE</td>
</tr>
<tr>
<td>IN0LEVEL</td>
<td>IN0LEVEL</td>
<td>IN0LEVEL</td>
</tr>
<tr>
<td>POSINT</td>
<td>POSINT</td>
<td>POSINT</td>
</tr>
<tr>
<td>PWRD0WN</td>
<td>PWRD0WN</td>
<td>PWRD0WN</td>
</tr>
<tr>
<td>SIG0RW</td>
<td>SIG0RW</td>
<td>SIG0RW</td>
</tr>
<tr>
<td>URES0NIE</td>
<td>URES0NIE</td>
<td>URES0NIE</td>
</tr>
<tr>
<td>URESIE</td>
<td>URESIE</td>
<td>URESIE</td>
</tr>
</tbody>
</table>

**Full-duplex SPI mode (FDUPSPI=1) only:** These register bits simultaneously clock out on the MISO pin as the command byte is clocked into the MOSI pin.